

6ch White LED Driver Built-in Current Driver Buck-Boost DC/DC Controller for Automotive

BD81A76EFV-M

General Description

BD81A76EFV-M is a white LED driver with the capability of withstanding high input voltage (maximum 35 V). This driver has 6ch constant-current drivers in 1-chip, where each channel can draw up to 120 mA (Max), and it is suitable for high illumination LED drive. Furthermore, a buck-boost current mode DC/DC converter is also built to achieve stable operation during power voltage fluctuation. Light modulation (10,000:1@100 Hz dimming function) is possible by PWM input.

Key Specifications

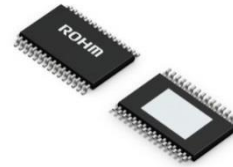
■ Operating Input Voltage Range	4.5 V to 35 V
■ Output LED Current Accuracy	±3.0 % @ 50 mA
■ DC/DC Oscillation Frequency	200 kHz to 2200 kHz
■ Operating Temperature	-40 °C to +125 °C
■ LED Maximum Output Current	120 mA/ch
■ PWM Minimum Pulse Width	1.0 μs

Packages

HTSSOP-B30

W (Typ) x D (Typ) x H (Max)

10.00 mm x 7.60 mm x 1.00 mm



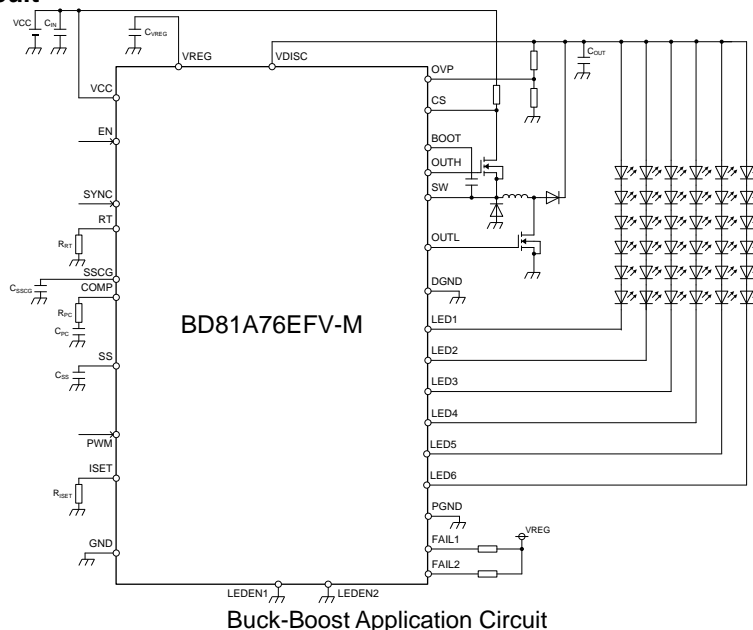
Features

- AEC-Q100 Qualified (Note 1)
 - 6ch Current Driver for LED Drive
 - Buck-Boost Current Mode DC/DC Converter
 - Control DC/DC Converter Oscillation Frequency by External Synchronized Signal
 - Spread Spectrum Function
 - LSI Protection Function (UVLO, OVP, TSD, OCP, SCP)
 - LED Abnormality Detection Function (Open/Short)
 - VOUT Discharge Function (Buck-Boost Structure Limitation)
- (Note 1) Grade 1

Applications

- Automotive CID (Center Information Display) Panel
- Car Navigation
- Cluster Panel
- HUD (Head Up Display)
- Small and Medium Type LCD Panels for Automotive Use

Typical Application Circuit



Buck-Boost Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

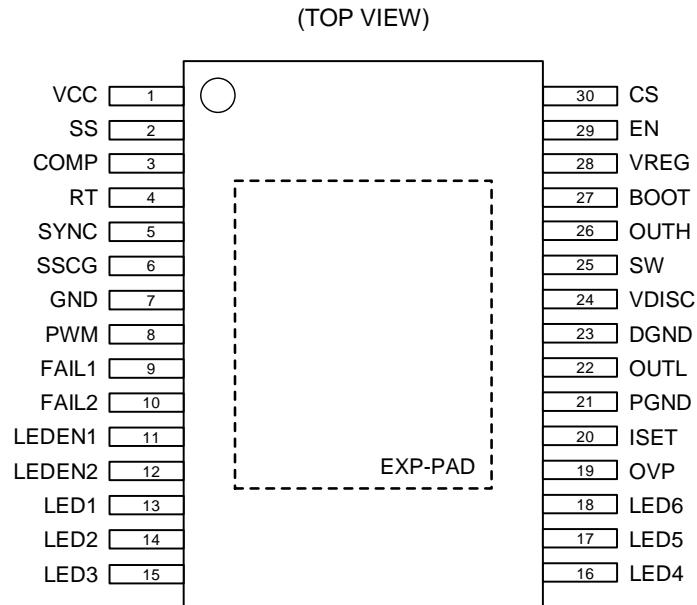
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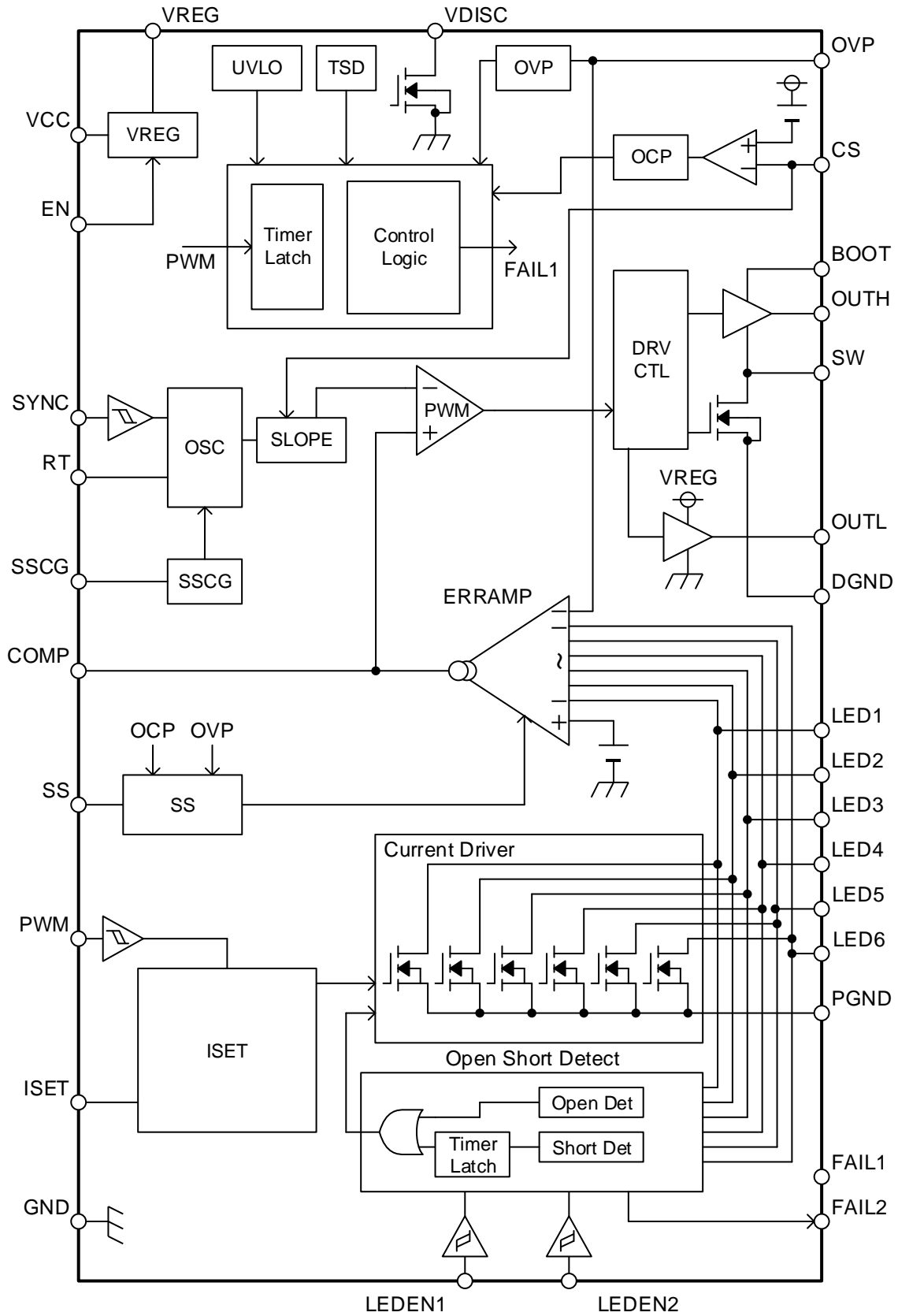
Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	VCC	Input power supply pin
2	SS	“Soft Start” capacitor connection
3	COMP	Error Amp output
4	RT	Oscillation frequency setting resistor connect
5	SYNC	External synchronization input pin
6	SSCG	Spread spectrum setting capacitor pin
7	GND	Small signal GND pin
8	PWM	PWM light modulation signal input pin
9	FAIL1	“Failure” signal output pin 1
10	FAIL2	“Failure” signal output pin 2
11	LEDEN1	Enable pin 1 for LED output
12	LEDEN2	Enable pin 2 for LED output
13	LED1	LED output pin 1
14	LED2	LED output pin 2
15	LED3	LED output pin 3
16	LED4	LED output pin 4
17	LED5	LED output pin 5
18	LED6	LED output pin 6
19	OVP	Over voltage detection pin
20	ISET	LED output current setting pin
21	PGND	LED output GND pin
22	OUTL	Low side FET gate pin
23	DGND	DC/DC converter output GND pin
24	VDISC	Output voltage discharge pin
25	SW	High side FET source pin
26	OUTH	High side FET gate pin
27	BOOT	High side FET driver power supply pin
28	VREG	Internal constant voltage
29	EN	Enable pin
30	CS	DC/DC converter input current sense pin
-	EXP-PAD	Back side thermal PAD (Connect to GND)

Block Diagram



Description of Blocks

If there is no description, the mentioned values are typical value.

1. Reference Voltage (VREG)

VREG Block generates 5 V at EN=High, and outputs to the VREG pin. This voltage (V_{VREG}) is used as power supply for internal circuit. It is also used to fix each input pin to High voltage outside IC. It cannot supply power to other parts than this IC. The VREG pin has UVLO function, and it starts operation at VCC ≥ 4.0 V and V_{VREG} ≥ 3.5 V and stops when at VCC ≤ 3.5 V or V_{VREG} ≤ 2.0 V. About the condition to release/detect VREG voltage, refer to [Table 2](#) on section 4 Protect Function. Connect a ceramic capacitor (C_{VREG}) to the VREG pin for phase margin. C_{VREG} range is 1.0 μF to 4.7 μF and recommended value is 2.2 μF. If the C_{VREG} is not connected, it might occur unstable operation e.g. oscillation.

2. Current Driver

Table 1. LED Control Logic

LEDEN1	LEDEN2	LED1	LED2	LED3	LED4	LED5	LED6
Low	Low	ON	ON	ON	ON	ON	ON
High	Low	ON	ON	ON	ON	ON	OFF
Low	High	ON	ON	ON	ON	OFF	OFF
High	High	ON	OFF	OFF	OFF	OFF	OFF

If there is the constant-current driver output not to use, make the LED1 to LED6 pin 'open' and turn off the channel, which is not used, with the LEDEN1 and LEDEN2 pins. The truth table for these pins is shown above. If the unused constant-current driver output is set open without the process of the LEDEN1 and LEDEN2 pins, the 'open detection' is activated. The LEDEN1 and LEDEN2 pins are pulled down internally in the IC and it is low at 'open' condition. They can be connected to the VREG pin and fixed to logic High. Logic of the LEDEN1 and LEDEN2 pins are not switchable during these in operation.

(1) Output Current Setting (R_{ISET})

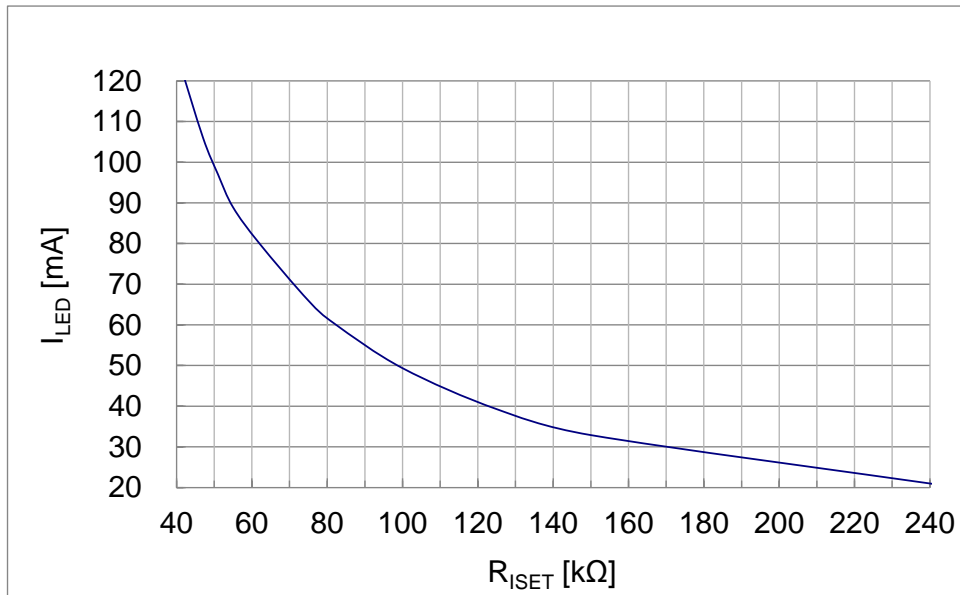


Figure 1. I_{LED} VS R_{ISET}

The Output Current I_{LED} can be obtained by the following equation:

$$I_{LED} = 5000/R_{ISET} \text{ [A]}$$

The operating range of the R_{ISET} value is from 41 kΩ to 250 kΩ. Additionally, the R_{ISET} value could not be changed during operation. In this IC, I_{SET}-GND short protection is built-in to protect an LED element from excess current when the ISET pin and GND are shorted. If the R_{ISET} value is 4.7 kΩ or less, the IC detects I_{SET}-GND short condition and LED current is turned off.

2. Current Driver - continued

(2) PWM Dimming Control

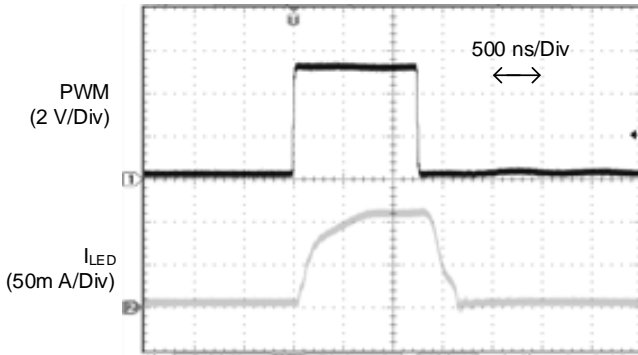


Figure 2. PWM=150 Hz, Duty=0.02 %, I_{LED} Waveform

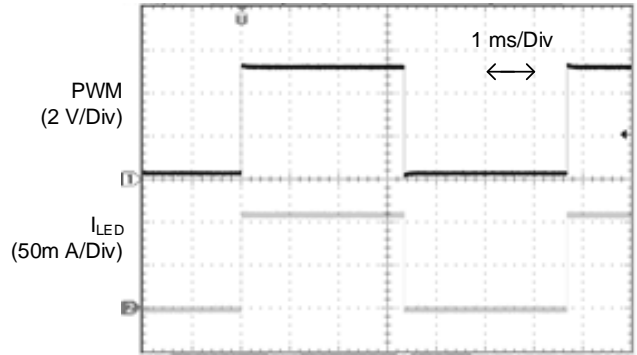


Figure 3. PWM=150 Hz, Duty=50.0 %, I_{LED} Waveform

The current driver ON/OFF is controlled by the PWM pin. The duty ratio of the PWM pin becomes duty ratio of I_{LED}. If PWM dimming is not totally used (i.e. 100 %), fix the PWM pin to High. Output light intensity is the highest at 100 %.

3. Buck-Boost DC/DC Controller

(1) Number of LED in Series Connection

This IC controls output voltage to become 1.0 V by detecting LED Cathode voltage (the LED1 to LED6 pin voltage). When multiple LED outputs are operating, it controls LED pin voltage with the highest LED Vf to become 1.0 V. Thus, the output voltage of other LED pins is higher by the variations of Vf. Set up Vf variation to meet the formula below.

$$LED\ Series\ Number \times Vf\ Variation < Short\ Detection\ Voltage\ (Min) - LED\ Control\ Voltage(Max)$$

(2) Over Voltage Protection (OVP)

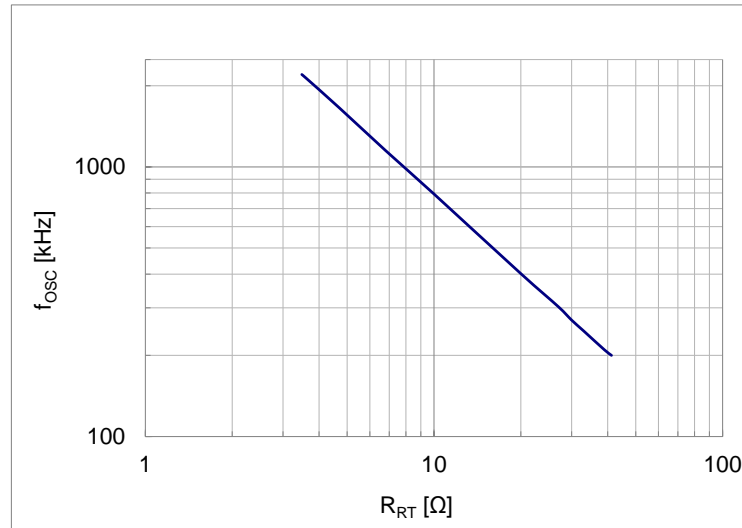
The output voltage (VOUT) should be connected to the OVP pin via resistor voltage divider. If the OVP pin voltage is 2.0 V or more, Over Voltage Protection (OVP) is active and stop the DC/DC converter switching. Determine the setting value of OVP function by the total number of the LEDs in the series and the Vf variation. When the OVP pin voltage drops less than 1.94 V after OVP operation, the OVP is released.

$$VOUT \geq \{(R_{OVP1} + R_{OVP2}) / R_{OVP1}\} \times 2.0$$

where:
 VOUT is the Output voltage.
 R_{OVP1} is the GND side OVP resistance.
 R_{OVP2} is the Output voltage side OVP resistance.

For example, OVP is active when VOUT ≥ 32 V if R_{OVP1}=22 kΩ and R_{OVP2}=330 kΩ.

3. Buck-Boost DC/DC Controller - continued

(3) Buck-Boost DC/DC Converter Oscillation Frequency (f_{osc})Figure 4. f_{osc} vs R_{RT}

DC/DC oscillation frequency can be set via a resistor connected to the RT pin. This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillation frequency. Please set the resistance of R_{RT} using the above data and the equation below.

$$f_{OSC} = (81 \times 10^5 / R_{RT}) \times \alpha \quad [\text{kHz}]$$

81×10^5 is the constant value determined in the internal circuit. α is coefficient for revision.

(RT: α = 41k Ω : 1.01, 27k Ω : 1.00, 18k Ω : 0.98, 10 k Ω : 0.96, 3.9k Ω : 0.91, 3.6k Ω : 0.9)

Take note that operation could not be guaranteed in the case of settings other than the recommended range.

3. Buck-Boost DC/DC Controller - continued

(4) Spread Spectrum Function

Operation in Spread Spectrum Clock Generation (SSCG) is possible by connecting capacitor to the SSCG pin. The SSCG pin has a comparator and constant current circuit to assume 0.6 V/0.48 V reference voltage, and changes into a triangular wave form. The average of noise can be reduced by changing the switching frequency by a frequency (f_{SSCG}) decided in the SSCG pin capacity C_{SSCG} . The band of the switching frequency becomes $90\% \pm 10\%$ of switching frequency when SSCG is not used.

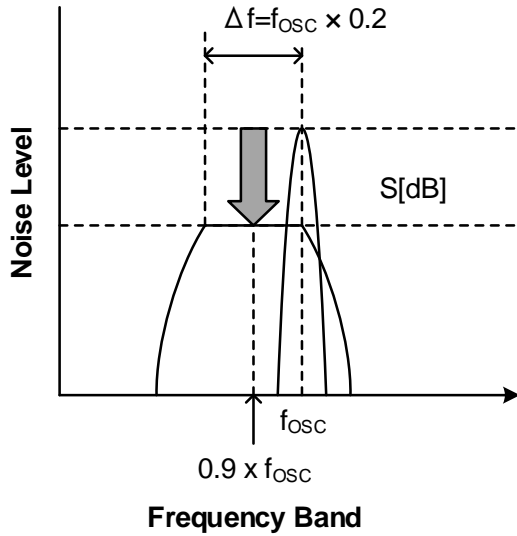


Figure 5. SSCG Noise Reduction Image

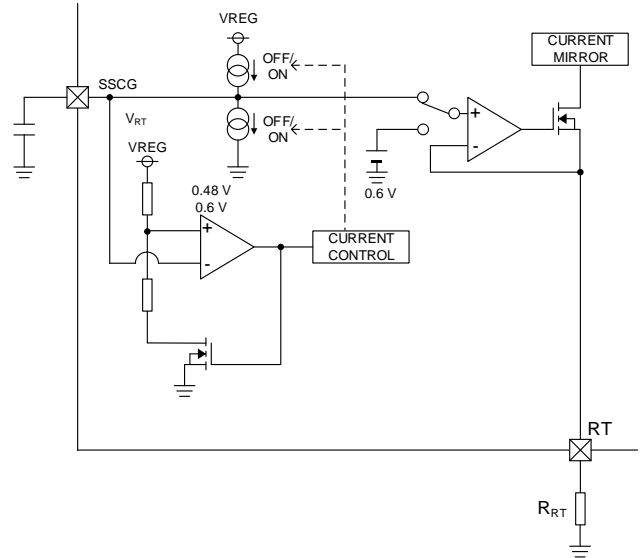


Figure 6. SSCG System Diagram

f_{SSCG} can be calculated by the following equation.

$$f_{SSCG} = \frac{3}{4 \times C_{SSCG} \times R_{RT}} \text{ [Hz]}$$

Set it to satisfy the equation of $0.4 \text{ kHz} \leq f_{SSCG} \leq 30 \text{ kHz}$.

Furthermore, quantity of noise reduction S [dB] in SSCG can be roughly estimated by the equation below.

$$S = -10 \times \log \left(\frac{f_{SSCG}}{f_{OSC} \times 0.9 \times 0.2} \right) \text{ [dB]}$$

Short the SSCG pin and the GND pin when SSCG function is not used.

(5) External Synchronization Oscillation Frequency

By clock signal input to the SYNC pin, the internal oscillation frequency can be synchronized externally. Do not switch from external to internal oscillation if the DC/DC switching is active. The clock input to the SYNC pin is valid only in rising edge. Input the external input frequency within $\pm 20\%$ of internal oscillatory frequency set by the RT pin resistance.

(6) Soft Start Function (SS)

The soft-start (SS) function can start the output voltage slowly while controlling the current during the start by connecting the capacitance (C_{SS}) to the SS pin. In this way, output voltage overshoot and inrush current can be prevented. When SS function is not used, set the SS pin open. Refer to [10. Setting of Soft Start Time](#) for the calculation of SS time.

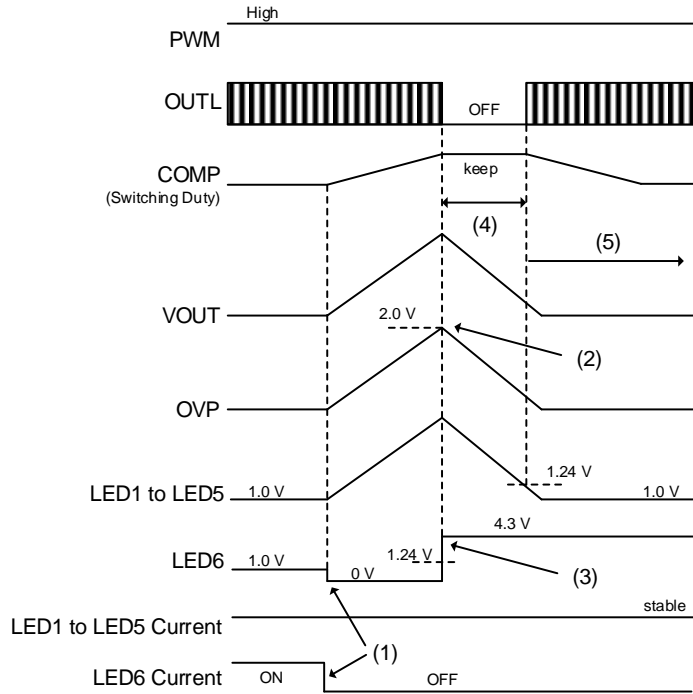
(7) Maximum Duty

When DC/DC switching reaches Maximum Duty, expected VOUT voltage could be not output, and LED lights-out might occur by the reduction of LED output current and detection of ground short protection. Set input condition and load condition such that it does not reach Maximum Duty.

3. Buck-Boost DC/DC Controller - continued

(8) DC/DC Switching Control at Over Voltage Output (LSDET)

When the lowest voltage in LED1 to LED6 pin (DC/DC feedback voltage) is more than 1.24 V, LSDET function works and turns off the switching of the DC/DC converter and maintains the COMP voltage (switching Duty). This function reduces the VOUT voltage quickly and intended to output stable switching Duty when VOUT is higher than the aim voltage. For example, LSDET works at the time of the LED OPEN detection. The timing chart example is described below.



(1) LED6 is OPEN and LED6 current does not flow, LED6 pin voltage is 0 V.

(2) VOUT is increase because of LED6 pin voltage is 0 V. Therefore OVP rises to 2.0 V, and LED6 becomes the OPEN detection state.

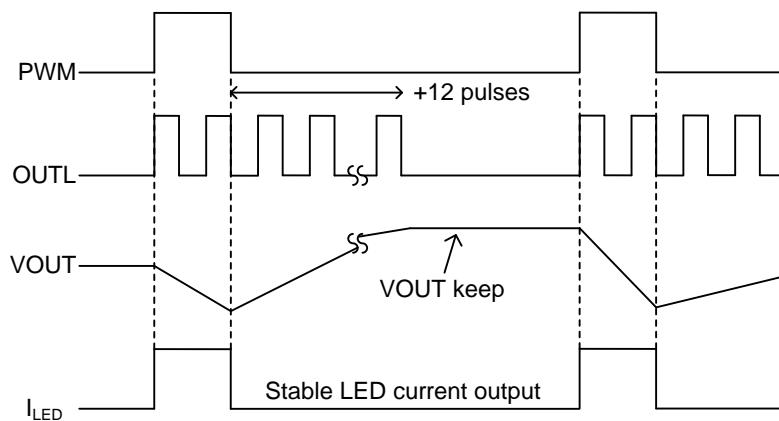
(3) LED6 pin voltage pulls up to 4.3 V in the IC by the OPEN detection.

(4) Because LED1 to LED6 pin becomes more than 1.24 V, LSDET function works. DCDC switching is OFF and COMP pin voltage is kept by LSDET function. VOUT is decrease because DC/DC switching is OFF.

(5) LED1 to LED5 pin voltages decrease with a drop of VOUT. And LSDET function is released when any of them is 1.24 V or less. DC/DC switching is turned on again and COMP pin voltage is controlled to appropriate duty.

(9) PWM Pulse and DC/DC Switching

After the fall of the PWM pulse, DC/DC switching is output 12 times and after that, turn off the DC/DC switching during PWM=Low. When PWM becomes High again, the DC/DC switching is on. Because of this, when PWM pulse width is short, it can maintain the output voltage and output the stable LED current.

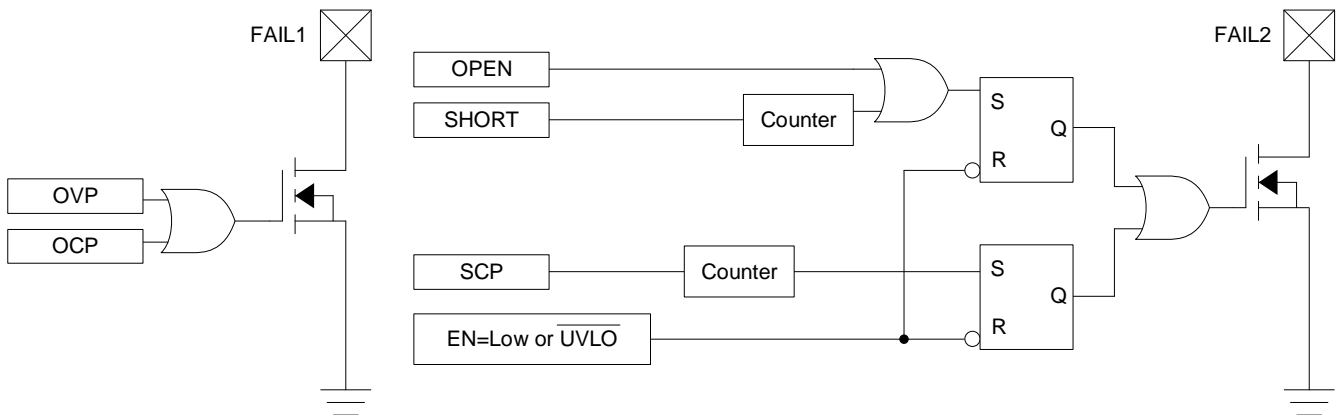


Description of Blocks - continued

4. Protection Feature

Table 2. Detect Condition of Each Protection Feature and Operation During Detection

Function	Detect Condition		Operation During Detection
	[Detection]	[Release/Cancellation]	
UVLO	$V_{CC} \leq 3.5 \text{ V}$ or $V_{VREG} \leq 2.0 \text{ V}$	$V_{CC} \geq 4.0 \text{ V}$ and $V_{VREG} \geq 3.5 \text{ V}$	All blocks shut down except VREG
TSD	$T_a \geq 175 \text{ }^\circ\text{C}$	$T_a \leq 150 \text{ }^\circ\text{C}$	All blocks shut down except VREG
OVP	$V_{OVP} \geq 2.0 \text{ V}$	$V_{OVP} \leq 1.94 \text{ V}$	DC/DC switching OFF
OCP	$V_{CS} \leq V_{CC} - 0.2 \text{ V}$	$V_{CS} > V_{CC} - 0.2 \text{ V}$	DC/DC switching OFF
SCP	$V_{OVP} \leq 0.57 \text{ V}$ or Any of V_{LED1} to V_{LED6} is 0.3 V or less (100 ms delay @300 kHz)	EN Reset or UVLO Reset	After SCP delay time, all blocks latch OFF except VREG
LED Open Protection	Any of V_{LED1} to V_{LED6} is 0.3 V or less and $V_{OVP} \geq 2.0 \text{ V}$	EN Reset or UVLO Reset	Only detected channel LED current latches OFF
LED Short Protection	Any of V_{LED1} to V_{LED6} is 4.5 V or more (100 ms delay @300 kHz)	EN Reset or UVLO Reset	After LED Short delay time, only detected channel LED current latches OFF



Protection Flag Output Block Diagram

FAIL1 becomes low when OVP or OCP protection is detected, whereas FAIL2 becomes low when SCP, LED open or LED short is detected. If the FAIL1, FAIL2 pin is not used as a flag output, set the FAIL1, FAIL2 pin open or connect it to GND. The output from the FAIL1 and FAIL2 pins are reset and return to High by starting up of EN or release of UVLO. Also, those output is unstable when EN=Low and detecting UVLO. If the FAIL pin is used as a flag output, it is recommended to pull-up the FAIL1, FAIL2 pins to the VREG pin. The recommended value of pull-up resistance is 100 kΩ.

4. Protection Feature - continued

- (1) Under-Voltage Lock Out (UVLO)
The UVLO shuts down DC/DC converter and Current Driver when $V_{CC} \leq 3.5 \text{ V}$ or $V_{VREG} \leq 2.0 \text{ V}$. And UVLO is released by $V_{CC} \geq 4.0 \text{ V}$ and $V_{VREG} \geq 3.5 \text{ V}$.
- (2) Thermal Shutdown (TSD)
The TSD shuts down DC/DC converter and Current Driver when the T_j 175 °C or more, and releases when the T_j becomes 150 °C or less.
- (3) Over Voltage Protection (OVP)
The output voltage of DC/DC converter is detected from the OVP pin voltage, and the over voltage protection is activate if the OVP pin voltage becomes $\geq 2.0 \text{ V}$. When OVP is activated, the switching operation of the DC/DC converter turns off. And the OVP pin voltage becomes $\leq 1.94 \text{ V}$, OVP is released and the switching operation of the DC/DC converter turns on.
- (4) Over Current Protection (OCP)
The OCP detects the coil current by monitoring the voltage of the high side resistor, and activates when $V_{CS} \leq V_{CC} - 0.2 \text{ V}$. When the OCP is activated, the switching operation of the DC/DC converter turns off. And $V_{CS} > V_{CC} - 0.2 \text{ V}$, OCP is released and the switching operation of the DC/DC converter turns on.
- (5) Short Circuit Protection (SCP)
The SCP can be operated when the SS pin voltage reaches 3.3 V while start-up. When any of the LED1 to LED6 pin voltage becomes 0.3 V or less or $V_{OVP} \leq 0.57 \text{ V}$, the built-in counter operation starts. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT} . After it counts 32770, the DC/DC converter and the current driver are latched off. When $f_{osc} = 300 \text{ kHz}$, the count time is 100 ms and SCP operates after this count time. If all of the LED pin voltage becomes more than 0.3 V or $V_{OVP} \geq 1.0 \text{ V}$ before 32770 count, the counter resets and SCP is not detected.
- (6) LED Open Protection
When any of the LED pins voltage is 0.3 V or less and $V_{OVP} 2.0 \text{ V}$ or more, LED open is detected and latches off the open LED channel only.
- (7) LED Short Protection
If any of V_{LED1} to V_{LED6} is 4.5 V or more, the built-in counter operation starts. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT} . After it counts 32770, latches off the short LED channel only. When $f_{osc} = 300 \text{ kHz}$, the count time is 100 ms and SCP operates after this count time. During PWM dimming, the LED Short Protection is carried out only when PWM=High. If the condition of LED Short is reset while working the counter, the counter resets and LED Short is not detected.
- (8) PWM Low Interval Detect
The low interval of PWM input is counted by built-in counter during EN=High. The clock frequency of counter is the oscillation frequency (f_{OSC}), which is determined by R_{RT} . It stops the operation of circuits except VREG at 32768 counts. When $f_{osc} = 300 \text{ kHz}$, the count time is 100 ms and the Low interval of PWM is detected after this count time.

4. Protection Feature - continued

(9) Output Voltage Discharge Circuit (VOUT Discharge Function)

If start-up with a charge remaining at VOUT, LED might occur flicker. To prevent this, it is necessary to discharge of VOUT when starting-up. If use only resistance for setting OVP to discharge, it takes a lot time for discharging VOUT. Therefore, this product has functionality of circuit for VOUT discharge. VOUT discharge function is available at Buck-Boost application and Buck application. For this case, be sure to connect VOUT and the VDISC pin. It discharges the residual electric charge of VOUT when DC/DC circuit is OFF; changing EN High to Low or operating protect function. The discharge time (t_{DISC}) is expressed in the following equations.

$$t_{DISC} = \frac{3 \times V_{OUT} \times C_{OUT}}{4 \times I_{DISC}} \quad [s]$$

where:

t_{DISC} is the DC/DC converter output discharge time.

C_{OUT} is the VOUT capacity.

V_{OUT} is the DC/DC converter output voltage.

I_{DISC} is the discharge current.

From the graph below, find the I_{DISC} value in 25 % VOUT voltage, and substitute it in the above equation. For example, substitute I_{DISC} value in VOUT=5 V (approximately 76 mA) in the above equation when using in VOUT=20 V, and calculate the discharge time.

In order to suppress the flickering of the LED, the time of restarting EN=Low should be secured t_{DISC} or more long. Always check with actual machine because the t_{DISC} found here is a reference level.

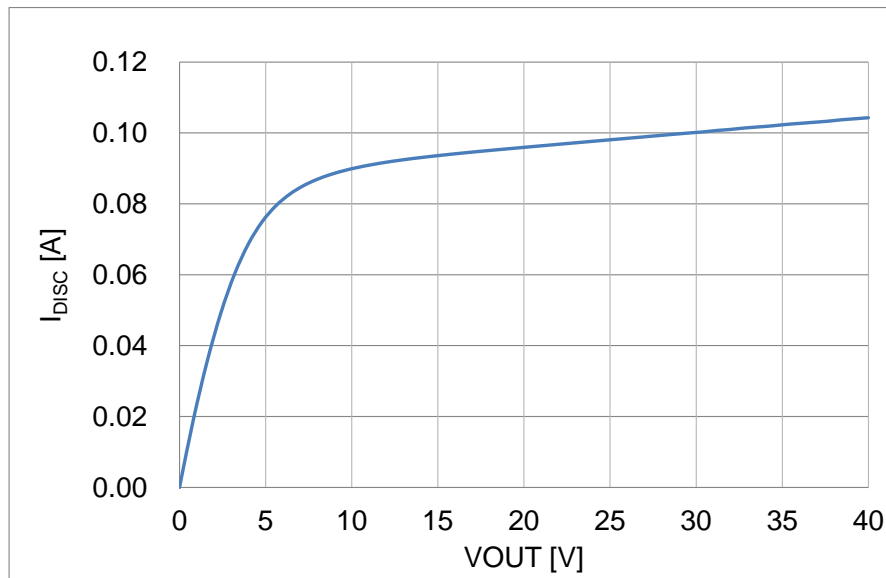


Figure 7. I_{DISC} vs VOUT

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCC	40	V
BOOT, OUTH Pin Voltage	V _{BOOT} , V _{OUTH}	45	V
SW, CS, Pin Voltage	V _{SW} , V _{CS}	40	V
BOOT-SW Pin Voltage	V _{BOOT-SW}	7	V
LED1 to LED6, VDISC Pin Voltage	V _{LED1} , V _{LED2} , V _{LED3} , V _{LED4} , V _{LED5} , V _{LED6} , V _{DISC}	40	V
PWM, SYNC, EN Pin Voltage	V _{PWM} , V _{SYNC} , V _{EN}	-0.3 ~ +7	V
VREG, OVP, FAIL1, FAIL2, SS, RT, SSCG Pin Voltage	V _{VREG} , V _{OVP} , V _{FAIL1} , V _{FAIL2} , V _{SS} , V _{RT} , V _{SSCG}	-0.3 ~ +7 < VCC	V
LEDEN1, LEDEN2, ISET, OUTL, COMP, Pin Voltage	V _{LEDEN1} , V _{LEDEN2} , V _{ISET} V _{OUTL} , V _{COMP}	-0.3 ~ +7 < V _{VREG}	V
Maximum Junction Temperature	T _{jmax}	150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
LED Maximum Output Current	I _{LED}	120 ^(Note 1)	mA

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB board with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Current level per channel. Set the LED current that does not over Junction Temperature Range (T_j) maximum.

Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
HTSSOP-B30				
Junction to Ambient	θ _{JA}	72.72	24.45	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	5.27	3.75	°C/W

(Note 2) Based on JESD51-2A(Still-Air), using a BD81A76EFV-M Chip.

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt
Top		
Copper Pattern	Thickness	
Footprints and Traces	70 μm	

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 6)		
			Pitch	Diameter	
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm	
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ^(Note 1)	VCC	4.5	12	35	V
Operating Temperature	Topr	-40	+25	+125	°C
DC/DC Oscillation Frequency	f _{OSC}	200	300	2200	kHz
External Synchronized Frequency ^{(Note 2)(Note 3)}	f _{SYNC}	200 or higher of f _{OSC} x 0.8	300	2200 or lower of f _{OSC} x 1.2	kHz
External Synchronized Pulse Duty	D _{SYNC}	40	50	60	%

(Note 1) This indicates the voltage near the VCC pin. Be careful of voltage drop by the impedance of power line.

(Note 2) When external synchronization frequency is not used, connect the SYNC pin to open or GND.

(Note 3) When external synchronization frequency is used, do not change to internal oscillation frequency along the way.

Operating Conditions (External Constant Range)

Parameter	Symbol	Min	Typ	Max	Unit
VREG Capacity	C _{VREG}	1.0	2.2	4.7	μF
LED Current Setting Resistance	R _{ISSET}	41	100	250	kΩ
Oscillation Frequency Setting Resistance	R _{RT}	3.6	27	41	kΩ
Soft Start Capacity Setting	C _{SS}	0.047	0.1	0.47	μF
Spread Spectrum Setting Capacity	C _{SSCG}	4.7	10	47	nF

Electrical Characteristics

(Unless otherwise specified, VCC=12 V, Ta=-40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current	I _{CC}	-	-	10	mA	EN=High, SYNC=High, RT=OPEN, PWM=Low, ISET=OPEN, CIN=10 μF
Standby Current	I _{ST}	-	-	10	μA	EN=Low, VDISC=OPEN
[VREG]						
Reference Voltage	V _{VREG}	4.5	5.0	5.5	V	I _{VREG} =-5 mA, C _{VREG} =2.2 μF
[OUTH]						
OUTH High Side ON-Resistor	R _{ONHH}	1.5	3.5	7.0	Ω	I _{OUTH} =-10 mA
OUTH Low Side ON-Resistor	R _{ONHL}	0.8	2.5	5.5	Ω	I _{OUTH} =10 mA
OCP Detection Voltage	V _{OLIMIT}	VCC-0.22	VCC-0.20	VCC-0.18	V	
OCP Detection Mask Time	t _{OLIMIT}	-	30	-	ns	V _{CS} =VCC-0.5V
[OUTL]						
OUTL High Side ON-Resistor	R _{ONLH}	1.5	3.5	10.0	Ω	I _{OUTL} =-10 mA
OUTL Low Side ON-Resistor	R _{ONLL}	0.8	2.5	5.5	Ω	I _{OUTL} =10 mA
[SW]						
SW ON-Resistor	R _{ON_SW}	4.0	10.0	25.0	Ω	I _{SW} =10 mA
[ERRAMP]						
LED Control Voltage	V _{LED}	0.9	1.0	1.1	V	
COMP Sink Current	I _{COMPSINK}	35	80	145	μA	V _{LEDn} =2 V (n=1, 2, 3, 4, 5, 6), V _{COMP} =1 V
COMP Source Current	I _{COMPSOURCE}	-145	-80	-35	μA	V _{LEDn} =0.5 V (n=1, 2, 3, 4, 5, 6), V _{COMP} =1 V
[Oscillator]						
Oscillation Frequency 1	f _{OSC1}	285	300	315	kHz	R _{RT} =27 kΩ
Oscillation Frequency 2	f _{OSC2}	1800	2000	2200	kHz	R _{RT} =3.6 kΩ
[OVP]						
OVP Detection Voltage	V _{OVP1}	1.9	2.0	2.1	V	V _{OVP} : Sweep up
OVP Hysteresis Width	V _{OVPHYS1}	0.02	0.06	0.10	V	V _{OVP} : Sweep down

Electrical Characteristics - continued

(Unless otherwise specified, VCC=12 V, Ta=-40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[UVLO]						
UVLO Detection Voltage	V _{UVLO}	3.2	3.5	3.8	V	VCC: Sweep down
UVLO Hysteresis Width	V _{UHYS}	0.25	0.50	0.75	V	VCC: Sweep up, V _{VREG} > 3.5 V
[LED Output]						
LED Current Relative Dispersion	I _{LED1}	-3	-	+3	%	I _{LED} =50 mA, Ta=25 °C $\Delta I_{LED1} = (I_{LEDn}/I_{LEDn_AVG}-1) \times 100$ (n = 1, 2, 3, 4, 5, 6)
		-5	-	+5	%	I _{LED} =50 mA, Ta=-40 °C to +125 °C $\Delta I_{LED1} = (I_{LEDn}/I_{LEDn_AVG}-1) \times 100$ (n=1, 2, 3, 4, 5, 6)
LED Current Absolute Dispersion	I _{LED2}	-3	-	+3	%	I _{LED} =50 mA, Ta=25 °C $\Delta I_{LED2} = (I_{LEDn}/50mA-1) \times 100$ (n=1, 2, 3, 4, 5, 6)
		-5	-	+5	%	I _{LED} =50 mA, Ta=-40 °C to +125 °C $\Delta I_{LED2} = (I_{LEDn}/50mA-1) \times 100$ (n=1, 2, 3, 4, 5, 6)
ISET Voltage	V _{ISET}	0.9	1.0	1.1	V	R _{ISET} =100 kΩ
PWM Minimum Pulse Width	t _{MIN}	1	-	-	μs	f _{PWM} =100 Hz to 20 kHz, I _{LED} =20 mA to 100 mA
PWM Frequency	f _{PWM}	0.1	-	20	kHz	
[Protection Circuit]						
LED Open Detection Voltage	V _{OPEN}	0.2	0.3	0.4	V	V _{LED1} , V _{LED2} , V _{LED3} , V _{LED4} , V _{LED5} , V _{LED6} : Sweep down
LED Short Detection Voltage	V _{SHORT}	4.2	4.5	4.8	V	V _{LED1} , V _{LED2} , V _{LED3} , V _{LED4} , V _{LED5} , V _{LED6} : Sweep up
LED Short Detection Latch OFF Delay Time	t _{SHORT}	70	100	130	ms	R _{RT} =27 kΩ
SCP Latch OFF Delay Time	t _{SCP}	70	100	130	ms	R _{RT} =27 kΩ
PWM Latch OFF Delay Time	t _{PWM}	70	100	130	ms	R _{RT} =27 kΩ
ISET-GND Short Protection Impedance	I _{SETPROT}	-	-	4.7	kΩ	
LSDET Detection Voltage	V _{LSDET}	-	1.24	-	V	
[Logic Input Voltage]						
Input High Voltage	V _{INH}	2.1	-	V _{VREG}	V	EN, SYNC, PWM, LEDEN1, LEDEN2
Input Low Voltage	V _{INL}	GND	-	0.8	V	EN, SYNC, PWM, LEDEN1, LEDEN2
Input Current	I _{IN}	15	50	100	μA	V _{IN} =5 V (EN, SYNC, PWM, LEDEN1, LEDEN2)
[FAIL Output (Open Drain)]						
FAIL Low Voltage	V _{OL}	-	0.1	0.2	V	I _{FAIL} =0.1 mA

Typical Performance Curves

(Reference Data. Unless otherwise specified, $T_a = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$)

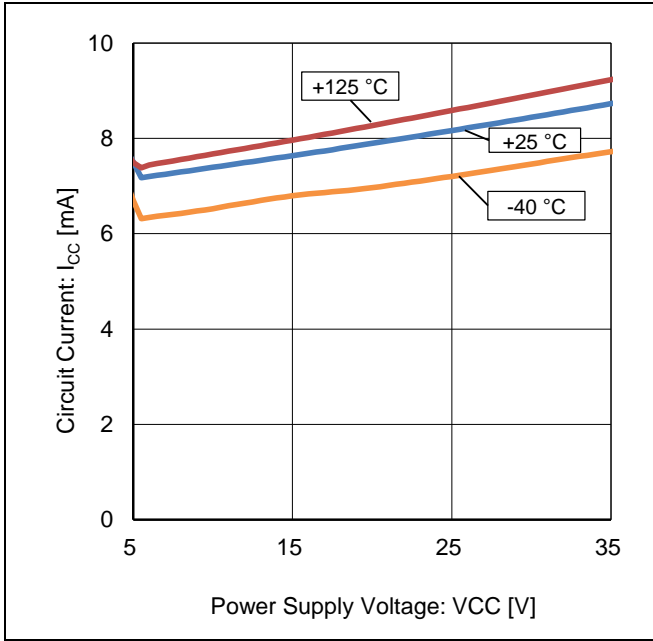


Figure 8. Circuit Current vs Power Supply Voltage
($V_{CC}=5\text{ V}$ to 35 V , $V_{EN}=3.3\text{ V}$, $V_{PWM}=0\text{ V}$)

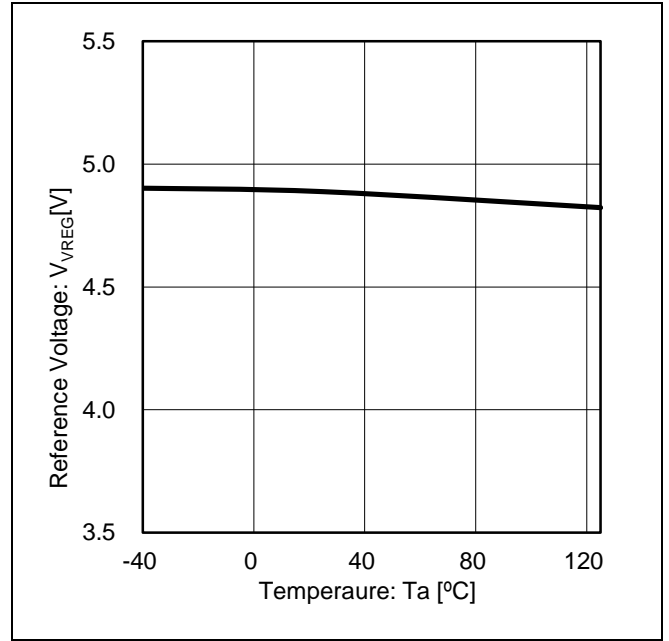


Figure 9. Reference Voltage vs Temperature
($V_{CC}=12\text{ V}$, $V_{EN}=3.3\text{ V}$, $V_{PWM}=0\text{ V}$)

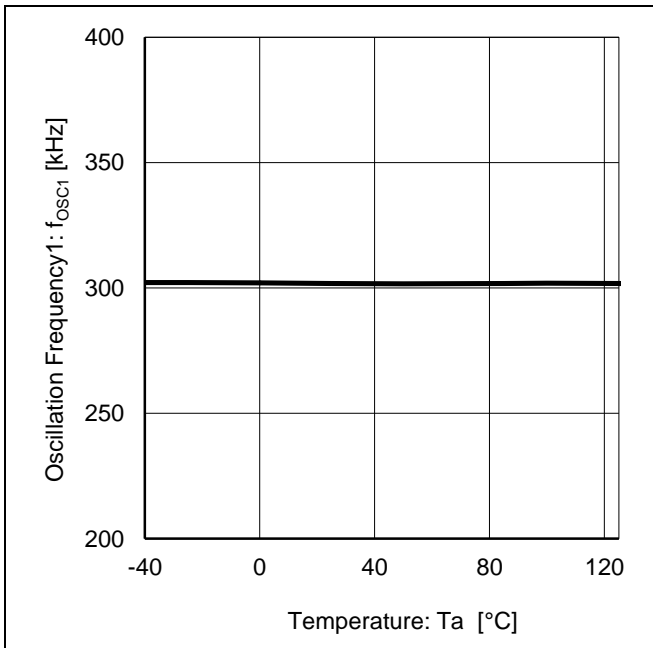


Figure 10. Oscillation Frequency1 vs Temperature
(@300 kHz, $V_{CC}=12\text{ V}$, $V_{EN}=3.3\text{ V}$, $R_{RT}=27\text{ k}\Omega$)

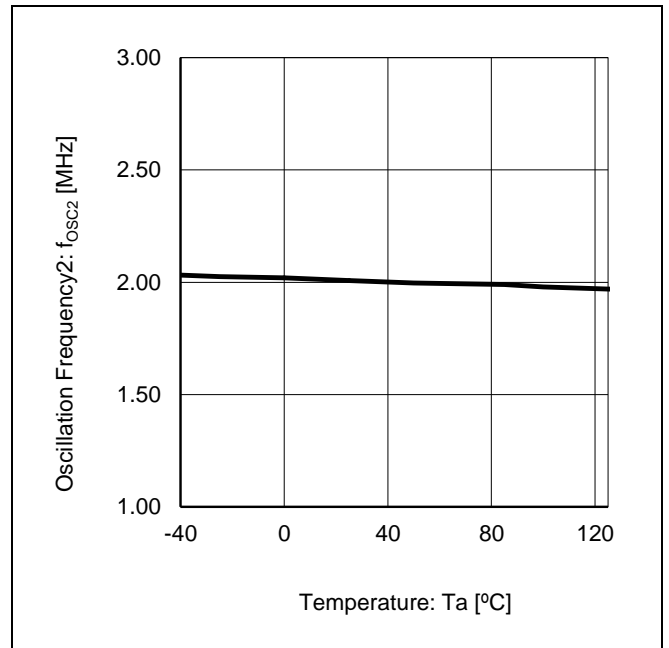


Figure 11. Oscillation Frequency2 vs Temperature
(@2000 kHz, $V_{CC}=12\text{ V}$, $V_{EN}=3.3\text{ V}$, $R_{RT}=3.6\text{ k}\Omega$)

Typical Performance Curves - continued

(Reference Data. Unless otherwise specified, Ta=-40 °C to +125 °C)

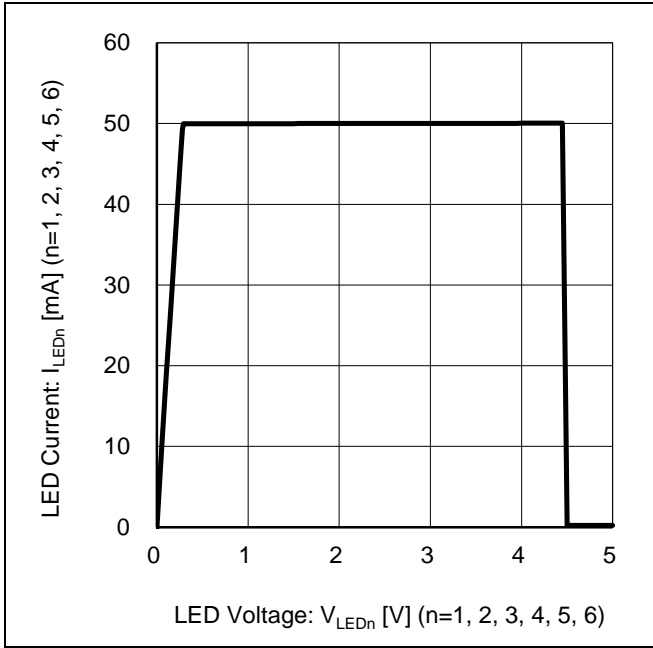


Figure 12. LED Current vs LED Voltage
(Ta=25 °C, VCC=12 V, VEN=3.3 V, VLEDn=sweep)

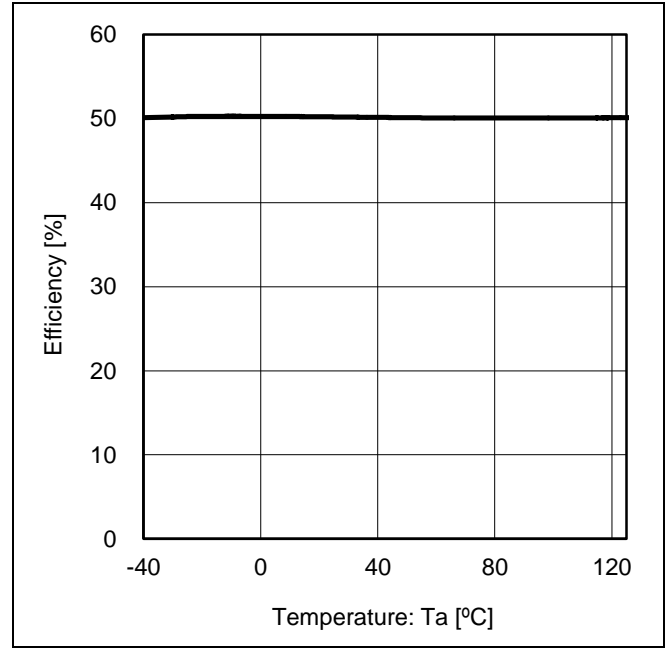


Figure 13. Efficiency vs Temperature
(VCC=12 V, VEN=3.3 V, VLEDn=2 V (n=1, 2, 3, 4, 5, 6)
VPWM=VREG)

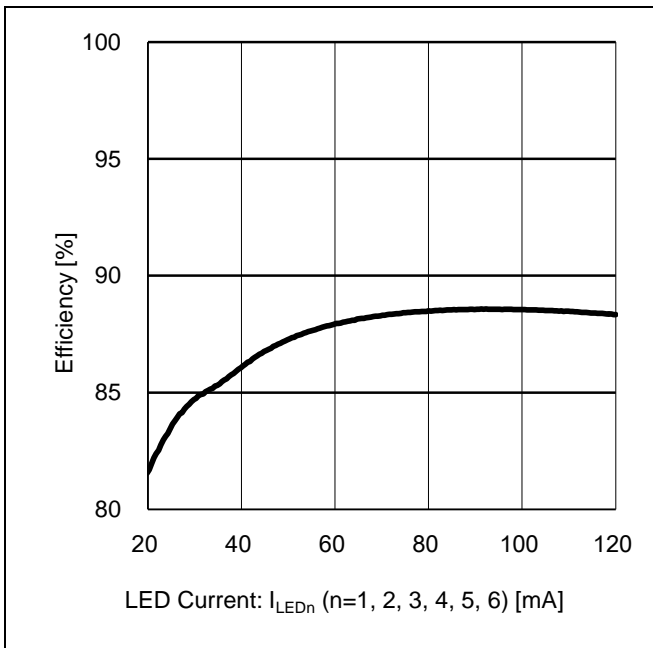


Figure 14. Efficiency vs LED Current
(Buck-Boost application)
(Ta=25 °C, VCC=12 V, VEN=3.3 V, VPWM=VREG,
LED4 Series 6ch)

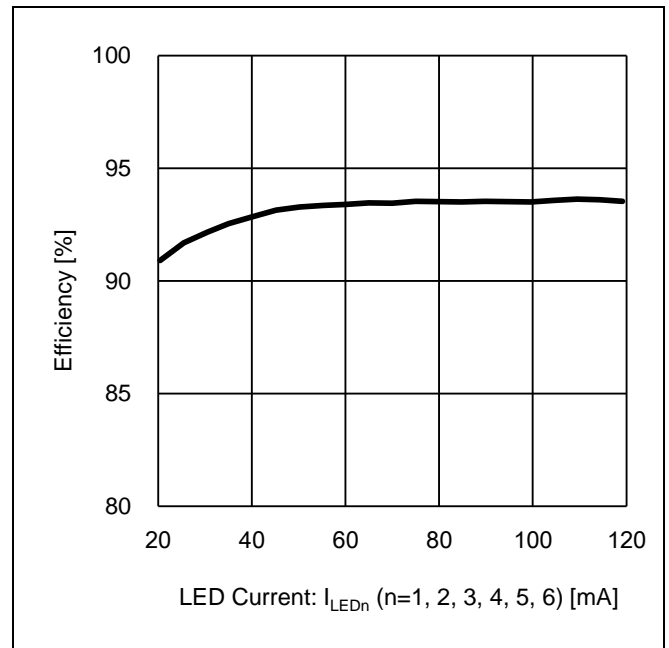
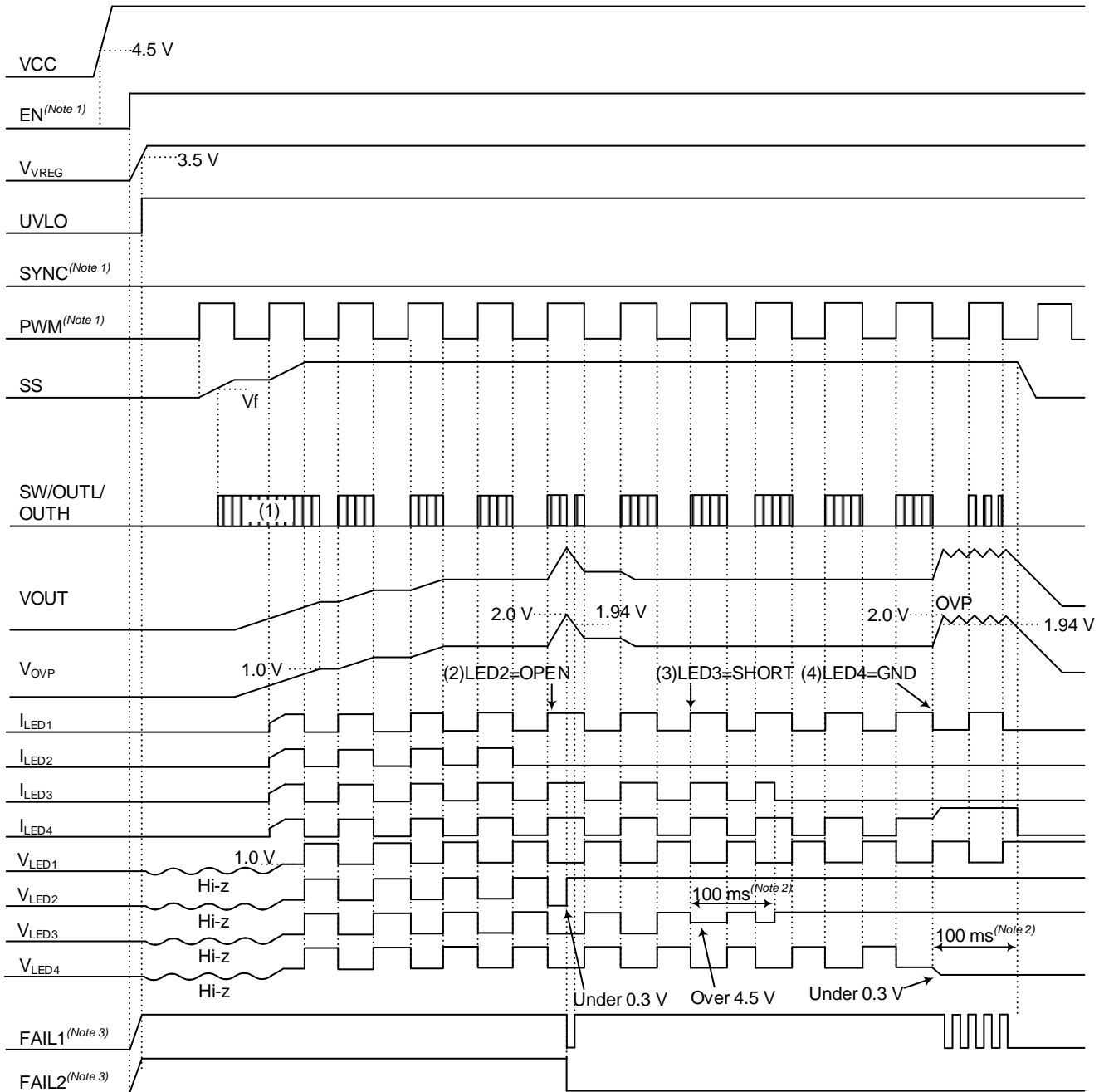


Figure 15. Efficiency vs LED Current
(Boost application)
(Ta=25 °C, VCC=12 V, VEN=3.3 V, VPWM=VREG,
LED8 Series 6ch)

Timing Chart (Start-up and Protection)



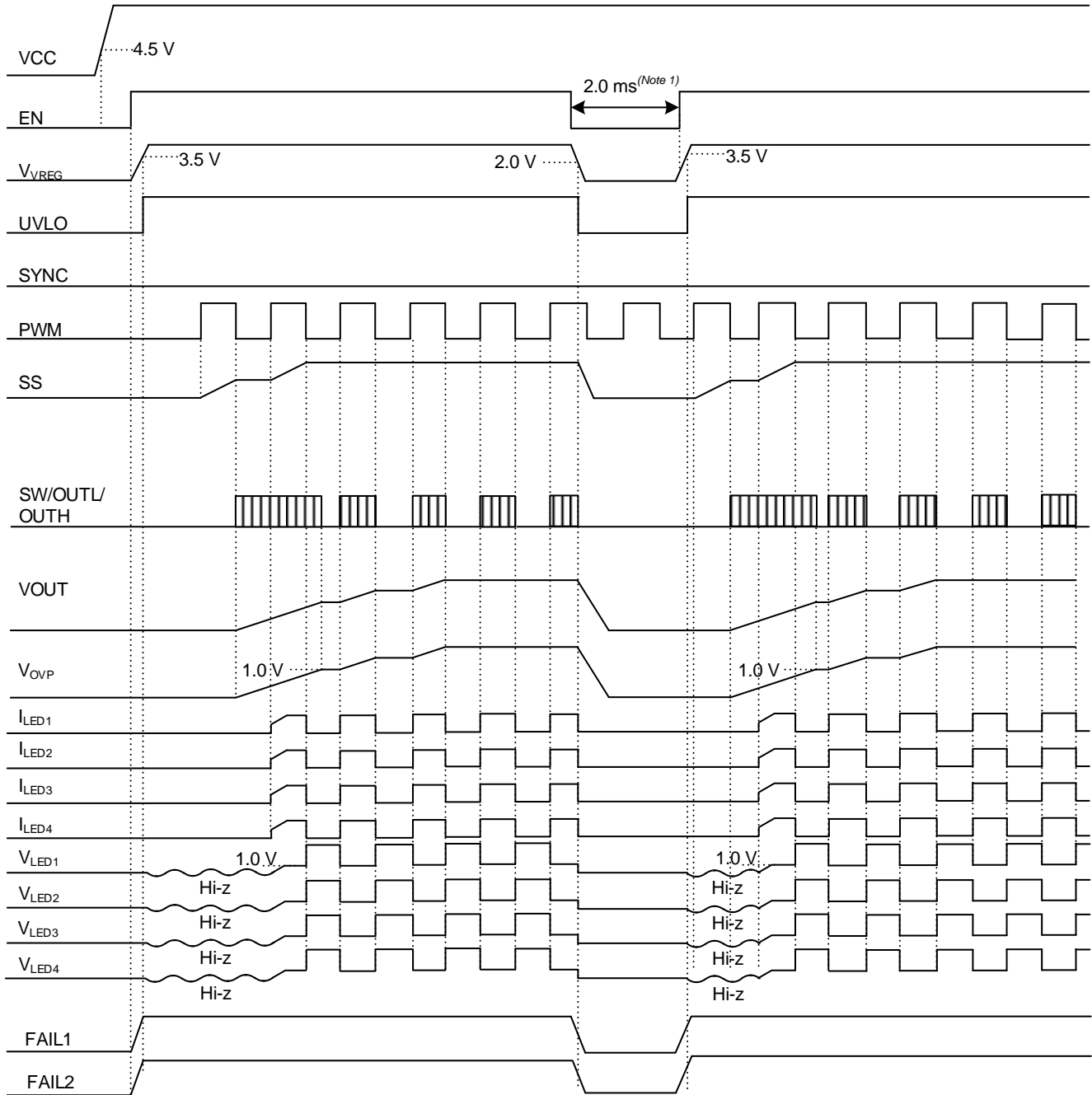
(Note 1) EN is input after input VCC in the timing chart above, but there is no problem to input EN, PWM, and SYNC before input VCC. EN is judged as Low at V_{EN} is 0.8 V or less and as High at V_{EN} is 2.1 V or more. Do not use this IC in the condition of V_{EN} is between 0.8 V and 2.1 V.

(Note 2) The count time of $32770 \text{ clk} \times 1/f_{OSC}$. In case of $f_{osc}=300 \text{ kHz}$, the count time is 100 ms.

(Note 3) The above timing chart is when the FAIL1 and FAIL2 pin are pulled up to the VREG pin.

- (1) When V_{OVp} is less than 1.0 V, regardless of PWM input, the DC/DC switching operation is active (Pre-Boost function). And if V_{OVp} reaches 1.0 V, the Pre-Boost is finished. Only when PWM is activated, switches to the Normal mode which operates the DC/DC switching.
- (2) When V_{LED2} is 0.3 V or less and V_{OVp} is 2.0 V or more, LED Open Protect is active and LED2 is turned OFF. Then FAIL2 becomes Low.
- (3) If the condition of V_{LED3} is 4.5 V or more and passes 100 ms ($@f_{osc}=300 \text{ kHz}$), LED3 is turned OFF. Then FAIL2 becomes Low.
- (4) When V_{LED4} is shorted to GND, increase the VOUT voltage. Then V_{OVp} rises 2.0 V or more and detect OVP. FAIL1 becomes Low. If OVP occurs, DC/DC switching is OFF and decrease the VOUT voltage, then OVP repeats ON/OFF. And DC/DC switching and LED current of each channel is turned OFF after 100 ms by detecting ground short protection. (In case of $f_{osc}=300 \text{ kHz}$).

Timing Chart (Start-up and EN Restart)



(Note 1) The Low section during EN restart requires 2.0 ms or more.

Restart after VOUT voltage is discharged. VOUT discharge function or external discharge switch is recommended (Refer to 4. Protection Feature (9) [Output Voltage Discharge Circuit \(VOUT discharge function\)](#)). If EN is restarted with remaining VOUT voltage, LED flickering might occur.

Application Examples

When using as Boost DC/DC converter

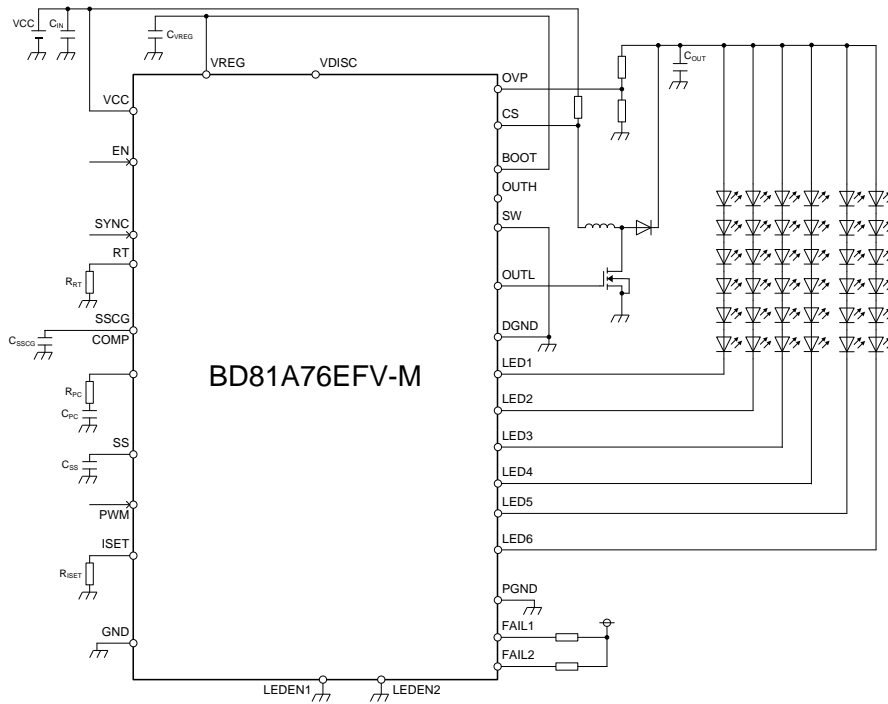


Figure 16. Boost Application Circuit

If the VOUT and LED pin are shorted in this case, the over current from V_{IN} cannot be prevented. To prevent over current, carry out measure such as inserting fuse of which value is OCP setting value or more and is part's rating current or less in between VCC and R_{CS} .

When using as Buck DC/DC Converter

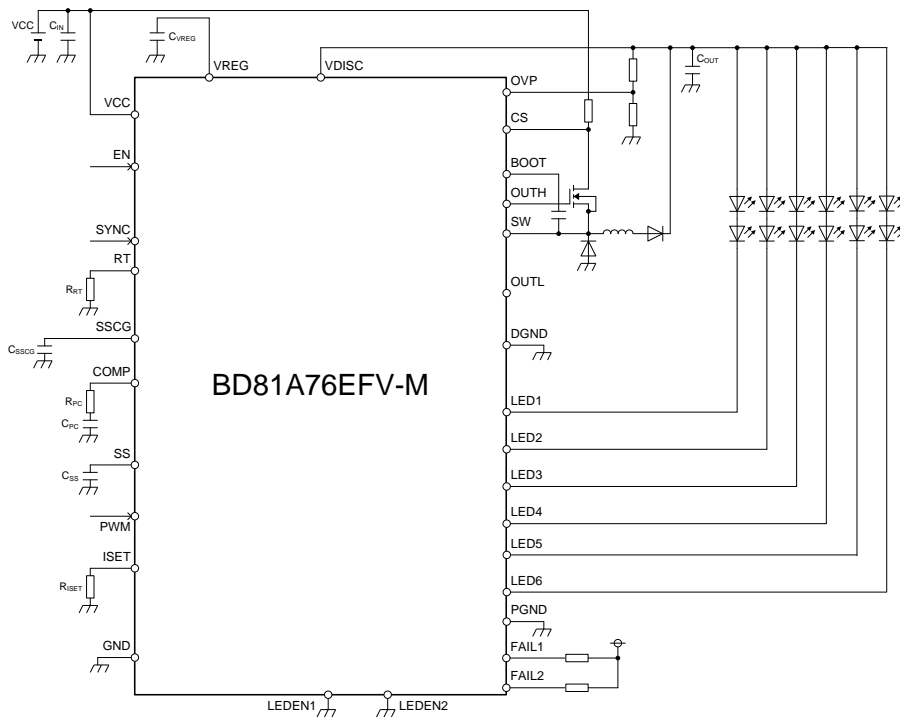


Figure 17. Buck Application Circuit

PCB Application Circuit

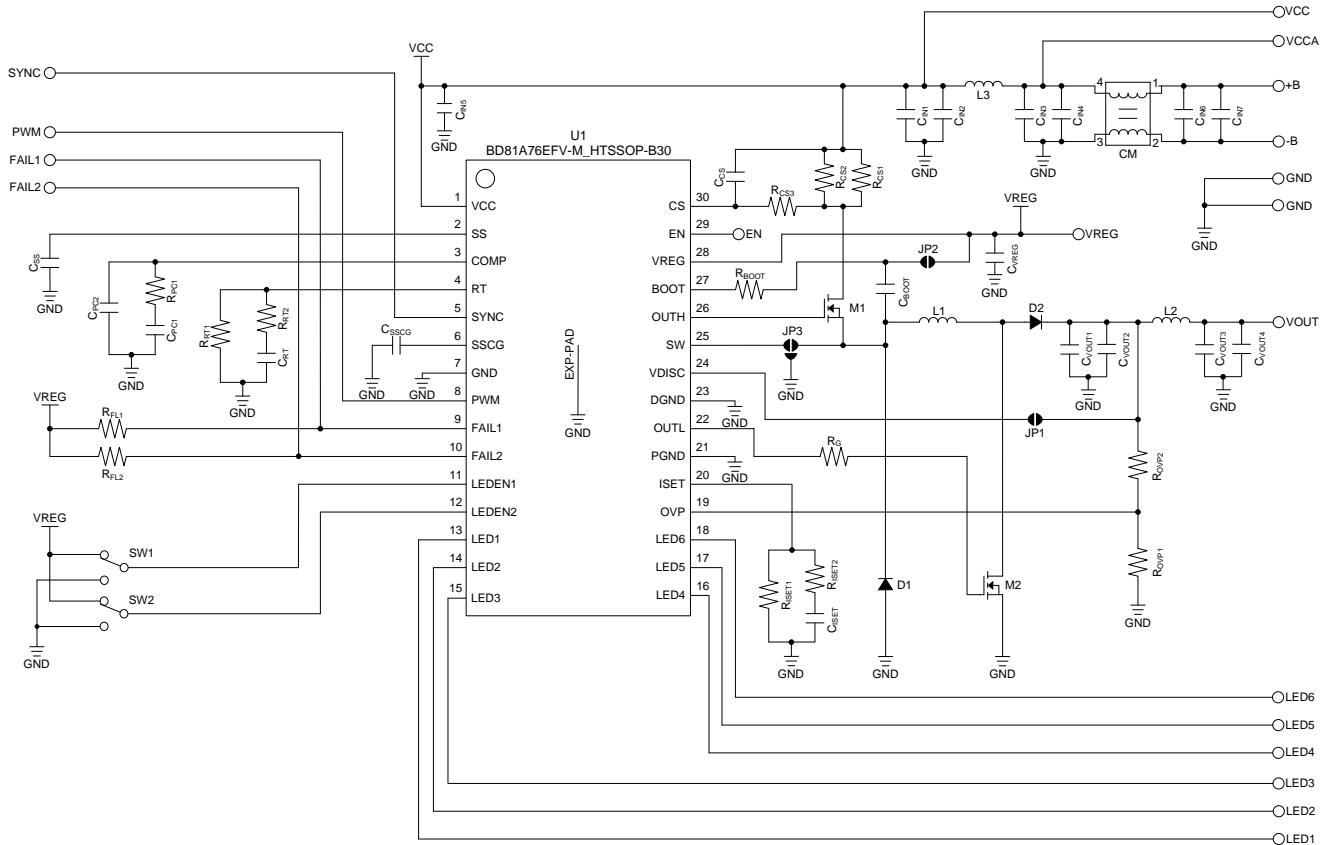


Figure 18. PCB Application Circuit

- Arrange R_{RT} resistor near the RT pin and do not attach capacitor.
- Arrange R_{ISET} resistor near the ISET pin and do not attach capacitor.
- Attach the decoupling capacitor of C_{IN} and C_{VREG} to IC pin as close as possible.
- Keep the impedance low because large current might flow into DGND and PGND.
- Be careful not to occur noise in the ISET, RT, and COMP pins.
- Since PWM, OUTH, OUTL, SW, SYNC and LED1 to LED6 have switching, avoid affecting the surrounding patterns.
- The SW, OUTH, BOOT pin to each components, keep shortest wiring and minimum impedance.
- There is thermal PAD at the back of package. Solder the board GND for thermal PAD.
- Set the gate resistor of FET (M1) to 0 Ω . If resistor is connected, M1 OFF timing is delayed in M1 parasitic capacity and gate resistor, and the penetrating current flows to the internal transistor of M1 and SW. The penetrating current might worsen the efficiency or detect OCP.
- To reduce noise, consider the board layout in the shortest wiring and minimum impedance for Boost loop ($D2 \rightarrow C_{VOUT} \rightarrow DGND \rightarrow M2 \rightarrow D2$) and Buck loop ($VCC \rightarrow R_{CS} \rightarrow M1 \rightarrow D1 \rightarrow DGND \rightarrow GND \rightarrow C_{IN} \rightarrow VCC$).
- The ringing of Low-side FET can be suppressed by R_G , but there is a concern that efficiency might worsen when R_G increases. When using R_G , decide the resistance value after full evaluation.
- Wire both ends of R_{CS1} and R_{CS2} (Red line of below figure) most shortly. If a wiring is long, it may lead to false detection of OCP by an inductance.

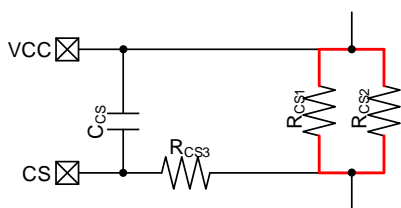


Figure 19. The Case of R_{CS} Parallel

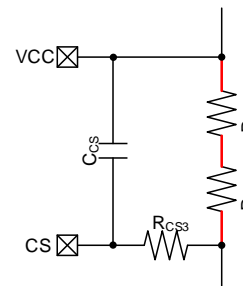


Figure 20. The case of R_{CS} Series

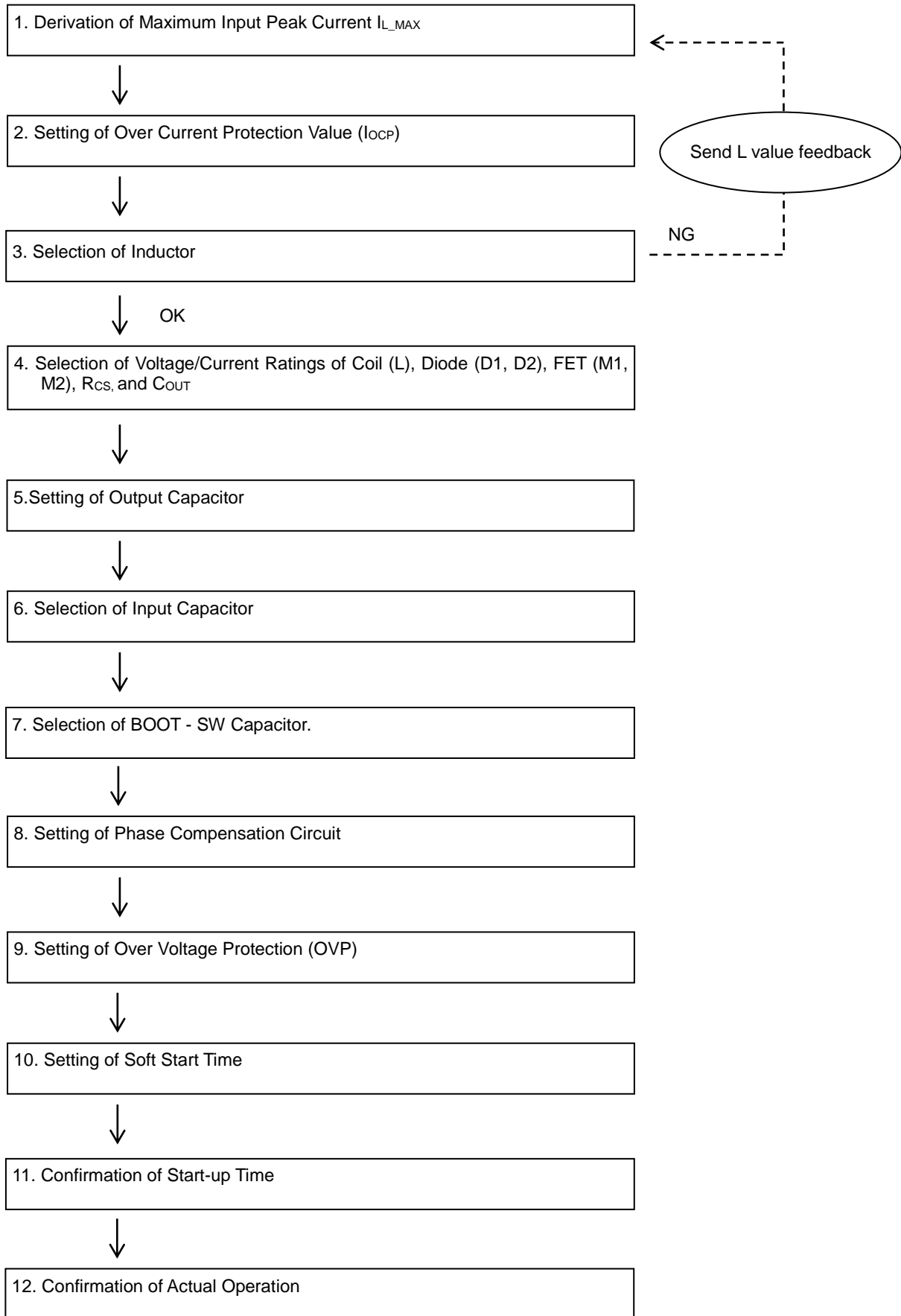
PCB Board External Components List (Buck Boost Application)

Serial No.	Component Name	Component Value	Product Name	Manufacturer
1	C _{IN1}	10 μ F	GCM32EC71H106KA03	murata
2	C _{IN2}	-	-	-
3	C _{IN3}	-	-	-
4	C _{IN4}	-	-	-
5	C _{IN5}	0.1 μ F	GCM155R71H104KE37	murata
6	C _{IN6}	-	-	-
7	C _{IN7}	-	-	-
8	CM	-	-	-
9	L3	-	-	-
10	R _{CS1}	150 m Ω	MCR100JZHFL0R15	Rohm
11	R _{CS2}	150 m Ω	MCR100JZHFL0R15	Rohm
12	R _{CS3}	Short	-	-
13	C _{CS}	-	-	-
14	C _{SS}	0.1 μ F	GCM155R11C104JA40	murata
15	C _{PC1}	0.01 μ F	GCM155R71H103KA40	murata
16	R _{PC1}	5.1 k Ω	MCR03EZPJ512	Rohm
17	C _{PC2}	-	-	-
18	R _{RT1}	27 k Ω	MCR03EZPD2702	Rohm
19	R _{RT2}	-	-	-
20	C _{RT}	-	-	-
21	C _{SSCG}	0.01 μ F	GCM155R71H103KA40	murata
22	R _{FL1}	100 k Ω	MCR03EZPJ104	Rohm
23	R _{FL2}	100 k Ω	MCR03EZPJ104	Rohm
24	C _{VREG}	2.2 μ F	GCM188C71A225KE01	murata
25	C _{BOOT}	0.1 μ F	GCM155R11C104JA40	murata
26	R _{BOOT}	Short	-	-
27	L1	22 μ H	CLF10060NIT-220M-D	TDK
28	M1	-	RSS070N05FRA	Rohm
29	M2	-	RSS070N05FRA	Rohm
30	D1	-	RBR3LAM40BTF	Rohm
31	D2	-	RBR3LAM40BTF	Rohm
32	L2	Short	-	-
33	C _{VOUT1}	10 μ F	GCM32EC71H106KA03	murata
34	C _{VOUT2}	10 μ F	GCM32EC71H106KA03	murata
35	C _{VOUT3}	10 μ F	GCM32EC71H106KA03	murata
36	C _{VOUT4}	10 μ F	GCM32EC71H106KA03	murata
37	R _{OVP1}	20 k Ω	MCR03EZPD2002	Rohm
38	R _{OVP2}	360 k Ω	MCR03EZPD3603	Rohm
39	R _{ISSET1}	100 k Ω	MCR03EZPJ104	Rohm
40	R _{ISSET2}	-	-	-
41	C _{ISSET}	-	-	-
42	R _G	0 Ω	-	-
43	JP1	Short	-	-
44	JP2	Open	-	-
45	JP3	Short	(SW-L1 short)	-

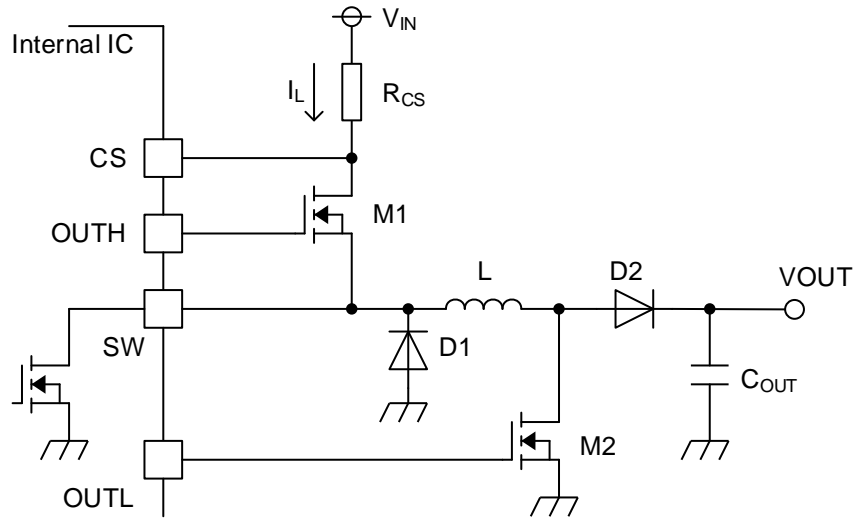
* The above components are modified according to operating conditions and load to be used.

Selection of Components Externally Connected

Select the external components following the steps below.



Selection of Components Externally Connected - continued

1. Derivation of Maximum Input Peak Current I_{L_MAX} 

Output Application Circuit Diagram (Buck-Boost Application)

- (1) Maximum Output Voltage (V_{OUT_MAX}) Computation
Consider the V_f variation and number of LED connection in series for V_{OUT_MAX} derivation

$$V_{OUT_MAX} = (V_f + \Delta V_f) \times N + 1.1$$

where:

V_{OUT_MAX} is the Maximum output voltage.

V_f is the LED V_f voltage.

ΔV_f is the LED V_f voltage variation.

N is the LED series number.

- (2) Maximum Output Current I_{OUT_MAX} Computation

$$I_{OUT_MAX} = I_{LED} \times 1.05 \times M$$

where:

I_{OUT_MAX} is the Max output current.

I_{LED} is the Output current per channel.

M is the LED parallel number.

- (3) Maximum Input Peak Current I_{L_MAX} Computation

$$I_{L_MAX} = I_{L_AVG} + \frac{1}{2} \Delta I_L$$

where:

I_{L_MAX} is the Maximum input current.

I_{L_AVG} is the Maximum Input average current.

ΔI_L is the coil current amplification.

(In case of Boost Application)

$$I_{L_AVG} = V_{OUT_MAX} \times \frac{I_{OUT_MAX}}{\eta \times V_{CC}}$$

$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{1}{f_{OSC}} \times \frac{V_{OUT_MAX} - V_{CC}}{V_{OUT_MAX}}$$

1. Derivation of Maximum Input Peak Current I_{L_MAX} - continued

(In case of Buck-Boost application)

$$I_{L_AVG} = (VCC + VOUT_MAX) \times \frac{I_{OUT_MAX}}{\eta \times VCC}$$

$$\Delta I_L = \frac{VCC}{L} \times \frac{1}{f_{OSC}} \times \frac{VOUT_MAX}{VCC + VOUT_MAX}$$

(In case of Buck application)

$$I_{L_AVG} = I_{OUT_MAX} / \eta$$

$$\Delta I_L = \frac{VOUT}{L} \times \frac{1}{f_{OSC}} \times \frac{VCC - VOUT_MAX}{VCC}$$

where:

VCC is the supply voltage.

η is the efficiency.

f_{OSC} is the DC/DC oscillation frequency.

L is the coil value.

- The worst case for V_{IN} is minimum, so the minimum value should be applied in the equation.
- BD81A76EFV-M adopts the current mode DC/DC converter control and is appropriately designed for coil value. The abovementioned value is recommended according to efficiency and stability. If choose the L values outside this recommended range, it not to be guaranteed the stable continuous operation. For example, it may cause irregular switching waveform.
- η (efficiency) is around 80 %.

2. Setting of Over Current Protection Value (I_{OCP})

$$I_{OCP} = \frac{V_{OCP_MIN}}{R_{CS}} > I_{L_MAX} \quad [A]$$

where:

I_{OCP_MIN} is the over current protection detect voltage.

V_{OCP_MIN} is the over current protection detect voltage (0.18 V).

R_{CS} is the current detect resistance.

I_{L_MAX} is the maximum input peak current.

R_{CS} should be selected by the above equation.

3. Selection of Inductor

In order to achieve stable operation of the current mode DC/DC converter, it is recommended adjusting the L value within the range indicated below.

$$0.05 < \frac{VOUT \times R_{CS}}{L \times 10^6} < \frac{0.63 \times f_{OSC}}{10^6} \quad [V/\mu s]$$

where:

$VOUT$ is the DC/DC converter output voltage.

R_{CS} is the current detect resistance.

L is the coil value.

f_{OSC} is the DC/DC oscillation frequency.

Consider the deviation of L value and set with enough margins.

It is more stable by reducing the value of $\frac{VOUT \times R_{CS}}{L \times 10^6}$, however it slows down the response time.

3. Selection of Inductor - continued

Also, the following equation should be satisfied during coil selection in case it is used in VCC=5 V or less.

$$L < \frac{12 \times VCC \times VCC \times \eta}{VOUT \times I_{LED} \times M \times f_{OSC}}$$

where:

L is the coil value.

VCC is the supply voltage.

η is the efficiency.

$VOUT$ is the DC/DC converter output voltage.

I_{LED} is the LED current per channel.

f_{OSC} is the DC/DC oscillation frequency.

M is the LED parallel number.

LED intensity may drop when a coil which does not satisfy the above is chosen.

4. Selection of Voltage/Current Ratings of Coil (L), Diode (D1, D2), FET (M1, M2), Rcs, and COUT

	Current Rating	Voltage Rating	Heat Loss
Coil L	> I_{L_MAX}	-	-
Diode D1	> I_{OCP}	> VCC_MAX	-
Diode D2	> I_{OCP}	> V_{OVP_MAX}	-
FET M1	> I_{OCP}	> VCC_MAX	-
FET M2	> I_{OCP}	> V_{OVP_MAX}	-
Rcs	-	-	> $I_{OCP}^2 \times R_{CS}$
COUT	-	> V_{OVP_MAX}	-

Consider deviation of external parts and set with enough margins.

In order to achieve fast switching, choose the FET's with smaller gate-capacitance.

5. Setting of Output Capacitor

Select the output capacitor C_{OUT} based on the requirements of the ripple voltage $VOUT_{pp}$.

$$VOUT_{pp} = \frac{20 \times I_{LED} \times M}{f_{OSC} \times C_{VOUT} \times \eta} + \Delta I_L \times R_{ESR} \quad [V]$$

where:

$VOUT_{pp}$ is the VOUT ripple voltage.

I_{LED} is the LED current per channel.

M is the LED parallel number.

f_{OSC} is the DC/DC oscillation frequency.

C_{VOUT} is the VOUT capacity.

η is the efficiency.

ΔI_L is the coil current amplification.

R_{ESR} is the equivalent series resistance of output capacitor C_{OUT} .

The actual VOUT ripple voltage is affected by PCB layout and external components characteristics. Therefore, check with the actual machine, and design a capacity with enough margins to fit in allowable ripple voltage.

The maximum value of C_{OUT} that can be set is 500 μF .

6. Selection of Input Capacitor

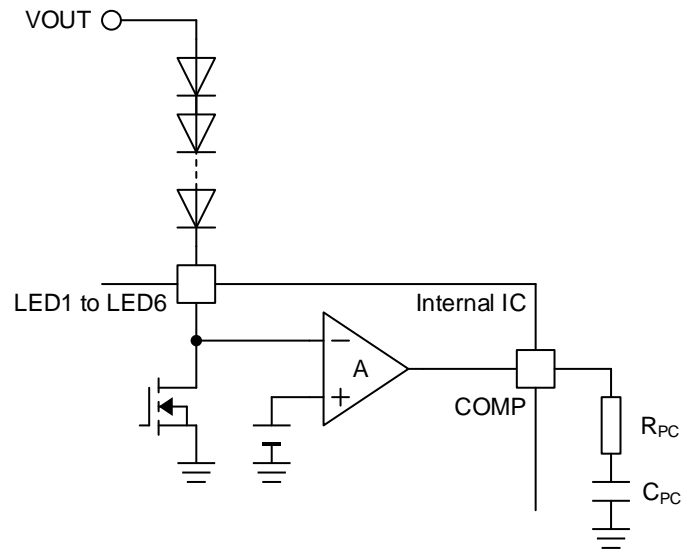
An input capacitor which is 10 μF or more with low ESR ceramic capacitor is recommended. An input capacitor which is not recommended may cause large ripple voltage at the input and hence lead to malfunction of the IC.

7. Selection of BOOT - SW Capacitor

When using the Buck-Boost application or Buck application, insert 0.1 μF capacitor between the BOOT pin and the SW pin.

Selection of Components Externally Connected - continued

8. Setting of Phase Compensation Circuit



COMP Pin Application Schematic

Stability Condition of Application

The stability in LED voltage feedback system is achieved when the following conditions are met.

- (1) When gain is 1 (0 dB), the phase delay is 150 °C or less (or simply, phase margin is 30 °C or more).
- (2) When gain is 1 (0 dB), the frequency (Unity Gain Frequency) is 1/10 or less of switching frequency.

To assure stability based on phase margin adjustment is setting the Phase-lead f_z close to unity gain frequency. In addition, the Phase-lag f_{p1} is decided based on C_{OUT} and output impedance R_L .

The respective formulas are as follows.

$$\text{Phase-lead} \quad f_z = 1/(2\pi R_{PC} C_{PC}) \quad [\text{Hz}]$$

$$\text{Phase-lag} \quad f_{p1} = 1/(2\pi R_L C_{OUT}) \quad [\text{Hz}]$$

* The output impedance that is calculated in $R_L = V_{OUT}/I_{OUT}$

To make a good result, set f_z between 1 kHz to 10 kHz. Substitute the value in the maximum load for R_L .

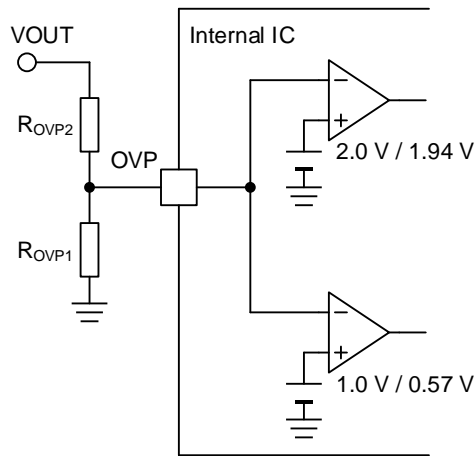
Further, this setting is easily obtained, and the adjustment with the actual machine may be necessary because it is not strictly calculated. In case of mass production design, thorough confirmation with the actual machine is necessary because these characteristics can change based on board layout, load condition and etc.

Selection of Components Externally Connected - continued

9. Setting of Over Voltage Protection (OVP)

Over voltage protection (OVP) is set from the external resistance R_{OVP} , R_{OVP2} .

The setting described below is important in the either boost, buck and buck-boost applications.



OVP Application Circuit

The OVP pin detects the over voltage when it is 2.0 V (Typ) or more and stops the DC/DC switching. In addition, it detects the open condition when the OVP pin is at 2.0 V (Typ) or more and LED1 to LED6 pin voltage is at 0.3 V (Typ) or less, and the circuit is latched to OFF (Refer to Description of Blocks 4. Protection Feature [\(6\) LED Open Protection](#)). In preventing the error in detection of OPEN, it is necessary that the resistor divide voltage shall be less than the minimum value of OPEN detection voltage. Set the R_{OVP1} , R_{OVP2} in such a way the formula shown below can be met.

$$V_{OUT}(Max) \times \frac{R_{OVP1}}{(R_{OVP1} + R_{OVP2})} < V_{OVPOpen}(Min) \dots (1)$$

where:

V_{OUT} is the DC/DC output voltage.

$V_{OVPOpen}$ is the OVP pin open detection voltage.

Example 1: When $V_f = 3.2 \text{ V} \pm 0.3 \text{ V}$ LED is used in 8 series

$$V_{OUT}(Max) = 1.1(\text{LED control voltage Max}) + (3.2 + 0.3) \times 8 = 29.1 \text{ [V]}$$

$$\text{Open Detection OVP Pin Voltage } V_{OVPOpen}(Min) = 1.9 \text{ [V]}$$

If $R_{OVP1} = 20 \text{ k}\Omega$, set by $R_{OVP2} > 286.3 \text{ k}\Omega$ from (1).

Example 2: When $V_f = 3.2 \text{ V} \pm 0.3 \text{ V}$ LED is used in 3 series

$$V_{OUT}(Max) = 1.1(\text{LED control voltage Max}) + (3.2 + 0.3) \times 3 = 11.6 \text{ [V]}$$

$$\text{Open Detection OVP Pin Voltage } V_{OVPOpen}(Min) = 1.9 \text{ [V]}$$

If $R_{OVP1} = 20 \text{ k}\Omega$, set by $R_{OVP2} > 102.1 \text{ k}\Omega$ from (1).

10. Setting of Soft Start Time

The soft start circuit is necessary to prevent increase of the coil current and overshoot of the output during the start-up. A capacitance in the range of 0.047 μF to 0.47 μF is recommended. A capacitance less than 0.047 μF may cause overshoot at the output voltage. On the other hand, a capacitance more than 0.47 μF may cause massive reverse current through the parasitic elements when power supply is OFF and may damage the IC.

Soft start time t_{SS} (Typ).

$$t_{SS} = C_{SS} \times 3.3 / (5 \times 10^{-6}) \text{ [s]}$$

where:

C_{SS} is the Capacitance at SS pin.

Selection of Components Externally Connected - continued

11. Confirmation of Start-up Time

If the PWM duty is smaller at start-up, the start-up time becomes longer. It is effective to reduce the C_{PC} value to shorten start-up time, however, confirmation of the phase margin is necessary. PWM duty and data of start-up time in typical 2 conditions are shown below.

Condition 1 (Boost)

$V_{CC}=12\text{ V}$, $V_{OUT}=30\text{ V}$ (assume LED8 series), $R_{RT}=27\text{ k}\Omega$ ($f_{OSC}=300\text{ kHz}$), $R_{ISET}=100\text{ k}\Omega$ ($I_{LED}=50\text{ mA}$), $C_{PC}=0.01\text{ }\mu\text{F}$, $R_{PC}=5.1\text{ k}\Omega$, $C_{SS}=0.1\text{ }\mu\text{F}$, $R_{OVP1}=20\text{ k}\Omega$, $R_{OVP2}=360\text{ k}\Omega$

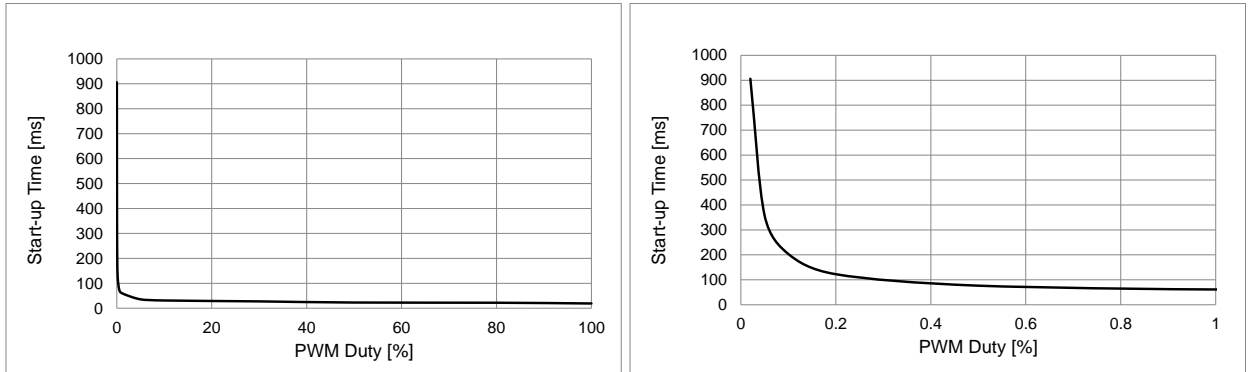


Figure 21. Start-up Time (Boost) vs PWM Duty

Condition 2 (Buck-Boost)

$V_{CC}=12\text{ V}$, $V_{OUT}=20\text{ V}$ (assume LED5 series), $R_{RT}=27\text{ k}\Omega$ ($f_{OSC}=300\text{ kHz}$), $R_{ISET}=100\text{ k}\Omega$ ($I_{LED}=50\text{ mA}$), $C_{PC}=0.01\text{ }\mu\text{F}$, $R_{PC}=5.1\text{ k}\Omega$, $C_{SS}=0.1\text{ }\mu\text{F}$, $R_{OVP1}=30\text{ k}\Omega$, $R_{OVP2}=360\text{ k}\Omega$

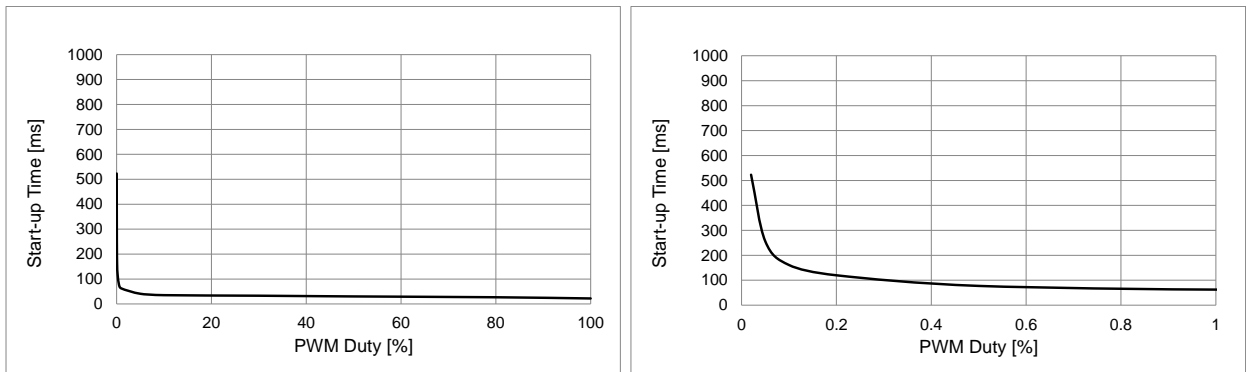


Figure 22. Start-up Time (Buck-Boost) vs PWM Duty

The above are reference data. Always confirm by machine operation because the actual start-up time depends on layout pattern, component constant, and component characteristics.

Selection of Components Externally Connected - continued

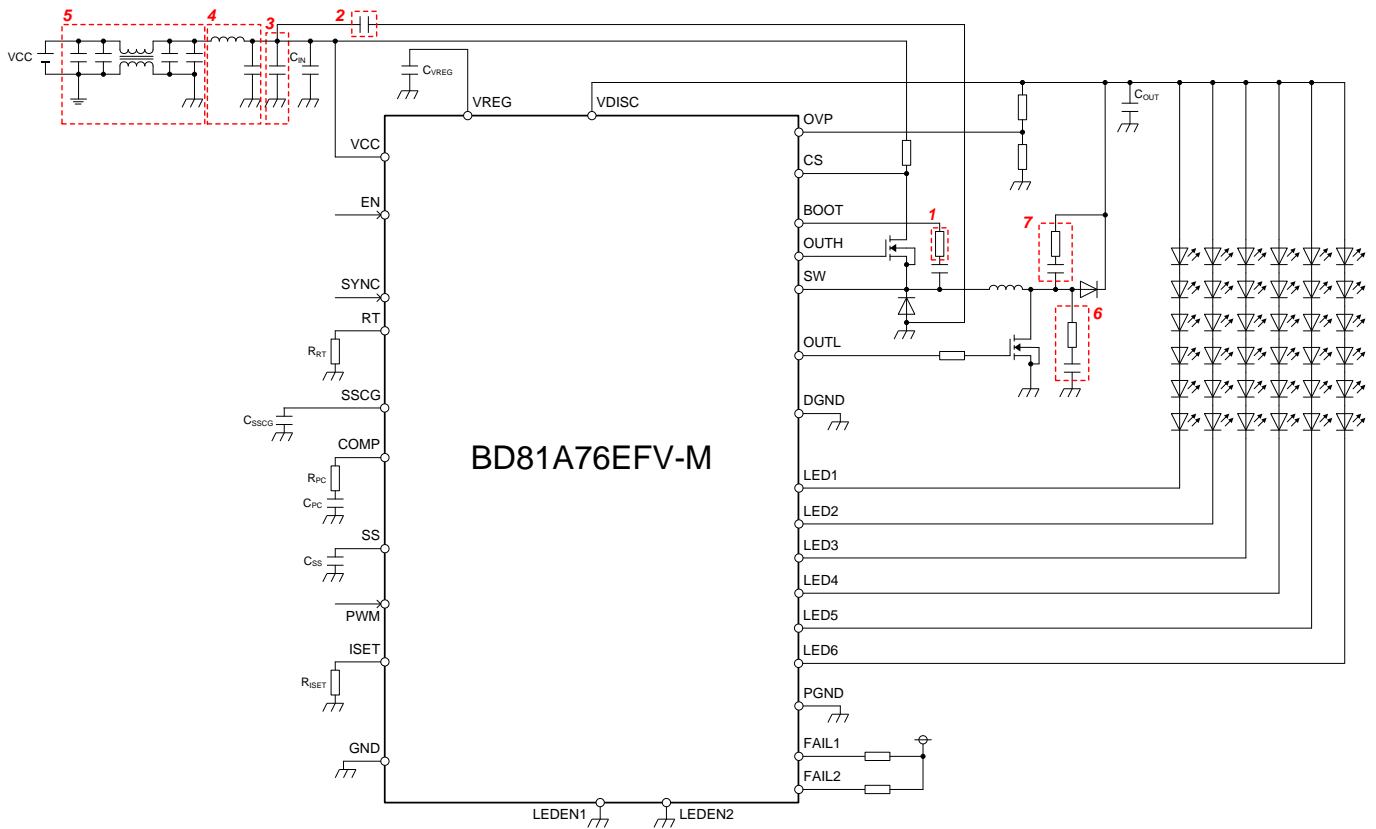
12. Confirmation of Actual Operation

Set up the external components value by procedures and attentions mentioned above. However, those settings above are not guaranteed because these are theoretically calculated and it does not include the external parts' variation or characteristics changing. The overall characteristics may change depend on power supply voltage, LED current, LED number, inductance, output capacitance, switching frequency, and PCB layout. We strongly recommend verifying your design by taking the actual measurements.

Additional parts for EMC

The example of EMC countermeasure components is shown in the chart below.

1. The resistance for adjusting Slew Rate of high side FET
2. The capacitor for reducing current loop noise of high side FET.
3. The capacitor for reducing noise of high frequency on power line.
4. The low pass filter for reducing noise of power line.
5. The common mode filter for reducing noise of power line.
6. The snubber circuit for reducing noise of high frequency of low side FET.
7. The snubber circuit for reducing ringing of low side FET switching.



Application Circuit Reference Example (Including EMC Countermeasure Components)

Precautions on PCB Layout

The layout pattern greatly affects the efficiency and ripple characteristics. Therefore, it is necessary to examine carefully when designing. As show in the figure on right, Buck-Boost DC/DC converter has two loops; “Loop1” and “Loop2”. The parts in each loop have to be set as near as possible to each other. (For example, GND of C_{OUT} and DGND should be very near, GND of C_{IN} and GND of D1 should be very near and so on.)

Moreover, the wirings of each loop should be as low impedance as possible.

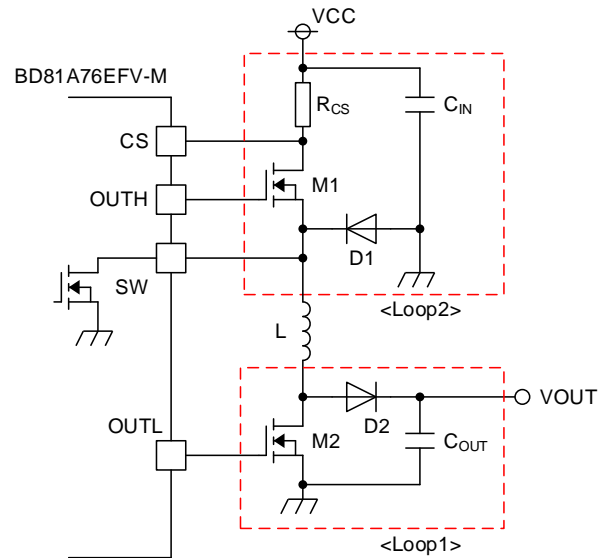


Figure 23. Circuit of DC/DC Block

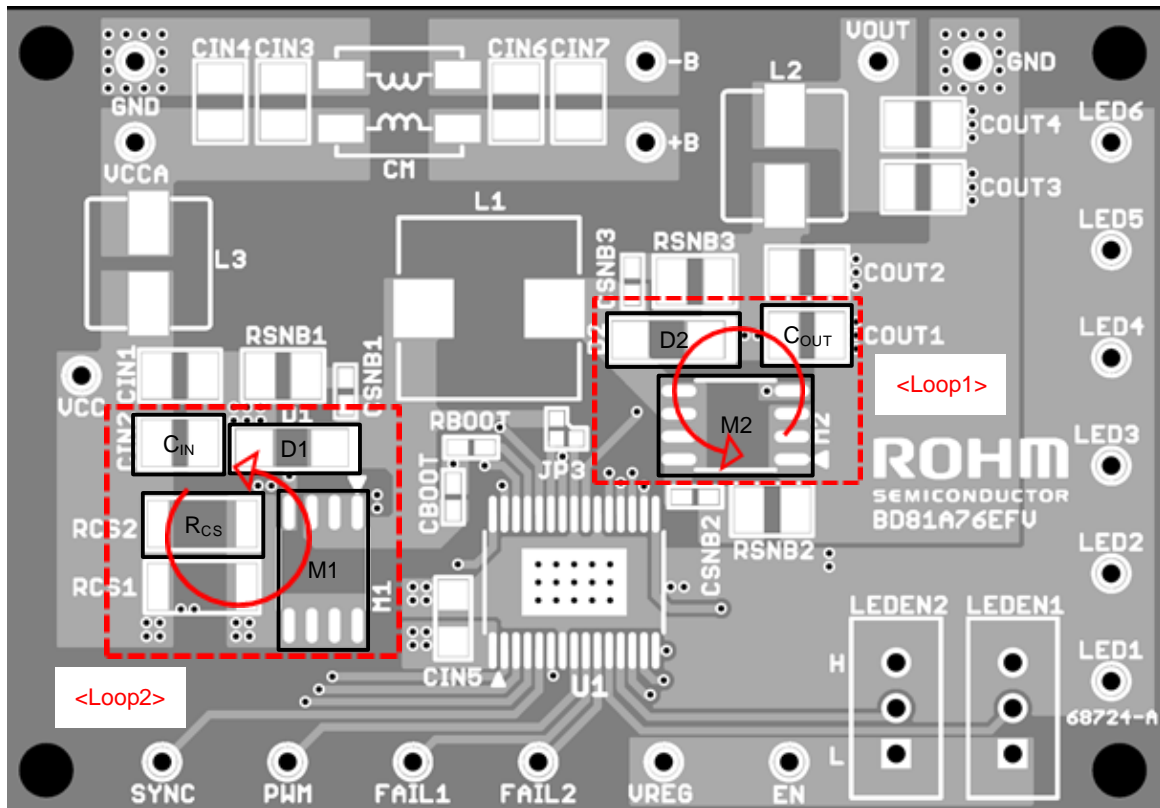


Figure 24. BD81A76EFV-M PCB TOP-layer

Calculation Example of Power Consumption

$$P_C = I_{CC} \times V_{CC}$$

... (1) Circuit Power

$$+ C_{ISS1} \times V_{VREG} \times f_{OSC} \times V_{VREG}$$

... (2) External Boost FET Power

$$+ C_{ISS2} \times V_{VREG} \times f_{OSC} \times V_{VREG}$$

... (3) External Buck FET Power

$$+ \{V_{LED} \times M + \Delta V_f \times (M - 1)\} \times I_{LED}$$

... (4) Current Driver Power

where:

 P_C is the IC power consumption. I_{CC} is the circuit current. V_{CC} is the supply voltage. C_{ISS1} is the external boost FET gate capacity. C_{ISS2} is the external buck FET gate capacity. V_{VREG} is the VREG voltage. f_{OSC} is the switching frequency. V_{LED} is the LED control voltage. M is the LED parallel number. ΔV_f is the LED Vf tolerance of each strings. I_{LED} is the LED output current.

<Sample Calculation>

I_{CC}=10 mA, V_{CC}=12 V, C_{ISS1}=2000 pF, C_{ISS2}=2000 pF, V_{VREG}=5 V, f_{OSC}=2200 kHz, V_{LED}=0.9 V, M=6, ΔV_f=0.2 V, I_{LED}=150 mA

$$P_C = 10mA \times 12V + 2000pF \times 5V \times 2200kHz \times 5V + 2000pF \times 5V \times 2200kHz \times 5V + \{0.9V \times 6ch + 0.2V \times (6ch - 1)\} \times 150mA = 1.30 \text{ [W]}$$

Because of θ_{ja}=24.45 °C/W, the maximum temperature rise amount (ΔT_{max}) is calculated below.

$$\Delta T_{max} = P_C \times \theta_{ja} = 1.3W \times 24.45 \text{ °C/W} = 31.8 \text{ [°C]}$$

When T_a=85 °C, maximum chip temperature (T_{Cmax}) is calculated below.

$$T_{Cmax} = 85 \text{ °C} + 31.8 \text{ °C} = 116.8 \text{ [°C]}$$

Confirm that T_{Cmax} calculated here is less than T_{jmax}=150 °C. The above is a simple calculation example, and the value of the thermal resistance changes by a real board condition and layout. Confirm the calculation here as a reference of the heat design.

I/O Equivalence Circuit

<p>VCC</p>	<p>SS</p>	<p>COMP</p>
<p>RT</p>	<p>SYNC, PWM</p>	<p>SSCG</p>
<p>FAIL1, FAIL2</p>	<p>LEDEN1, LEDEN2</p>	<p>LED1, LED2, LED3, LED4, LED5, LED6</p>
<p>OVP</p>	<p>ISET</p>	<p>OUTL</p>
<p>VDISC</p>	<p>SW</p>	<p>OUTH, BOOT</p>
<p>VREG</p>	<p>EN</p>	<p>CS</p>

*All values are Typical value

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

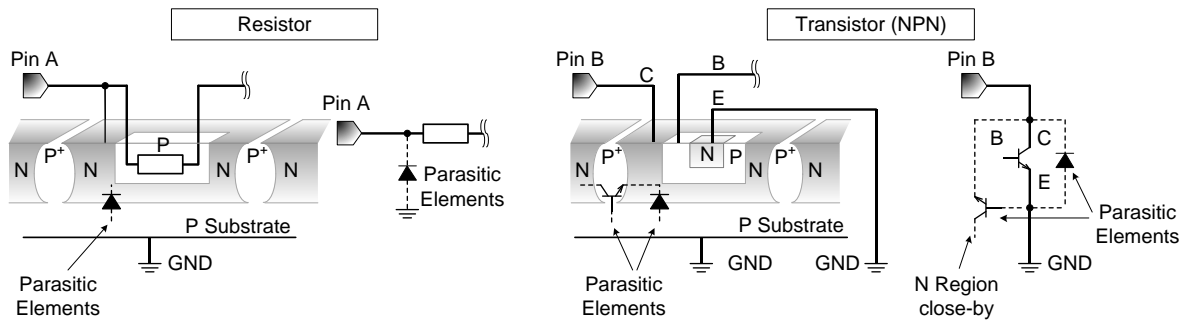
10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

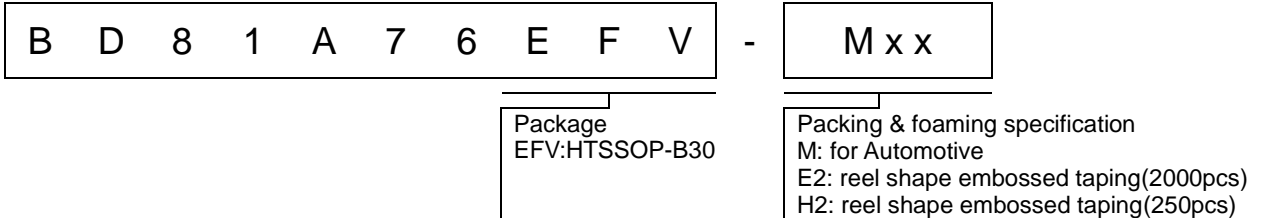
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

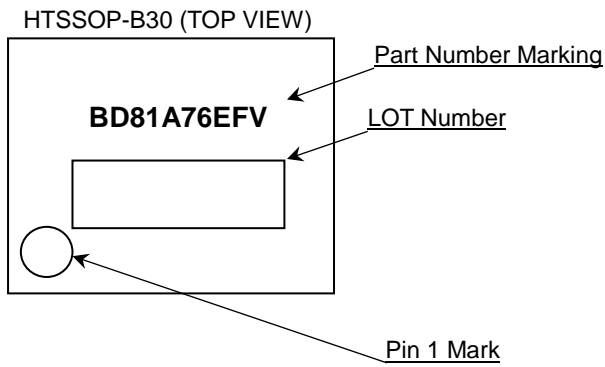
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

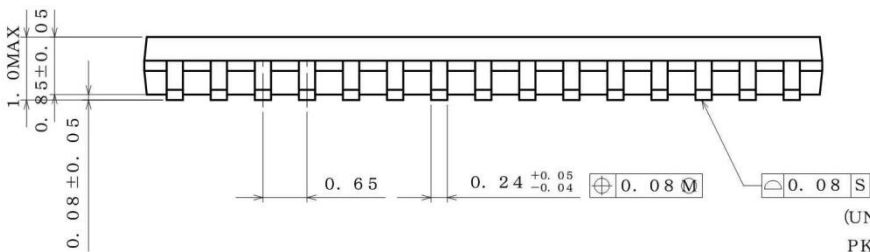
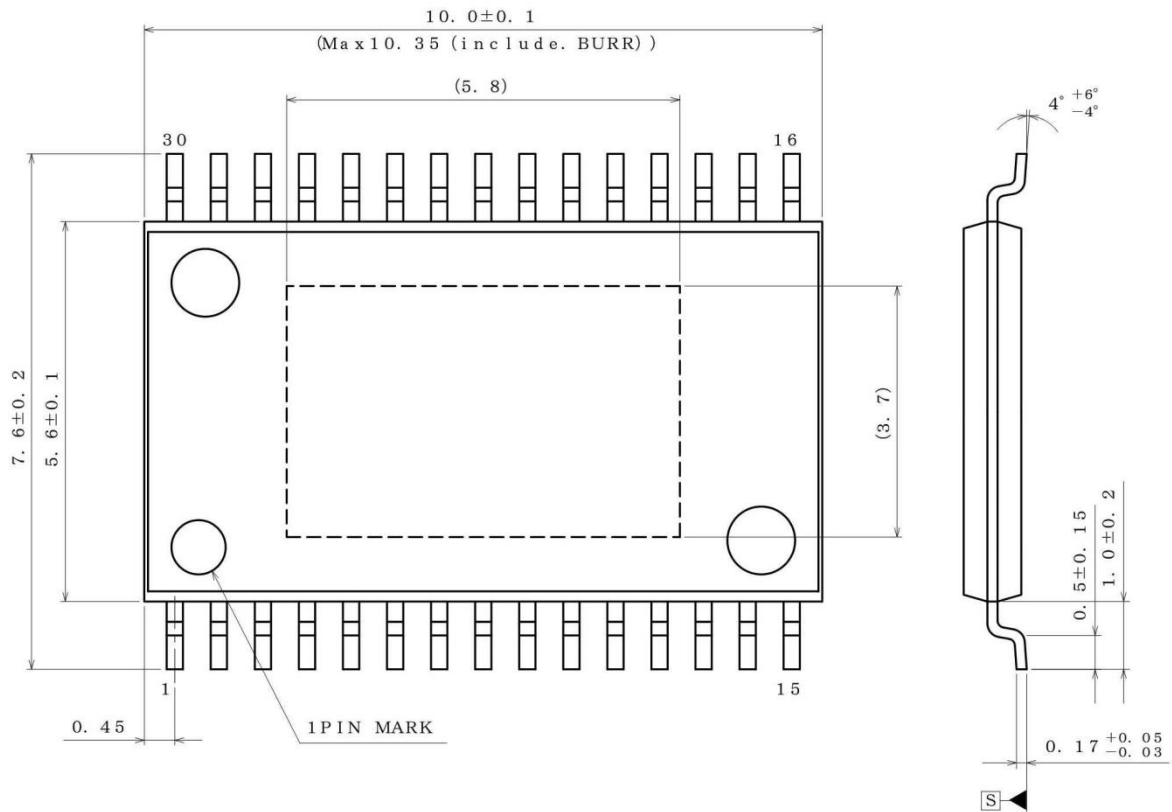


Marking Diagram



Physical Dimension and Packing Information

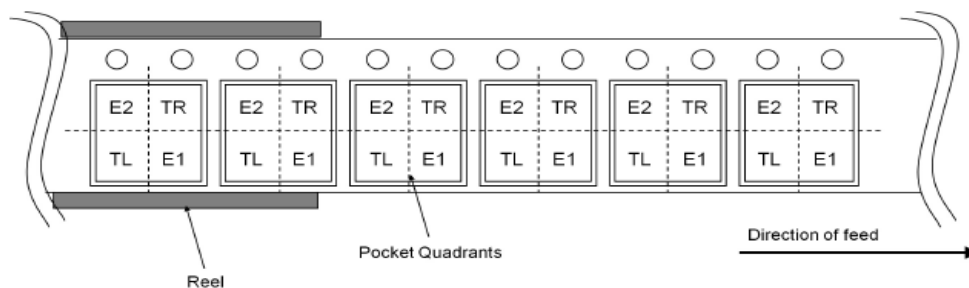
Package Name	HTSSOP-B30
--------------	------------



(UNIT : mm)
 PKG : HTSSOP-B30
 Drawing No. EX200-5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	E2 : 2000pcs / H2 : 250pcs
Direction of feed	The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Details
21.Feb.2019	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD81A76EFV-M - Web Page

[Distribution Inventory](#)

Part Number	BD81A76EFV-M
Package	HTSSOP-B30
Unit Quantity	2000
Minimum Package Quantity	2000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes