RICOH

RN5T5610 Series

Programmable Power Management System IC for Industrial Applications

NO. EY-579-200508

OUTLINE

The RN5T5610 is a power management multi-channel IC (PMIC) for industrial applications. This IC provides four high-efficiency step-down DCDC converters, seven low-dropout regulators, four GPIOs, an interrupt controller (INTC), and an I^{2}C-Bus interface. This IC can customize the power supply voltage and the power-on / off sequence to meet user-system with using a built-in OTP (One-Time Programmable) memory. In addition, this IC provides DVS (Dynamic Voltage Scaling), a thermal shut-down function, an overcurrent protection, and a watchdog timer and provides optionally a power-on / off mode which is controllable individually by GPIO[0-3] pins (Subsequently referred to as "Parts Mode[(1)]").

This is a high-reliability semiconductor device for industrial application that has passed both the screening at high temperature and the reliability test with extended hours.

FEATURES

- Operating Voltage Range (Maximum Rating)·····2.7 V to 5.5 V (6.0 V)
- Operating Temperature Range ·····-40°C to 105°C
- System:
  - ✓ I^{2}C-Bus interface @3.4MHz and 400kHz
  - ✓ Detector Function (System/IO-Voltage-detector, UVLO, DETVSB)
  - ✓ Thermal Shutdown Function
  - ✓ Watchdog Timer
  - ✓ Power-on Key Input for System's power up
  - ✓ Power-on Reset Output for CPU
  - ✓ Flexible Power-on / off Sequence by OTP
  - ✓ Flexible DCDC[1-4] and LDO[1-5] Default-on/off Control by OTP
- High Efficiency Step-down DCDC Converters:
  - ✓ DCDC1 / 2·····0.6 V to 3.5 V (Max. 3000 mA)
  - ✓ DCDC3 / 4·····0.6 V to 3.5 V (Max. 2000 mA)
  - ✓ Soft-start circuit
  - ✓ Equipped with DVS and Power Save Mode (PSM)
- Low Drop Voltage Regulators:
  - ✓ LDO1 / 2 ·····0.9 V to 3.5 V (Max. 300 mA)
  - ✓ LDO3 ·····0.6 V to 3.5 V (Max. 300 mA)
  - ✓ LDO4 / 5 ·····0.9 V to 3.5 V (Max. 200 mA)
  - ✓ LDORTC1 (Always-on, for Coin battery)··1.2 V to 3.5 V (Max. 30 mA)
  - ✓ LDORTC2 (Always-on)·····0.9 V to 3.5 V (Max. 10 mA)
  - ✓ Overcurrent Protection and Short-circuit Protection.
- 4-channel GPIO:
  - ✓ Interrupt function (level/edge) for input signals
  - ✓ Power-on output signal for external devices
  - ✓ Power on/off input for System's power up/down
  - ✓ Controllable DCDC[1-4] and LDO[1-5] by external input
  - ✓ LDORTC2 output via GPIO2 pin
  - ✓ Current Sink for LED via GPIO0/1 pins ···Max.15 mA
  - ✓ C32KOUT output via GPIO[0-3] as a clock for external devices
- Interrupt Controller (INTC)
- Package····· QFN0707-48-P25 (0.5mm pitch)

(1) Refer to "Parts Mode" for details.

APPLICATION

- FPGA / SoC Solution
- PLC / Servo Amp / Inverter
- Industrial Machine Controller Box

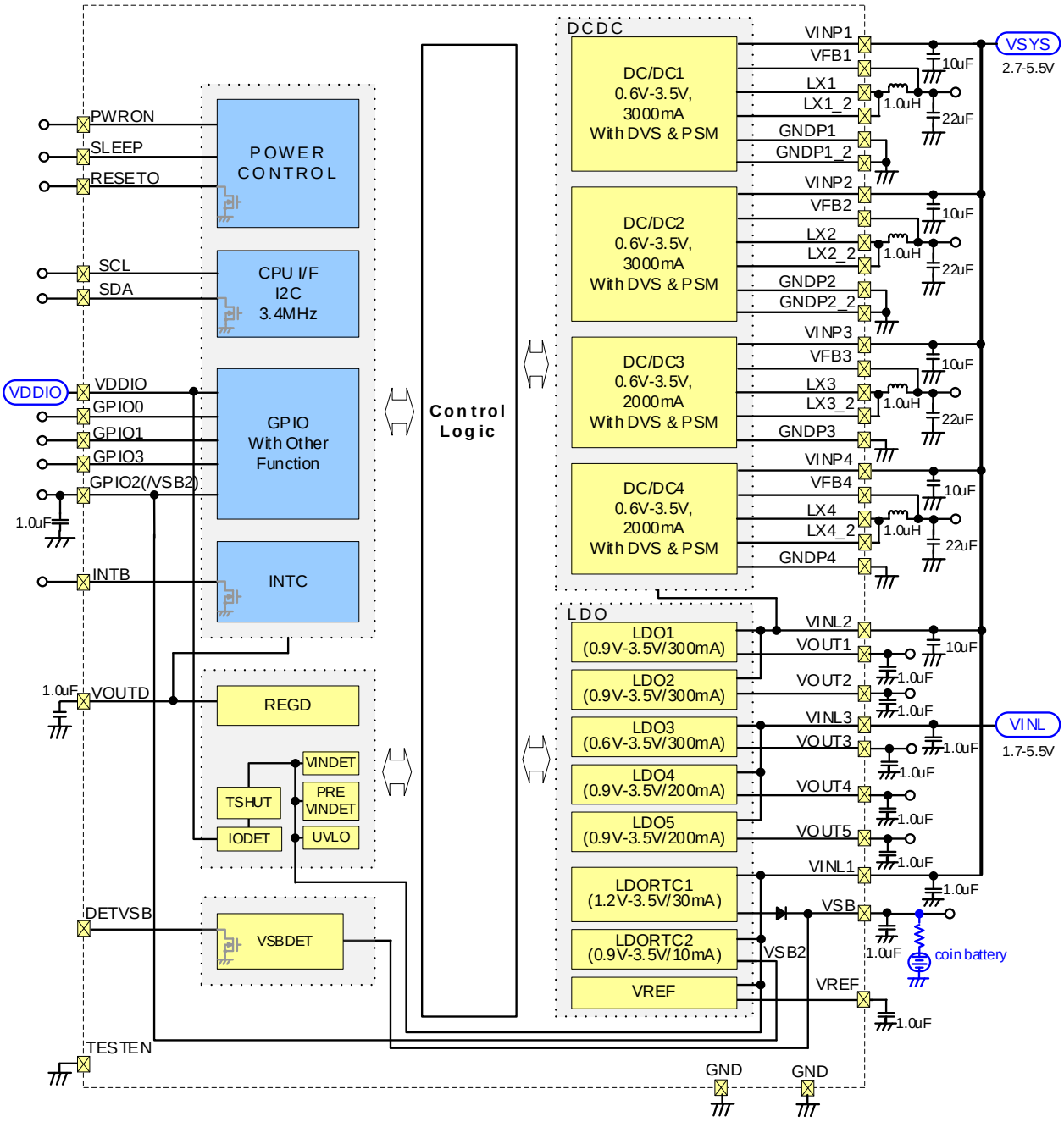
SELECTION GUIDE

Selection Guide

Product Name	Package	Halogen Free	Pb Free	Shipping (Packaging / MOQ)
RN5T5610xx-E4	QFN0707-48-P25	Yes	Yes	Reel / 2,000 pcs
RN5T5610xx				Tray / 50 pcs

xx : Specify the OTP code. Refer to the Appendix *"OTP Code List"* for details.

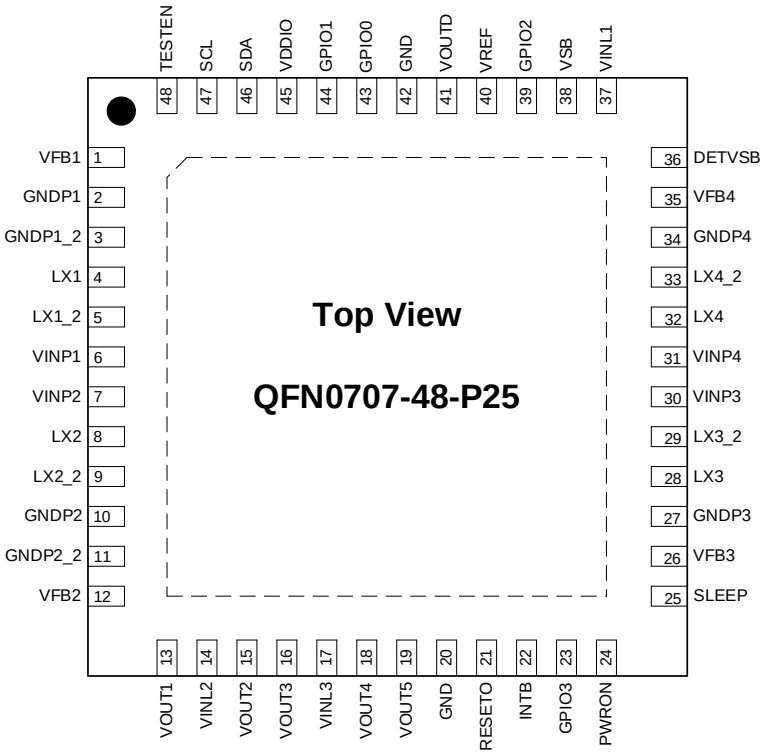
BLOCK DIAGRAM



RN5T5610 Block Diagram

PIN DESCRIPTION

Pin Configuration



RN5T5610 (QFN0707-48-P25) Pin Configuration

Pin Assignments

No.	Pin Name	Function	I/O(1)	D/A(2)	Reset State		Note
					I/O	Level	
1	VFB1	DCDC1 output voltage feedback signal	I/O	A			
2	GNDP1	GND for DCDC1	-	G			
3	GNDP1_2		-	G			
4	LX1	DCDC1 switching signal	O	A			
5	LX1_2		O	A			
6	VINP1	Power supply for DCDC1	-	P			
7	VINP2	Power supply for DCDC2	-	P			
8	LX2	DCDC2 switching signal	O	A			
9	LX2_2		O	A			
10	GNDP2	GND for DCDC2	-	G			
11	GNDP2_2		-	G			
12	VFB2	DCDC2 output voltage feedback signal	I/O	A			
13	VOUT1	LDO1 output voltage signal	O	A			
14	VINL2	Power supply for LDO1/2 and DCDC analog	-	P			
15	VOUT2	LDO2 output voltage signal	O	A			
16	VOUT3	LDO3 output voltage signal	O	A			
17	VINL3	Power supply for LDO3/4/5	-	P			
18	VOUT4	LDO4 output voltage signal	O	A			
19	VOUT5	LOD5 output voltage signal	O	A			
20	GND	GND for Logic circuit, Analog circuit, I/O, etc.	-	G			
21	RESETO	Host reset signal	O	D	O	Low	NOD
22	INTB	Interrupt request signal	O	D	O	Hi-z	NOD
23	GPIO3	General purpose I/O signal (3)	I/O	D			
24	PWRON	External power-on signal	I	D	I	-	1.4 V to V_{SYS}
25	SLEEP	Stand-by mode control signal	I	D	I	-	1.4 V to V_{SYS}
26	VFB3	DCDC3 output voltage feedback signal	I/O	A			
27	GNDP3	GND for DCDC3	-	G			
28	LX3	DCDC3 switching signal	O	A			
29	LX3_2		O	A			
30	VINP3	Power supply for DCDC3	-	P			
31	VINP4	Power supply for DCDC4	-	P			
32	LX4	DCDC4 switching signal	O	A			
33	LX4_2		O	A			
34	GNDP4	GND for DCDC4	-	G			
35	VFB4	DCDC4 output voltage feedback signal	I/O	A			
36	DETVSB	VSB output for Voltage detection (Nch Open-drain)	O	D	O	-	NOD
37	VINL1	Power supply for LDORTC1/2, VREF, DET, I/O, etc.	-	P			
38	VSB	LDORTC1 output voltage signal	O	A			
39	GPIO2 (/ VSB2)	General purpose I/O signal (3)	I/O	D			
40	VREF	Bypass capacitor connecting signal	O	A			
41	VOUTD	Capacitor connecting signal for built-in regulator	O	A			
42	GND	GND for Logic and Analog circuits, I/O, etc.	-	G			
43	GPIO0	General purpose I/O signal (3)	I/O	D			
44	GPIO1		I/O	D			
45	VDDIO	Power supply for CPU I/F	-	P			
46	SDA	I^2C bus data signal	I/O	D	I	-	CMOS Schmitt, NOD
47	SCL	I^2C bus input clock signal	I	D	I	-	CMOS Schmitt
48	TESTEN	Test signal (Connect to GND)	I	D	I	PD	CMOS Schmitt

(1) I: Input, O: Output
(2) A: Analog, D: Digital, P: Power, G: Ground
(3) GPIO[0-3]: "Input" or "Output" and its input/output type (CMOS or NMOS, Analog or Nch Open-drain output) are selectable by OTP. Refer to the chapter *"GPIO"* for details.

ABSOLUTE MAXIMUM RATINGS

(GNDs [1] = 0 V)

Symbol	Parameter	Conditions	Rating	Unit
V_{PS1}	Power Supply Voltage 1	VINP1-4 and VINL1-3 pins	-0.3 to 6.0	V
V_{PS2}	Power Supply Voltage 2	VDDIO pin	-0.3 to 4.5	V
V_{INPUT}	Input Voltage Range	PWRON and SLEEP pins	-0.3 to V_{SYS}+0.3	V
		SDA and SCL pins	-0.3 to 4.5	V
		GPIO0-1 pins	-0.3 to V_{SYS} +0.3 / -0.3 to V_{DDIO}+0.3	V
		GPIO2-3 pins	-0.3 to V_{SYS} +0.3	V
V_{OUTPUT}	Output Voltage Range	RESETO, INTB, and GPIO2-3 pins	-0.3 to V_{SYS} +0.3	V
		GPIO0-1 pins	-0.3 to V_{SYS} +0.3 / -0.3 to V_{DDIO}+0.3	V
		DETVSB pin	-0.3 to V_{SB}[2]+0.3	V
Tj	Junction Temperature	-	-40 to 125	°C
Tstg	Storage Temperature	-	-55 to 125	°C
P_D	Package Dissipation	Refer to Appendix *"POWER DISSIPATION".*		

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operations at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{SYS}	Power Supply Voltage	VINP1-4 and VINL1-2 pins [3]	2.7	3.6	5.5	V
V_{INL}	Power Supply Voltage	VINL3 pin [4]	1.7	3.6	5.5	V
V_{DDIO}	Power Supply Voltage	VDDIO pin (V_{SYS} > V_{DDIO})	1.7	1.8	3.4	V
V_{SB}	Power Supply Voltage	VSB pin	1.45	3.1	3.4	V
GND	Ground	GND, GNDP1, GNDP1_1, GNDP2, GNDP2_2, GNDP3, and GNDP4		0		V
Ta	Operating Temperature	-	-40		105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

[1] GNDs: GND signals including GND, GNDP1, GNDP1_1, GNDP2, GNDP2_2, GNDP3, and GNDP4.
[2] V_{SB}: LDORTC1_Output or Coin Battery
[3] VINP1-4 and VINL2 pin voltages must be equal to VINL1 pin voltage. To reduce the power supply, VINP1-4 and VINL2 pins can be powered off only in the POWROFF state. But the input pin level must be connected to GND only in Parts mode.
[4] VINL3 pin voltage must be less than or equal to VINL1 pin voltage.

ELECTRICAL CHARACTERISTICS

The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

RN5T5610 I/O Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VINL1 NMOS Input Pin: PWRON, SLEEP, GPIO0, GPIO1, GPIO2, GPIO3						
V_{IL}	Low level input voltage				0.4	V
V_{IH}	High level input voltage		1.4		V_{SYS}	V
VINL1 Nch Open-drain Output Pin: RESETO						
V_{OL}	Low level output voltage	I_{OUT} = 2mA			0.4	V
V_{TO}	Tolerant				V_{SYS}	V
VINL1 CMOS Input / Output Pin: GPIO0, GPIO1, GPIO2, GPIO3						
V_{IL}	Low level input voltage				V_{SYS} ×0.2	V
V_{IH}	High level input voltage		V_{SYS} ×0.8		V_{SYS}	V
V_{OL}	Low level output voltage	I_{OUT} = 4mA			0.4	V
V_{OH}	High level output voltage	I_{OUT} = -4mA	V_{SYS} -0.4			V
VINL1 Nch Open-drain Output Pin: INTB, GPIO0, GPIO1, GPIO2, GPIO3						
V_{OL}	Low level output voltage	I_{OUT} = 4mA			0.4	V
V_{TO}	Tolerant				V_{SYS}	V
VINL1 Nch Open-drain Output Pin: GPIO0, GPIO1 (for LED)						
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
V_{TO}	Tolerant				V_{SYS}	V
VSB Nch Open-drain Output Pin: DETVSB						
V_{OL}	Low level output voltage	I_{OUT} = 1mA			0.2	V
V_{TO}	Tolerant				V_{SB}	V
VOUTD CMOS Input Pin (Schmitt Input): SCL						
V_{IL}	Low level input voltage				V_{OUTD} (1) ×0.3	V
V_{IH}	High level input voltage		V_{OUTD} (1) ×0.7		3.4	V
ΔV_I	Hysteresis		V_{OUTD} (1) ×0.1			V
VOUTD CMOS Input / Output Pin (Schmitt Input / Nch Open-drain Output): SDA						
V_{IL}	Low level input voltage				V_{OUTD} (1) ×0.3	V
V_{IH}	High level input voltage		V_{OUTD} (1) ×0.7		3.4	V
ΔV_I	Hysteresis		V_{OUTD} (1) ×0.1			V
V_{OL}	Low level output voltage	I_{OUT} = 3mA			0.4	V
VDDIO CMOS Input / Output Pin: GPIO0, GPIO1						
V_{IL}	Low level input voltage				V_{DDIO} ×0.2	V
V_{IH}	High level input voltage		V_{DDIO} ×0.8		V_{DDIO}	V
V_{OL}	Low level output voltage	I_{OUT} = 4mA			0.4	V
V_{OH}	High level output voltage	I_{OUT} = -4mA	V_{DDIO} -0.4			V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

(1) V_{OUTD}: REGD_Output (1.8V)

V_{IN} = 3.6 V, No-load, unless otherwise specified.
The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

Consumption Current (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{ST}	Standby current	Power Off		13	35	μA
I_{OP}	Operating current	Power On		440	840	μA

Each parameter indicates the values (Typ./Max.) that the following conditions of Power OFF/ON are met.
The enabled LDO / DCDC at Power On are changeable depending on user-request.

Example of combinations of each Power Off / On

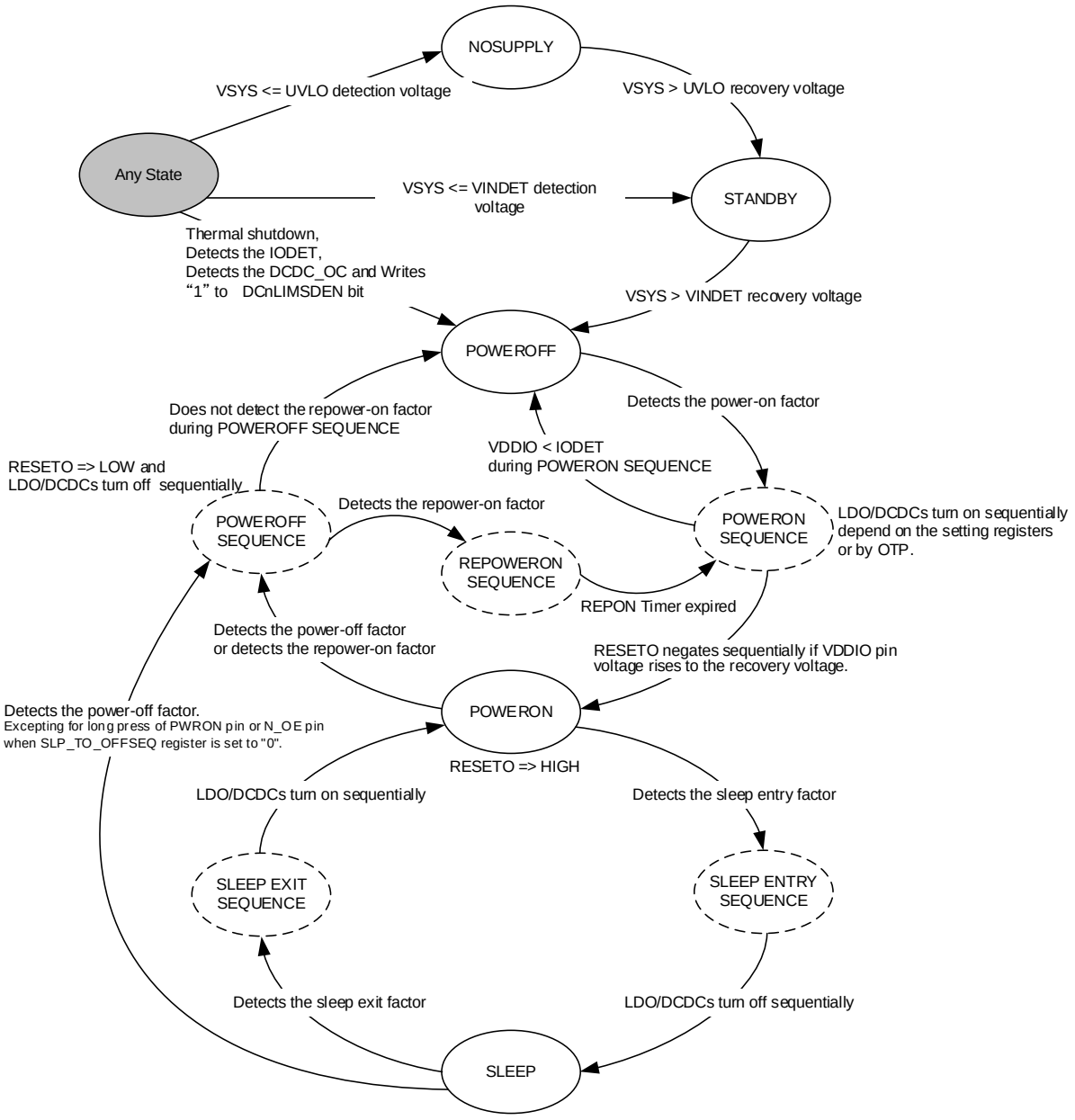
	Power OFF (1)	Power ON
LDO1	-	On
LDO2	-	On
LDO3	-	On
LDO4	-	On
LDO5	-	On
LDORTC1	On	On
LDORTC2	-	-
VREF	ECO	On
DCDC1	-	On
DCDC2	-	On
DCDC3	-	On
DCDC4	-	On
UVLO	On	On
VINDET	On	On
IODET	-	On
PREVINDET	-	On
VSBDET	On	On
TSHUT	-	On
REGD	On	On
Internal Logic	On	On

(1) Normal Mode

THEORY OF OPERATION

POWER CONTROL

This IC has the power-on/off sequence that can be flexibly set by OTP. The default on/off, timing, and voltage of DCDC[1-4] and LDO[1-5] are programmable. In addition, GPIO[0-3] pins output the power-on/off signal to external LDO/DCDC by the setting of OTP.



Power Control State Machine Diagram

State Machine Description

The state machine will step through the following statuses:

NOSUPPLY

The power supply to VSYS falls below the UVLO detection voltage.

STANDBY

The power supply to VSYS rises above the UVLO recovery voltage, followed by LDORTC1 turns on.

POWEROFF

The power supply to VSYS rises above the VINDET recovery voltage.
This IC is always monitoring the power-on factor, and if the factor is detected, it will start the power-on sequence.

POWERON SEQUENCE

LDO/DCDCs turn on sequentially according to a pre-programmed order by OTP. And RESETO will be pulled up high sequentially if VDDIO pin voltage rises to the recovery voltage. Even if VDDIO pin voltage falls below the IODET detection voltage during POWERON SEQUENCE state, it will change to POWEROFF state.

POWERON

RESETO is pulled up high. CPU can control this IC through some control pins or I^2C Interface. In this state, this IC is always monitoring the power-off or the repower-on factors.

POWEROFF SEQUENCE

This IC will change to this state by detecting the power-off factor in POWERON state. In this state, RESETO pin is output low level and all LDO/DCDCs turn off sequentially in reverse order of power-on sequence.

REPOWERON SEQUENCE

This IC will change to this state by detecting the repower-on factor. RESETO pin is output low level, and all LDO/DCDCs turn off sequentially in reverse order of power-on sequence. After turn-off is completed, repower-on timer starts, and it will change to POWERON SEQUENCE state when repower-on timer expired.

SLEEP ENTRY / EXIT SEQUENCE

This IC will change to this state by detecting the deep sleep entry/exit factor. LDO/DCDCs turn off/on sequentially and enter or exit SLEEP. Refer to SLEEP ENTRY / EXIT SEQUENCE section.

SLEEP

This IC will change to this state through SLEEP ENTRY SEQUENCE. In this state, it operates the low power consumption.

Shutdown

If this IC detects conditions shown below, this IC will change to NOSUPPLY state or STANDBY state or POWEROFF state regardless of the current state

- Low input voltage under the UVLO detection voltage
- Low input voltage under the VINDET detection voltage
- Low input voltage under the IODET detection voltage
  (Shutdown operation is disabled during POWERON/OFF and REPOWERON SEQUENCE.)
- Abnormal temperature
- Over current of DCDC*
  (Shutdown operation is disabled during POWERON/OFF SEQUENCE.)

Power-on Sequence

This IC's power is turned on by detecting the power-on factor at the POWEROFF state. The default settings of the resources as shown below are programmable. The slot duration can be selected in 0.5ms and 2ms by OTP.

[Controllable resources]

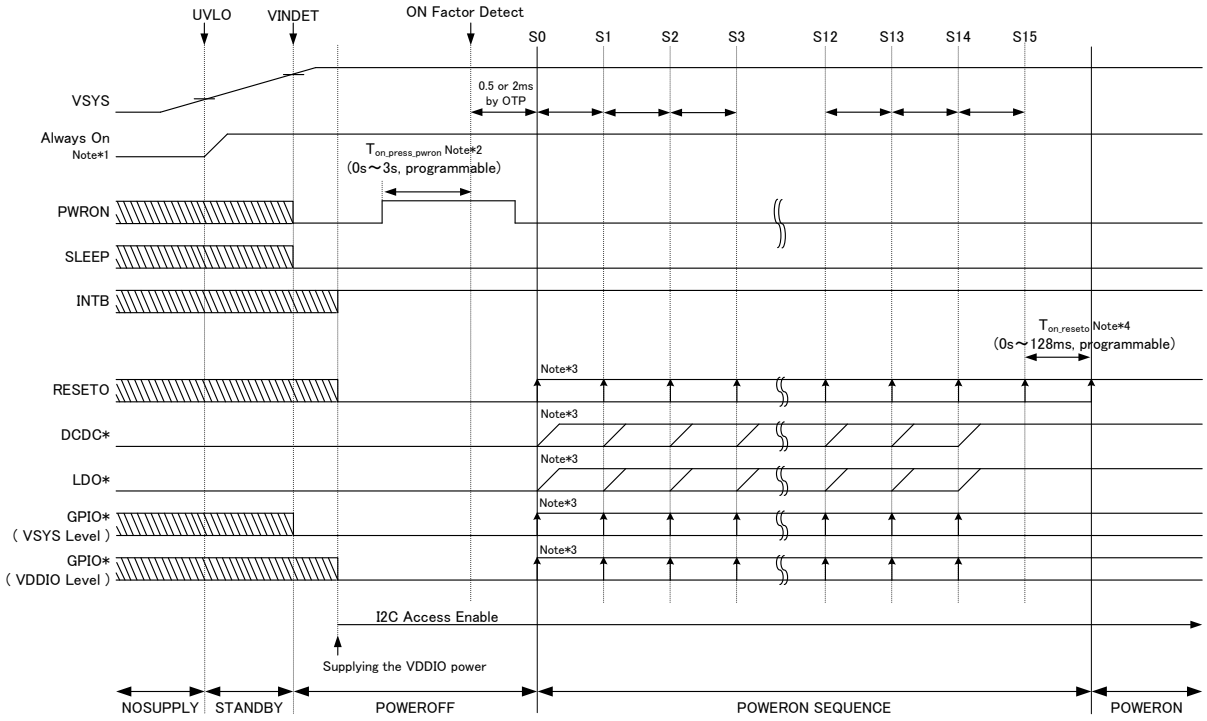
DCDC[1-4], LDO[1-5], RESETO, PSO[0-3](1)

[Power-on factor]

PWRON(2): High-level input to PWRON pin over a fixed time period.

ON_EXTIN(1): High-level input to ON_EXTIN pin.

Note: This IC powers on/off according to the on/off sequence. The interrupt is output when these pins are asserted. The power-on/off history is stored by the history register.



Notes:

1. Always-on for VREF/REGD works after UVLO released. LDORTC2 power-on timing is selectable between "Always-on" setting and the LDOEN2 register setting by OTP. LDORTC1 power-on timing is selectable between Always-on setting and the power-on sequence by OTP.
2. Initial values of register (0sec / 100us / 20ms / 128ms / 1sec / 2sec / 3sec) can be configured by OTP.
3. DCDC∗/LDO∗/GPIO∗ power-on timing (S0 to S14) is programmable by OTP.
   RESETO release timing (S0 to S15) is programmable by OTP.
4. Selected slot of DCDC∗/LDO∗/GPIO∗ must be set before RESETO release slot.
5. RESETO has extra time (0sec / 32ms / 64ms / 128ms) by OTP when it is programmed S15.

(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

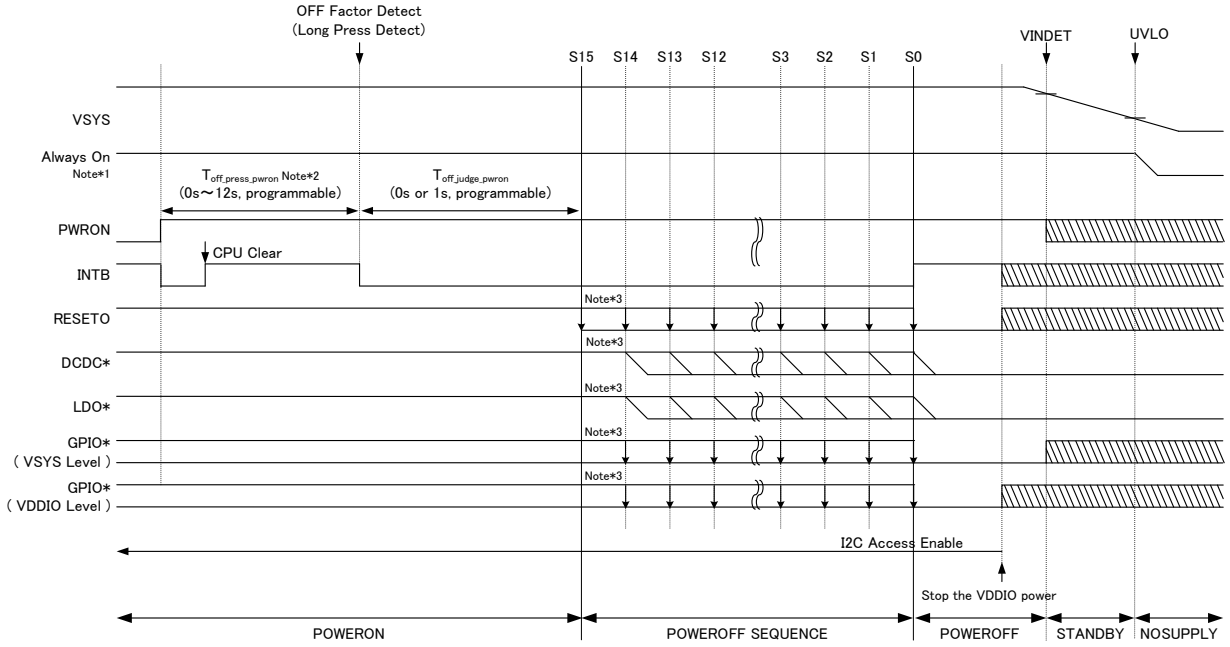
(2) Power-on factor is programmable by OTP.

Power-off Sequence

This IC's power is turn off by detecting the power-off factor at the POWERON or SLEEP state.

[Power-off factor]

Long power on key press:	High-level input to PWRON pin over a fixed time period.
Watchdog timer:	Internal watchdog timer expiration.
<SWPWROFF> register:	CPU's writing to a dedicated register.
N_OE(1):	High-level input to N_OE pin over a fixed time period.
PSHOLD(1):	Low-level input to PSHOLD pin.



Notes:

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2. This value (0 / 1 / 2 / 4 / 6 / 8 / 10 / 12 sec) can be selected by register.
3. The power-off timing reverse order of the power-on sequence.
   Selected slot of DCDC∗/LDO∗/GPIO∗ must set after RESETO assert slot.

(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

Sleep Entry/Exit Sequence

This IC is changed to the SLEEP state by detecting the sleep-entry factor at the PWRON and PWRON SEQUENCE state.

The state change timing of some resources as shown below is programmable.

[Controllable Resources]

Active/Sleep Control:	DCDC[1-4], LDO[1-5], PSO[0-3](1)
Output Voltage Control:	DCDC[1-4], LDO[1-5]

And, this IC is changed to the PWRON state by detecting the Sleep-exit factor at the SLEEP state.

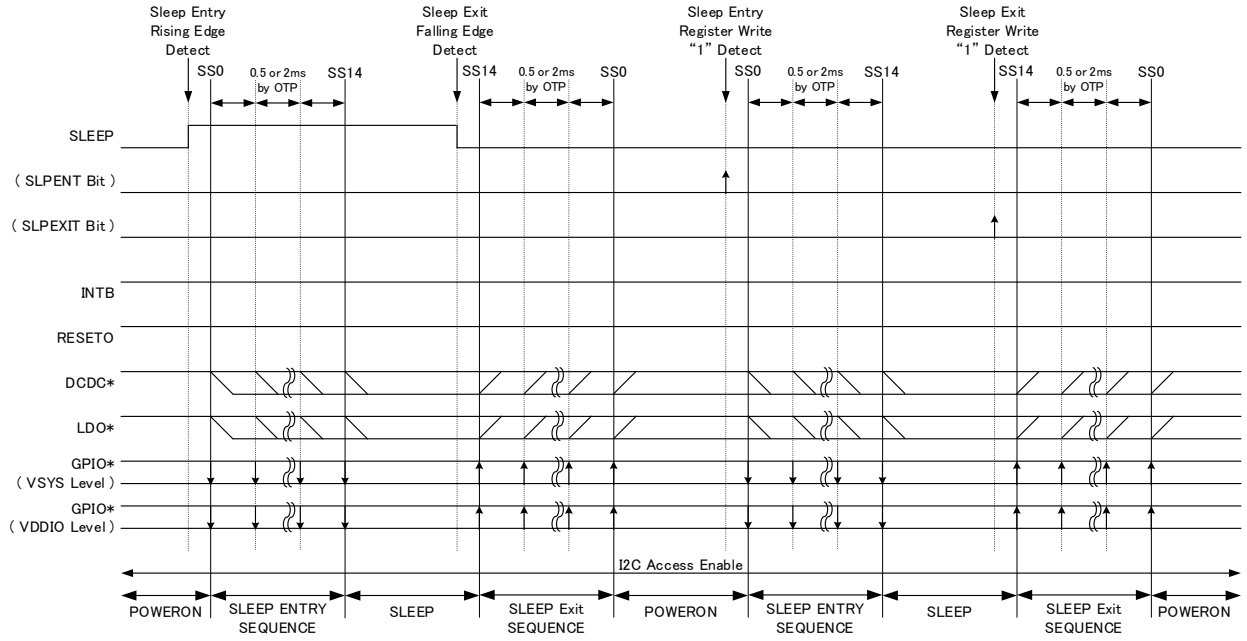
The state change timing of some resources is performed in reverse order of the sleep-entry sequence.

[Sleep-entry Factor]

SLEEP:	High-level input to SLEEP pin.
<SLPENT> register:	CPU's writing to a dedicated register.

[Sleep-exit Factor]

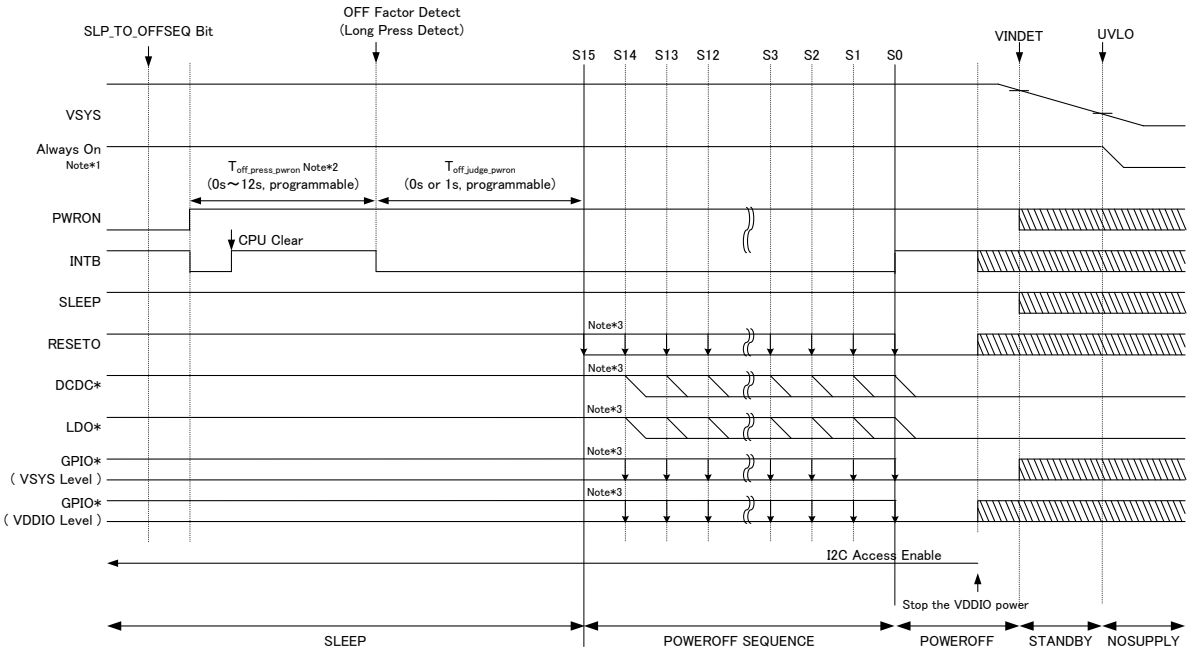
SLEEP:	Low-level input to SLEEP pin.
<SLPEXIT> register:	CPU's writing to a dedicated register.



(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

This IC is changed to the PWROFF SEQUENCE state by detecting PWRON long press at the SLEEP state. It is necessary to write the <SLP_TO_OFFSEQ> register in advance.

The state change timing of some resources is performed in reverse order of the power-on sequence.



Notes:

1. Always-on for VREF/REGD works after UVLO released. LDORTC2 power-on timing is selectable between “Always-on” setting and the LDOEN2 register setting by OTP. LDORTC1 power-on timing is selectable between Always-on setting and the power-on sequence by OTP.
2. This value (0 / 1 / 2 / 4 / 6 / 8 / 10 / 12 sec) can be selected by register.
3. The power-off timing is in reverse order of the power-on sequence.

Repower-on Sequence

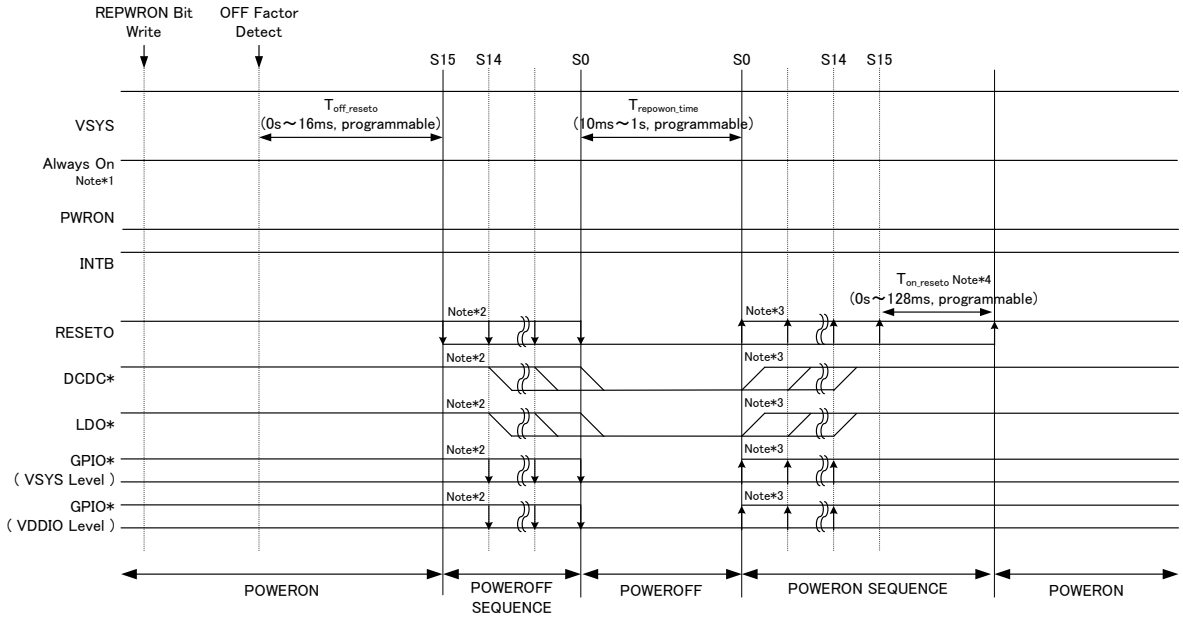
Once the repower-on factor is detected, this IC executes the power-on sequence after executing the power-off sequence without the power-on factor.

This IC does not change to POWERON state, when VDDIO pin voltage falls below the IODET detection voltage or repower-on timer is not expired. repower-on timer is selectable 10ms-1s. It is the waiting time for the all regulator's output capacitor to discharge.

[Repower-on factor]

Long power on key press:	High-level input to PWRON pin over a fixed time period.
Watchdog timer:	Internal watchdog timer expiration.
<SWPWROFF> register:	CPU's writing to a dedicated register.
N_OE(1):	High-level input to N_OE pin over a fixed time period.
HRESET(1):	High-level input to HRESET pin. After power off by detecting HRESET, this IC repower-on regardless of set value of REPWRON bit.

The state transition time from finishing the repower-on sequence to POWERON SEQUENCE state can be controlled by repower-on timer.



Notes:

1. Always-on for VREF/REGD works after UVLO released. LDORTC2 power-on timing is selectable between "Always-on" setting and the LDOEN2 register setting by OTP. LDORTC1 power-on timing is selectable between Always-on setting and the power-on sequence by OTP.
2. The power-off timing reverse order of the power-on sequence.
3. DCDC∗/LDO∗/GPIO∗ power-on timing (S0 to S14) is programmable by OTP.
4. RESETO has extra time (0 / 32 / 64 / 128 ms) by OTP when it is programmed S15.

(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

Shutdown Factor

The following factors trigger a shutdown, and each state is transited to NOSUPPLY State / STANDBY State / POWEROFF State.

The transition to POWERON State is enabled when each recovery condition for each shutdown factor is met.

	Shutdown Factor	State of Transition	Recovery Condition from Shutdown
1	UVLO detection	NOSUPPLY	UVLO release
2	VINDET detection	STANDBY	VINDET release
3	Temperature's abnormal detection	POWEROFF	Temperature's normal detection
4	DCDC∗ current limit detection (1)	POWEROFF	DCDC∗ current normal detection
5	IODET (VDDIO monitor) detection (2)	POWEROFF	IODET release

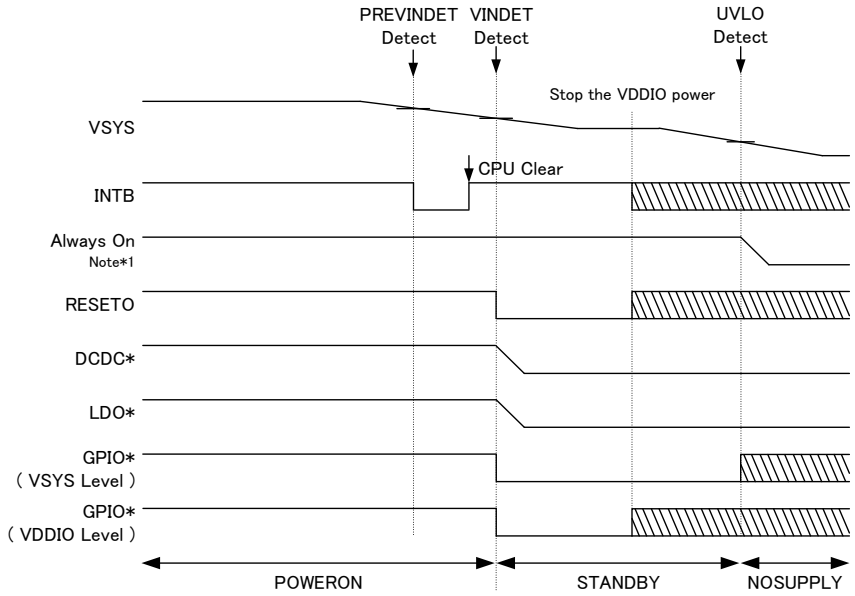
(1) Shutdown occurs if the over-current continues for 2ms. The shutdown operation is disabled during the POWERON / OFF sequence.

(2) The shutdown operation is disabled during the POWERON/OFF sequence and the REPOWERON sequence.

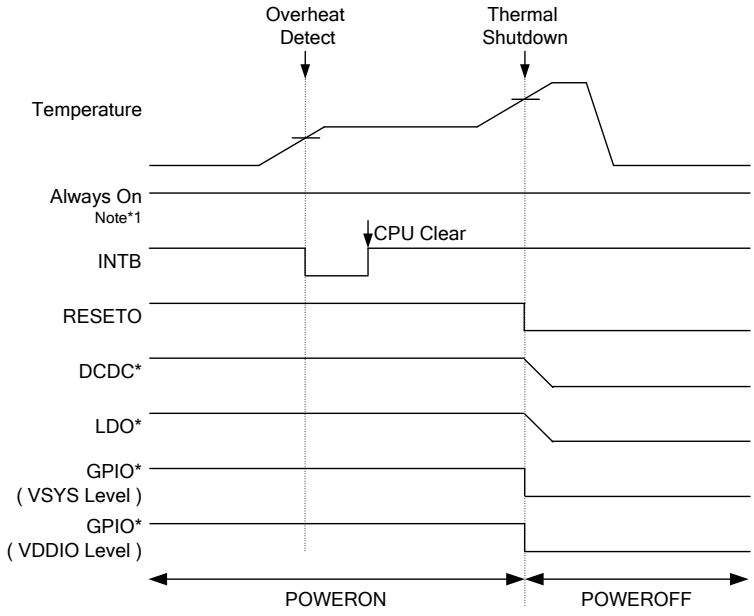
Shutdown Sequence

This IC is forcibly powered off when the shutdown factor is detected. All LDO/DCDCs are turned off at once. Until the shutdown condition is recovered, this IC does not accept the power-on factors. For the reset condition of register, refer to the register map.

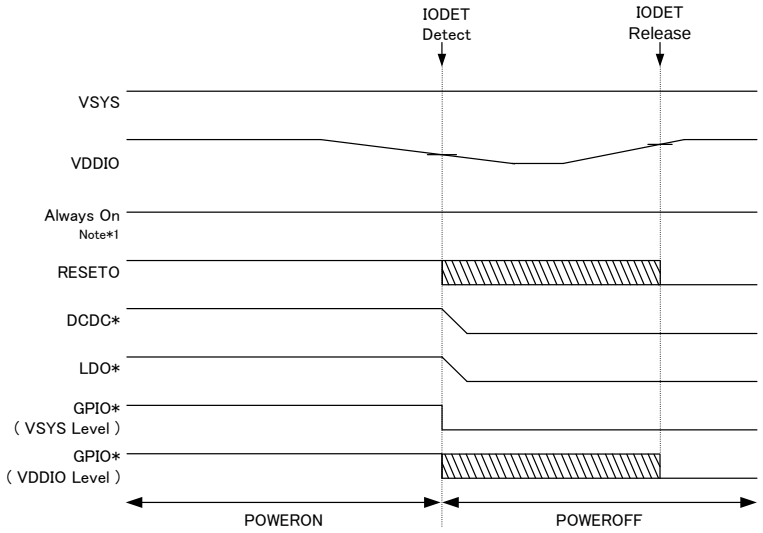
Shutdown Sequence (VINDET, UVLO)



Shutdown Sequence (Abnormal Temperature)

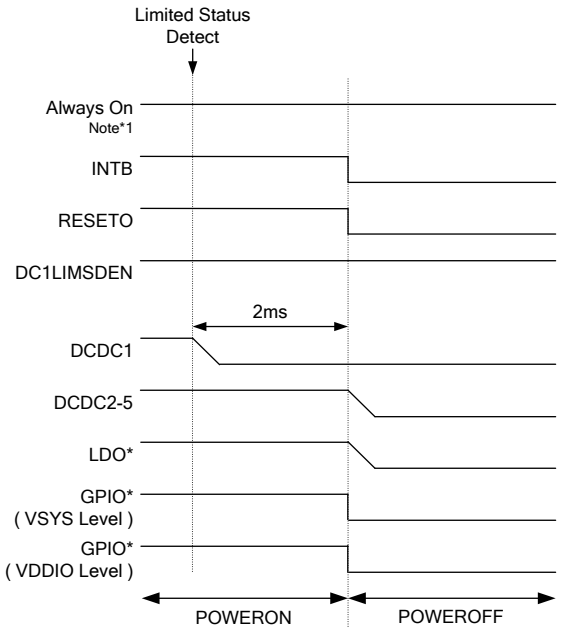


Shutdown Sequence (IODET)

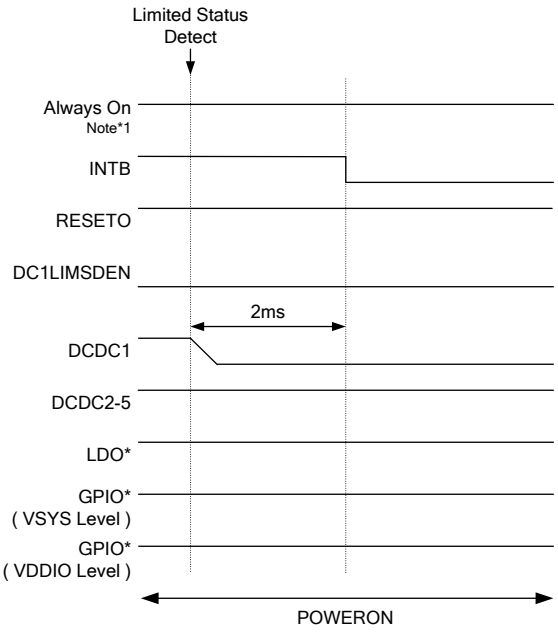


Shutdown Sequence (DCDC* current limit detection)

DC1LIMSDEN = 1 (Enable)



DC1LIMSDEN = 0 (Disable)



Notes:

1. Always-on for VREF/REGD works after UVLO released. LDORTC2 power-on timing is selectable between “Always-on” setting and the LDOEN2 register setting by OTP. LDORTC1 power-on timing is selectable between Always-on setting and the power-on sequence by OTP.
2. IODET is invalid when VDDIO is not selected as the power supply of both GPIO0 and GPIO1.

Power-on/off History

This IC has the register which monitors the power-on/off factor. After this IC powers on, CPU can recognize the power-on factor and power-off factor by reading PONHIS register and POFFHIS register.

The power-on factors as below are stored when the power-on sequence starts.

PWRON / ON_EXTIN [(1)] / HRESET [(1)]

The power-off /repower-on factors stored when the power-off sequence starts.

Long power on key press / Watchdog / SWPWROFF / N_OE [(1)] / PSHOLD [(1)] / HRESET [(1)]

The shutdown factors as below are stored immediately before the power-off.

TSHUT / VINDET / IODET / DCDC current limit

The repower-on factors as below are stored when the power-off sequence is finished

Repower-on

Watchdog Timer Function

This IC integrates a watchdog timer in order to power off the system when the CPU becomes hung-up. If the CPU does not access the WATCHDOG register until the watchdog timer expired, this IC output interrupt. And then if the CPU does not clear the interrupt within 1sec, this IC is transition to POWEROFF SEQUENCE.

A watchdog timer expiring time is programmable from 1 to 128 seconds with a default value of 128 seconds by dedicated register.

Power Control Block Interrupt Request

Power control block provides the interrupt requests to INTC block by the following pin input change or the transition state detection:

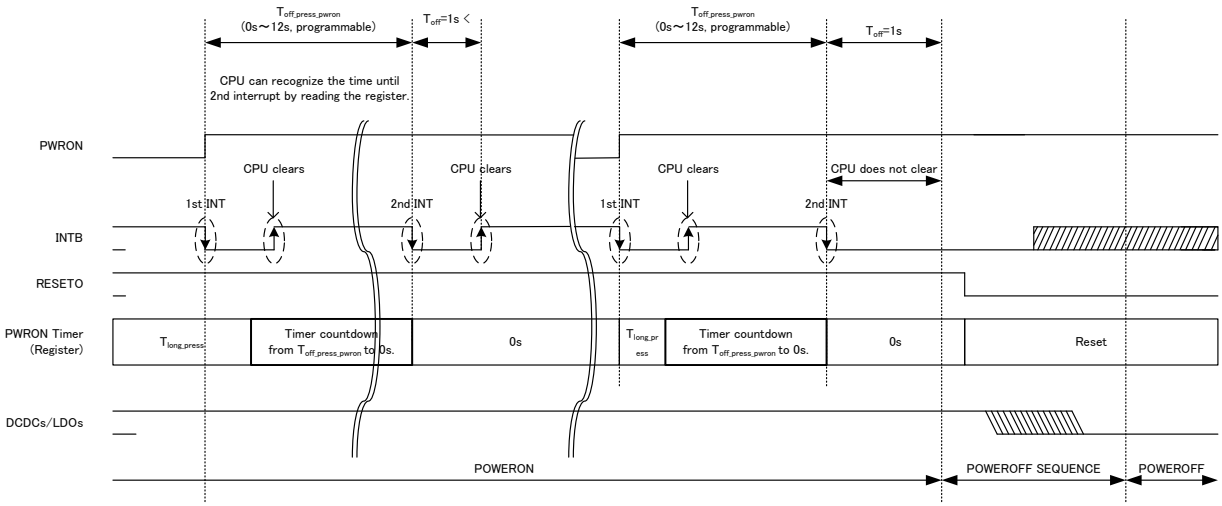
- PWRON pin input
  - ・Outputs the interrupt when PWRON pin input signal changes (See next section).
    Selectable both-edge/level interrupt type (Default level).
  - ・Outputs 2nd interrupt after PWRON pin input signal changes (See next section).
    The interrupt is falling-edge type. If it is not cleared, this IC powers off.
- Abnormal temperature detection
  - ・Outputs the interrupt when overheat detection circuit detects the abnormal temperature.
    Selectable both-edge/level interrupt type (Default level).
- Watchdog timer overflow
  - ・Outputs the interrupt when the watchdog timer expires.
- PREVINDET (Pre detection)
  - ・Outputs the interrupt when PREVINDET detects the pre detection voltage.
    Selectable both-edge/level interrupt type (Default level).

(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

The initial state of all the interrupt request signals from power control block is disabled. It is necessary to set the interrupt enable bit of each interrupt factor if the interrupt request output to INTC block is permitted. Even if the interrupt output is disabled, CPU can read each interrupt factor by PWRIRQ register.
For the details of interrupt, refer to the interrupt controller (INTC).

PWRON Long Press Operation

This IC can output two interrupts by changing the PWRON pin input signal during POWERON state. If CPU does not clear the 2nd interrupt, this IC changes to the POWEROFF state.
For other detailed operations, refer to the appendix.



Power-on Signal Output by GPIO0-3

This IC can output the power-on signal from GPIO[0-3] pins. This function is selected by OTP. The signals output by GPIO[0-3] are asserted sequentially according to a pre-programmed order by OTP. For example, these signals are used for operating external regulators. On SLEEP Entry/Exit sequence, these signals are programmable by the register.

Voltage Detector

The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

UVLO **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{RELEASE}$	UVLO threshold voltage	VINL1 voltage rising		2.30		V
V_{DETECT}	UVLO threshold voltage	VINL1 voltage falling	-10%	2.20	+10%	V
V_{HYS}	UVLO hysteresis			100		mV

・VINL1 < V_{DETECT} : Transition to NOSUPPLY state.

VINDET **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{RELEASE}$	VINDET threshold voltage	VINL1 voltage rising		2.90		V
V_{DETECT}	VINDET threshold voltage	VINL1 voltage falling	-3%	2.70	+3%	V
V_{HYS}	VINDET hysteresis			200		mV

・VINL1 < V_{DETECT} : Transition to STANDBY state or NOSUPPLY state.

・ V_{DETECT} is selected by OTP and register.

PREVINDET **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{RELEASE}$	PREVINDET threshold voltage	VINL1 voltage rising		2.85		V
V_{DETECT}	PREVINDET threshold voltage	VINL1 voltage falling	-3%	2.80	+3%	V
V_{HYS}	PREVINDET hysteresis			50		mV

・VINL1 < V_{DETECT} : Generate interrupt to INTB.

・V_{DETECT} is selected by OTP and register.

IODET **(Ta = 25°C)**

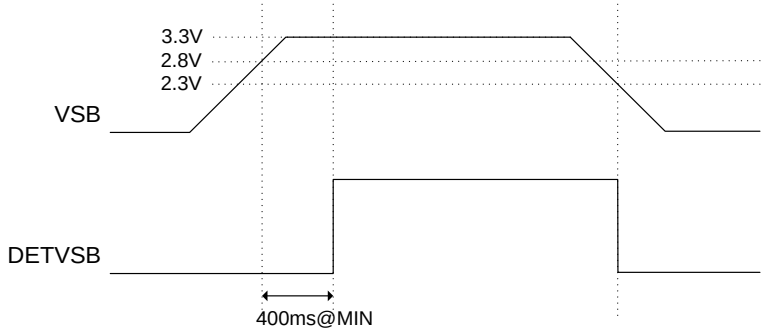
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{RELEASE}$	IODET threshold voltage	VDDIO voltage rising		1.65		V
V_{DETECT}	IODET threshold voltage	VDDIO voltage falling	-3%	1.60	+3%	V
V_{HYS}	IODET hysteresis			50		mV

・V_{DETECT} is selected by OTP and register.

VSBDET **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{RELEASE}$	VSBDET threshold voltage	VSB voltage rising		2.8		V
V_{DETECT}	VSBDET threshold voltage	VSB voltage falling	2.13	2.3	2.47	V
V_{HYS}	VSBDET hysteresis			500		mV

After VSB output (LDORTC1) rises, DETVSB signal turns to “High” after 400ms from the detection voltage is detected. DETVSB is Nch open-drain output pin.



Overheat Detection Block

Overheat Detection **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{DETECT}	Detection temperature	-	-	135 125 115 105	-	°C
$T_{RECOVER}$	Recover temperature	-	T_{DETECT} -20			°C

・Chip Temperature > T_{DETECT} : Generate interrupt to INTB.

・T_{DETECT} temperature is selected by OTP and register.

Thermal Shutdown **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{DETECT}	Detection temperature	-	-	140	-	°C
$T_{RECOVER}$	Recover temperature	-		110		°C

・Chip Temperature > T_{DETECT} : Transition to POWEROFF state.

REGULATORS

Regulator Tables

Symbol	DCDC1	DCDC2	DCDC3	DCDC4
Initial output voltage [V]	0.6 to 3.5	0.6 to 3.5	0.6 to 3.5	0.6 to 3.5
Maximum Output Current [mA]	3000	3000	2000	2000
External Inductor [µH]	1.0	1.0	1.0	1.0
External Capacitor [µF]	22	22	22	22
Output control	I^2C	I^2C	I^2C	I^2C

Regulator Table (DC/DC)

Symbol	LDO1	LDO2	LDO3	LDO4
Initial output voltage [V]	0.9 to 3.5	0.9 to 3.5	0.6 to 3.5	0.9 to 3.5
Maximum Output Current [mA]	300	300	300	200
Transient Response [mV] (1)	10	10	40	40
Ripple Rejection [dB] (2)	70	70	60	60
Output Noise [µVrms] (3)	25	25	60	50
External Capacitor [µF]	1	1	1	1
Output control	I^2C	I^2C	I^2C	I^2C

Symbol	LDO5	LDORTC1	LDORTC2	
Initial output voltage [V]	0.9 to 3.5	1.2 to 3.5	0.9 to 3.5	
Maximum Output Current [mA]	200	30	10	
Transient Response [mV] (1)	40	-	-	
Ripple Rejection [dB] (2)	60	-	-	
Output Noise [µVrms] (3)	50	-	-	
External Capacitor [µF]	1	1	1	
Output control	I^2C	Always-on / I^2C	Always-on / I^2C	

Regulator Table (LDO)

(1) Conditions: I_{OUT} = 100µA ↔ I_{OUTMAX} / 2

(2) Conditions: f = 217Hz to 1kHz, I_{OUT} = I_{OUTMAX} / 2, V_{DIFF} ≥ 0.6V

(3) Conditions: I_{OUT} = I_{OUTMAX} / 2, BW = 10Hz to 100kHz, V_{OUT} = 1.2V

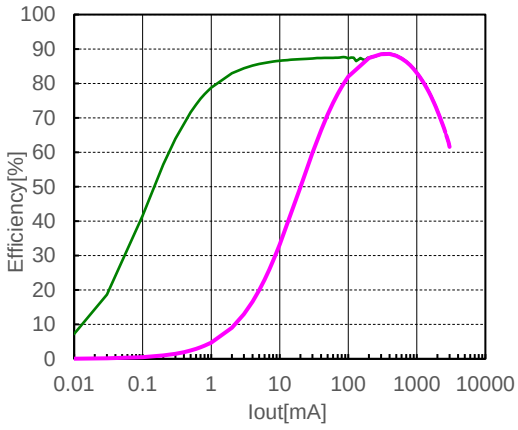
DCDC Electrical Characteristics

C_{IN} = 10 µF / C_{OUT} = 22 µF / L = 1µH, unless otherwise specified.
The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

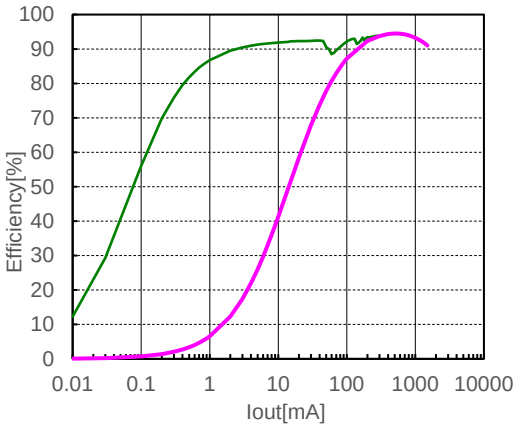
DCDC1-2 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-		2.7	3.6	5.5	V
V_{OUT}	Output voltage range	-		0.6	1.2	3.5	V
	Voltage setting step width	-			12.5		mV
V_{ACCU}	Output voltage accuracy	1mA ≤ I_{OUT} ≤ I_{OMAX} Auto/PSM/PWM Mode	V_{OUT} ≤ 1.0V	-20	0	20	mV
			1.0V ≤ V_{OUT}	-2	0	2	%
V_{RIP}	Output ripple voltage	PWM Mode		-10		10	mV
F_{OSC}	Switching frequency	PWM Mode		-10%	1.8(1)	+10%	MHz
I_{OUT_MAX}	Maximum output current(2)	Auto/PWM Mode V_{OUT} ≤ 3.5V, V_{IN} = V_{OUT}+1.0V		1000			mA
		Auto/PWM Mode V_{OUT} ≤ 2.4V, V_{IN} = V_{OUT}+1.1V		2000			mA
		Auto/PWM Mode V_{OUT} ≤ 1.5V, V_{IN} = V_{OUT}+1.5V		3000			mA
		PSM Mode		10			mA
I_{LIM1}	Limit current	DCnLIM bit (n:1, 2) = 3.2A		3200	4000		mA
V_{PEAK}	Output transition response	10 → 400mA@ΔT = 1.0µs, V_{IN} = 3.6V, V_{OUT} = 1.2V				5	%
I_{SS}	Consumption current	Auto Mode	I_{OUT} = 0mA		45	70	µA
		PSM Mode	I_{OUT} = 0mA		25	50	µA

※V_{IN} = 3.6V, V_{OUT} = 1.2V, f = 1.8MHz, L = 1.0µH



※V_{IN} = 5.0V, V_{OUT} = 3.3V, f = 1.8MHz, L = 1.0µH



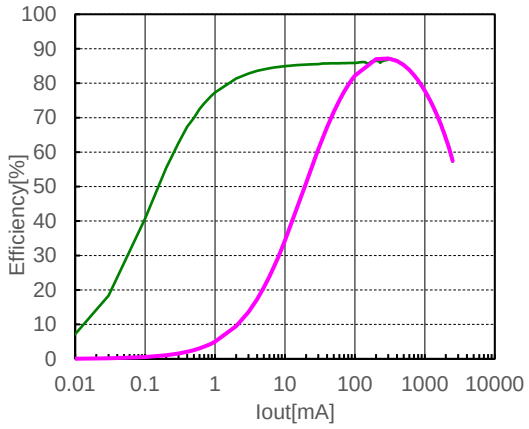
-PWMFIX
-AUTO

(1) Each switching frequency can be selected by OTP. Please contact us for more details.
(2) Each average load current must be suppressed as below.
DCDC1-2: 2.4A or less.
If load exceeding allowable average load current is applied, IC life may be shortened.

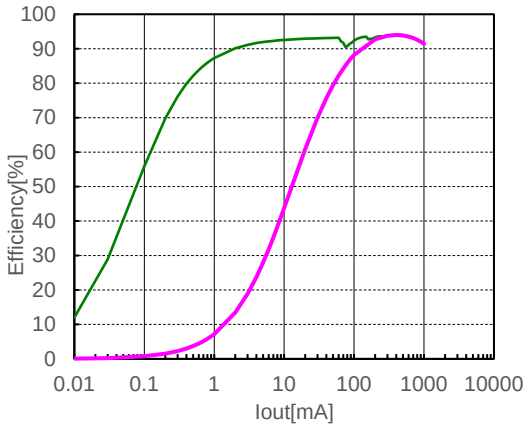
DCDC3-4 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-		2.7	3.6	5.5	V
V_{OUT}	Output voltage range	-		0.6	1.2	3.5	V
	Voltage setting step width	-			12.5		mV
V_{ACCU}	Output voltage accuracy	1mA ≤ I_{OUT} ≤ Iomax	V_{OUT} ≤ 1.0V	-20	0	20	mV
		Auto/PSM/PWM Mode	1.0V ≤ V_{OUT}	-2	0	2	%
V_{RIP}	Output ripple voltage	PWM Mode		-10		10	mV
F_{OSC}	Switching frequency	PWM Mode		-10%	1.8(1)	+10%	MHz
I_{OUT_MAX}	Maximum output current(2)	Auto/PWM Mode V_{OUT} ≤ 3.5V, V_{IN} = V_{OUT}+1.0V		500			mA
		Auto/PWM Mode V_{OUT} ≤ 3.1V, V_{IN} = V_{OUT}+1.1V		1000			mA
		Auto/PWM Mode V_{OUT} ≤ 1.5V, V_{IN} = V_{OUT}+1.6V		2000			mA
		PSM Mode		10			mA
I_{LIM1}	Limit current	DCnLIM bit (n:3, 4) = 2.3A		2300	3000		mA
V_{PEAK}	Output transition response	10→400mA@ΔT = 1.0μs, V_{IN} = 3.6V, V_{OUT} = 1.2V				5	%
I_{SS}	Consumption current	Auto Mode	I_{OUT} = 0mA		45	70	μA
		PSM Mode	I_{OUT} = 0mA		25	50	μA

※V_{IN} = 3.6V, V_{OUT} = 1.2V, f = 1.8MHz, L = 1.0μH



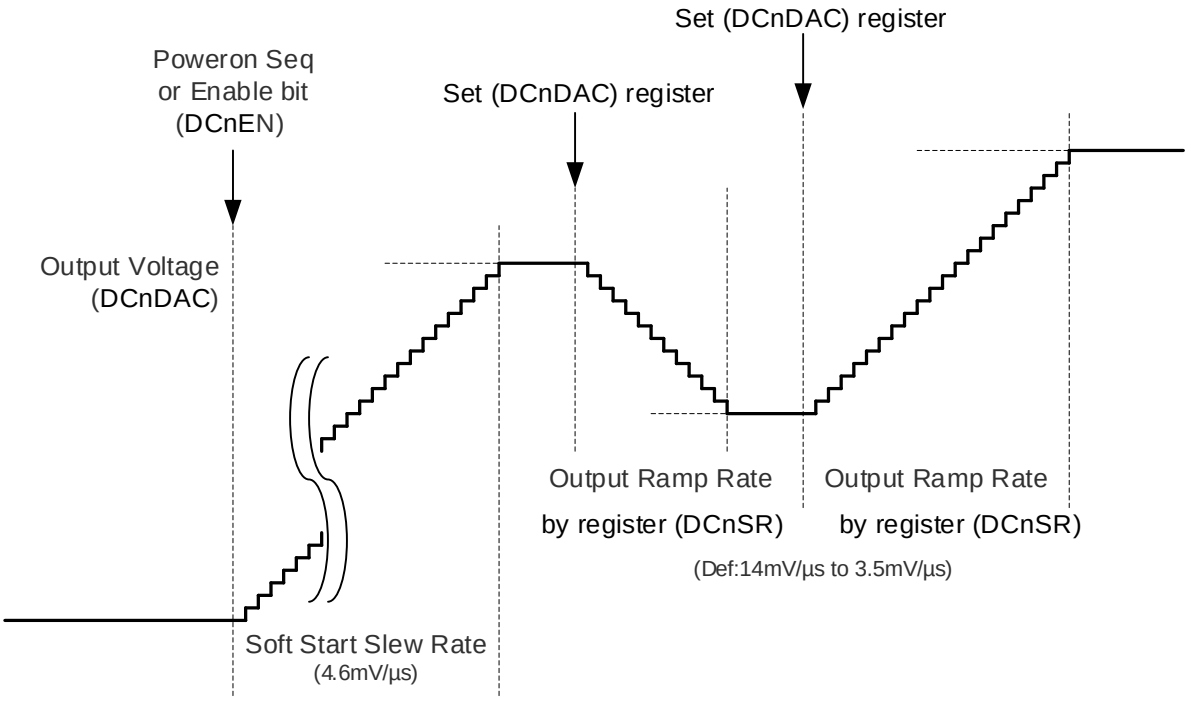
※V_{IN} = 5.0V, V_{OUT} = 3.3V, f = 1.8MHz, L = 1.0μH



(1) Each switching frequency can be selected by OTP. Please contact us for more details.
(2) Each average load current must be suppressed as below.
DCDC3-4: 1.75A or less.
If load exceeding allowable average load current is applied, IC life may be shortened.

RAMP Control Operation

This function starts by setting DCnDAC register and the ramp rate is controllable by DCnSR bit. (n: 1 to 4)



Ramp up/down Control Timing Chart

LDO Electrical Characteristics

V_{IN} = 3.6 V, C_{OUT} = 1.0 µF, unless otherwise specified.
The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

LDO1-2 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	2.7	3.6	5.5	V
V_{OUT}	Output voltage range		0.9		3.5	V
	Voltage setting step width			50		mV
V_{ACCU}	Output voltage accuracy	V_{OUT} = all output range, I_{OUT} = 1mA	-2.0		2.0	%
I_{OUTMAX}	Output current	-			300	mA
I_{LIM}	Limit current		350	500		mA
V_{DIFF}	Dropout voltage	V_{OUT} setting = V_{IN}, I_{OUT} = I_{OUTMAX}			0.2	V
V_{LINE}	Line regulation	2.7V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA			0.2	%/V
V_{LOAD}	Load regulation	1mA ≤ I_{OUT} ≤ I_{OUTMAX}			35	mV
I_{SS}	Supply current	I_{OUT} = 0mA		100	150	µA
I_{OFF}	Standby current	I_{OUT} = 0mA			1	µA
T_R	Rising time	V_{OUT}×0.9, I_{OUT} = 0mA			500	µs
T_F	Falling time	V_{OUT}×0.1, I_{OUT} = 0mA			500	µs

LDO3 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	1.7	3.6	5.5	V
V_{OUT}	Output voltage range		0.6		3.5	V
	Voltage setting step width			50		mV
V_{ACCU}	Output voltage accuracy	V_{OUT} = all output range, I_{OUT} = 1mA	-2.0		2.0	%
I_{OUTMAX}	Output current	-			300	mA
I_{LIM}	Limit current		350	500		mA
V_{DIFF}	Dropout voltage	V_{OUT} setting = V_{IN}, I_{OUT} = I_{OUTMAX}			0.3	V
V_{LINE}	Line regulation	1.7V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA			0.2	%/V
V_{LOAD}	Load regulation	1mA ≤ I_{OUT} ≤ I_{OUTMAX}			35	mV
I_{SS}	Supply current	I_{OUT} = 0mA		20	40	µA
I_{OFF}	Standby current	I_{OUT} = 0mA			1	µA
T_R	Rising time	V_{OUT}×0.9, I_{OUT} = 0mA			500	µs
T_F	Falling time	V_{OUT}×0.1, I_{OUT} = 0mA			500	µs

LDO4-5 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	1.7	3.6	5.5	V
V_{OUT}	Output voltage range		0.9		3.5	V
	Voltage setting step width			50		mV
V_{ACCU}	Output voltage accuracy	V_{OUT} = all output range, I_{OUT} = 1mA	-2.0		2.0	%
I_{OUTMAX}	Output current	-			200	mA
I_{LIM}	Limit current		250	350		mA
V_{DIFF}	Dropout voltage	V_{OUT} setting = V_{IN}, I_{OUT} = I_{OUTMAX}			0.4	V
V_{LINE}	Line regulation	1.7V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA			0.2	%/V
V_{LOAD}	Load regulation	1mA ≤ I_{OUT} ≤ I_{OUTMAX}			40	mV
I_{SS}	Supply current	I_{OUT} = 0mA		20	40	µA
I_{OFF}	Standby current	I_{OUT} = 0mA			1	µA
T_R	Rising time	V_{OUT}×0.9, I_{OUT} = 0mA			500	µs
T_F	Falling time	V_{OUT}×0.1, I_{OUT} = 0mA			500	µs

LDORTC1 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	2.2	3.6	5.5	V
V_{OUT}	Output voltage range		1.2		3.5	V
	Voltage setting step width			50		mV
V_{ACCU}	Output voltage accuracy	V_{OUT} = all output range, I_{OUT} = 1mA	-2.0		2.0	%
$I_{OUTMAX1}$	Output current				30	mA
$I_{OUTMAX2}$		4.5V ≤ V_{IN} ≤ 5.5V			100	mA
V_{DIFF}	Dropout voltage	V_{OUT} setting = V_{IN}, I_{OUT} = $I_{OUTMAX1}$			0.8	V
I_{LIM}	Limit current		110	170		mA
I_{SS}	Supply current	I_{OUT} = 0mA		2	4	µA
I_{OFF}	Standby current	I_{OUT} = 0mA			1	µA

LDORTC2 Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range	-	2.2	3.6	5.5	V
V_{OUT}	Output voltage range		0.9		3.5	V
	Voltage setting step width			50		mV
V_{ACCU}	Output voltage accuracy	V_{OUT} = all output range, I_{OUT} = 1mA	-2.0		2.0	%
I_{OUTMAX}	Output current	-			10	mA
I_{LIM}	Limit current		20	120		mA
V_{DIFF}	Dropout voltage	V_{OUT} setting = V_{IN}, I_{OUT} = I_{OUTMAX}			0.2	V
I_{SS}	Supply current	I_{OUT} = 0mA		1	2	µA
I_{OFF}	Standby current	I_{OUT} = 0mA			1	µA

MODE

This IC has two Modes selected by OTP.

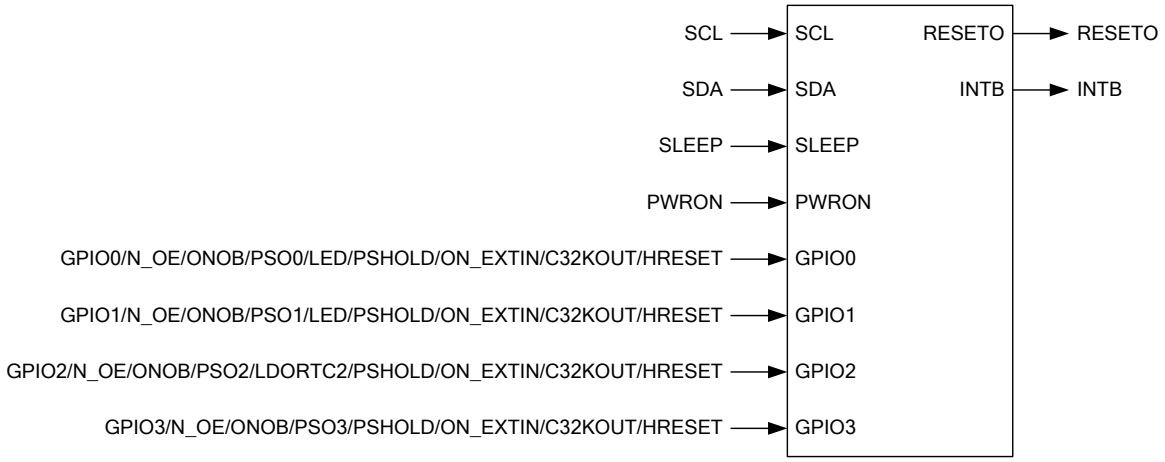
MODE	Pin					
	GPIO0	GPIO1	GPIO2	GPIO3	SLEEP	PWRON
Normal	selectable				SLEEP	PWRON
Parts	DCDC1 EXON	DCDC2 EXON	DCDC3 EXON	DCDC4EXON and LDO3EXON	LDO1EXON and LDO4EXON	LDO2EXON and LDO5EXON

Modes and Function of Pins

Normal Mode

The function of GPIO[0-3] (1) pins can be respectively selected by OTP.

The function of SLEEP and PWRON pins are respectively decided SLEEP and PWRON.



(1) For details of the function of GPIO[0-3] pins, refer to the chapter *"GPIO"*.

Parts Mode

ON/OFF of DCDC[1-4] and LDO[1-5] can be controlled by pin.

GPIO0 pin can control ON/OFF of DCDC1.

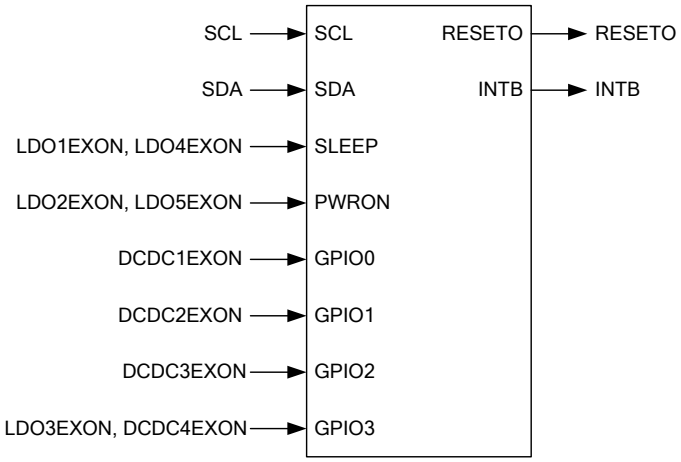
GPIO1 pin can control ON/OFF of DCDC2.

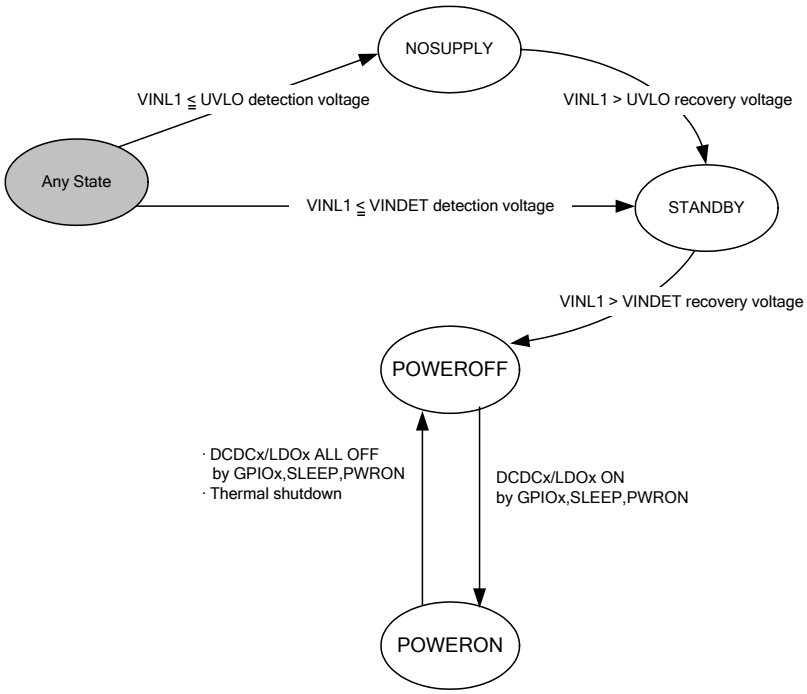
GPIO2 pin can control ON/OFF of DCDC3.

GPIO3 pin can control ON/OFF of DCDC4 and LDO3.

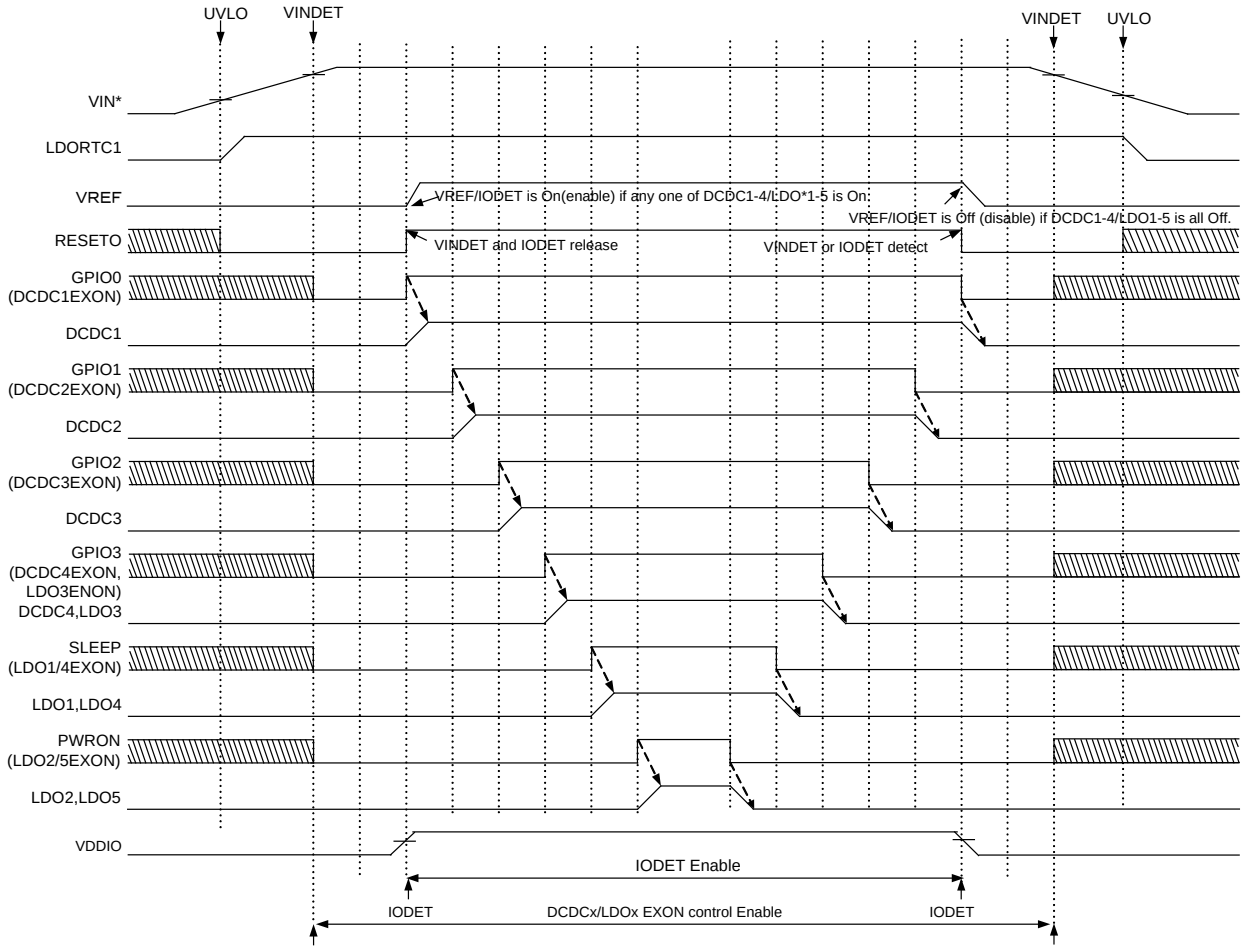
SLEEP pin can control ON/OFF of LDO1 and LDO4.

PWRON pin can control ON/OFF of LDO2 and LDO5.





State Machine Diagram in Parts Mode



Note: Each resource turns off by writing the enable bit (LDOnEN / DCnEN bit) to “0”.

LDOnEN (n:1 to 5): bit[4:0] in Add.44h

DCnEN (n:1 to 4): bit[0] in Add. 2Ch / 2Eh / 30h / 32h

GPIO

This IC supports four channels of general-purpose input/output.

GPIO[0-3] pins have the function selected by OTP as shown below.

Name	Function	Input (1,2)	Output (1,2)	Power(3)	GPIO			
					0	1	2	3
N_OE	External power off	N	-	V_{SYS}	√	√	√	√
GPIO0	General purpose I/O	C or N	C or N	V_{SYS} or V_{DDIO}	√	-	-	-
GPIO1	General purpose I/O	C or N	C or N	V_{SYS} or V_{DDIO}	-	√	-	-
GPIO2	General purpose I/O	C or N	C or N	V_{SYS}	-	-	√	-
GPIO3	General purpose I/O	C or N	C or N	V_{SYS}	-	-	-	√
ONOB	PWRON pin monitor	-	N	V_{SYS}	√	√	√	√
PSO0	Power-on signal output function	-	C or N	V_{SYS} or V_{DDIO}	√	-	-	-
PSO1	Power-on signal output function	-	C or N	V_{SYS} or V_{DDIO}	-	√	-	-
PSO2	Power-on signal output function	-	C or N	V_{SYS}	-	-	√	-
PSO3	Power-on signal output function	-	C or N	V_{SYS}	-	-	-	√
LDORTC2	LDORTC2 output	-	A	-	-	-	√	-
LED	LED function	-	N	V_{SYS}	√	√	-	-
PSHOLD	PSHOLD (power-on hold) function	N	-	V_{SYS}	√	√	√	√
ON_EXTIN	External input for on factor	N	-	V_{SYS}	√	√	√	√
LDOnEXON/ DCDCnEXON	External LDOn (n:1 to 5) / DCDCn (n:1 to 4) on/off input	N	-	V_{SYS}	(4)	(4)	(4)	(4)
C32KOUT	32 kHz clock output function	-	C or N	V_{SYS} or V_{DDIO}	√	√	√	√
HRESET	Hard RESET input	N	-	V_{SYS}	√	√	√	√

(1) Explanation of column of “Input” and “Output”:
A: Analog Output.
C: CMOS Input/Output.
N: NMOS Input (V_{SYS} only) / Nch Open-drain Output.

(2) CMOS or Nch is selectable by OTP.

(3) V_{SYS} or V_{DDIO} is selectable by OTP.

(4) Refer to the chapter of Mode.

N_OE function (Supported by GPIO[0-3] pins)

Power-off factor.

Programmable polarity of input signal by OTP.

GPIO function (Supported by GPIO[0-3] pins)

Can be controlled the direction by IOSEL register (output or input).

Output mode: Each output circuit is programmed CMOS or Nch open-drain by OTP.

Input mode: Programmable polarity of input signal by OTP.

Programmable interrupt detection, edge or level by GPEDGE1 / 2 register.

(For the details of interrupt, refer to the interrupt controller and GPIO).

ONOB function (Supported by GPIO[0-3] pins)

Output Low when PWRON pin is pressed.

PSO function (Supported by GPIO[0-3] pins)

Power-on signal output function.

Programmable output timing in the POWERON/POWEROFF sequence by OTP.

Programmable output timing in SLEEP_ENTRY/EXIT sequence by the register.

LDORTC2 output function (Supported by GPIO2 pin)

Output LDORTC2.

LED function (Supported by GPIO[0-1] pins)

Programmable Power On/Off mode or Register mode by register.

Programmable type of flicker by register in Register mode.

For details of type of flicker by register, refer to GPn_LEDMODE register (n:0,1).

Mode	Power State	Type of Flicker
Power On/Off Mode	Power On	Always Turn-on
	Power Off	Always Turn-off
Register Mode	Power On	Depend on GPn_LEDFUNC register

PSHOLD input function (Supported by GPIO[0-3] pins)

Power-on hold and power-off factor.

Hold power-on even if power-on factor de-asserts, when PSHOLD asserts less than 500ms since RESETO is released.

Power-off when PSHOLD de-asserts in power-on.

Programmable polarity of input signal by OTP.

For details of power-on/power-off by PSHOLD, refer to Appendix.

ON_EXTIN input function (Supported by GPIO[0-3] pins)

Power-on factor.

Programmable polarity of input signal by OTP.

LDOnEXON / DCDCnEXON input function (Supported by GPIO[0-3] pins)

DCDC[1-4] / LDO[1-5] on/off control signals.

Refer to the chapter of Mode.

32 kHz clock output function (Supported by GPIO[0-3] pins)

Output 32 kHz clock.

HRESET function (Supported by GPIO[0-3] pins)

Reset (Power OFF - Repower ON) factor.

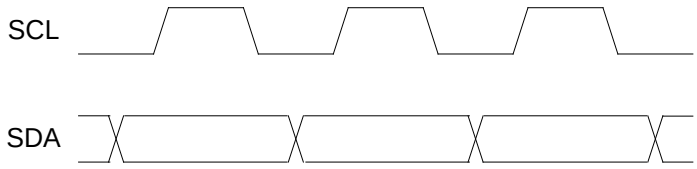
Programmable polarity of input signal by OTP.

I²C-BUS INTERFACE

This IC uses I²C-Bus system for CPU connection through two wires. Connection and transfer system of I²C-Bus are described in the following sections.

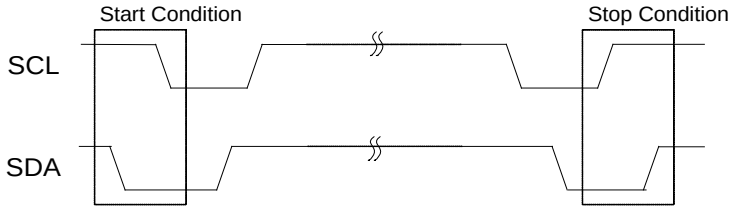
I²C-Bus Operation

Within the procedure of I²C-Bus, unique situations arise which are defined as start and stop conditions.



I²C-Bus Data Transmission

An “High” to “Low” transition on SDA line while SCL is “High” indicates a start condition. A “Low” to “High” transition on SDA line while SCL is “High” defines a stop condition. Start and stop conditions are always generated by master. (Refer to the figure below). It is considered that the bus becomes busy after the start condition and becomes free again a certain time after the stop condition.



AC Characteristics of I²C-Bus

V_{OUTD} = 1.8 V, C_B [(1)] = 400 pF (Max.), unless otherwise specified.
The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

Fast Speed Mode (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-			400	kHz
t_{BUF}	Bus free time between precedent and start	-	1.3		-	µs
t_{Low}	SCL clock time, “low”	-	1.3		-	µs
t_{HIGH}	SCL clock time, “high”	-	0.6		-	µs
$t_{SU;STA}$	Start condition setup time	-	0.6		-	µs
$t_{HD;STA}$	Start condition hold time	-	0.6		-	µs
$t_{SU;STO}$	Stop condition setup time	-	0.6		-	µs
$t_{HD;DAT}$	Data hold time	-	0			µs
$t_{SU;DAT}$	Data setup time	-	100		-	ns
t_R	Rising time of SCL and SDA (Input)	-			300	ns
t_F	Falling time of SCL and SDA (Input)	-			300	ns
t_{SP}	Suppressing pulse width	-	0		50	ns

V_{OUTD} = 1.8 V, C_B [(1)] = 100 pF (Max.), unless otherwise specified.
The specification surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

Hs Mode (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-			3.4	MHz
t_{Low}	SCL clock time, “low”	-	160		-	ns
t_{HIGH}	SCL clock time, “high”	-	60		-	ns
$t_{SU;STA}$	Start condition setup time	-	160		-	ns
$t_{HD;STA}$	Start condition hold time	-	160		-	ns
$t_{SU;STO}$	Stop condition setup time	-	160		-	ns
$t_{HD;DAT}$	Data hold time	-	0		70	ns
$t_{SU;DAT}$	Data setup time	-	10		-	ns
t_{RCL}, t_{FCL}	Rising and falling time of SCL	-	10		40	ns
t_{RDA}, t_{FDA}	Rising and falling time of SDA	-	20		80	ns
t_{SP}	Suppressing pulse width	-	0		10	ns

All the above-mentioned values are corresponding to V_{IH} min and V_{IL} max level.

(1) C_B: Capacitive load for each bus line

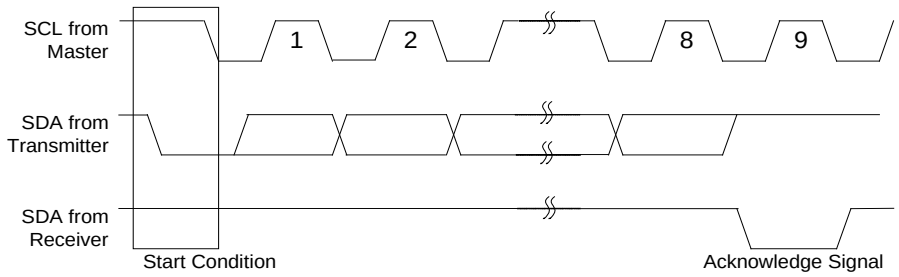
I²C-Bus Data Transmission and its Acknowledge

After start condition, data is transmitted by 1byte (8 bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit.

Data transmission with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases SDA line during the acknowledge clock pulse.

The receiver must pull down SDA line during the acknowledge clock pulse so that SDA line remains stable "Low" during the "High" period of the acknowledge clock pulse.

If a master–receiver is involved in a transfer, it must signal the end of the data to the slave-transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop condition.



I²C-Bus Slave Address

After start condition, a slave address is sent. The address is 7-bit long followed by an 8th bit which is data direction bit (Read/Write). The slave address of this IC is programmable by OTP.

	A7	A6	A5	A4	A3	A2	A1
Slave Address	0	1	1	0	0	1	0

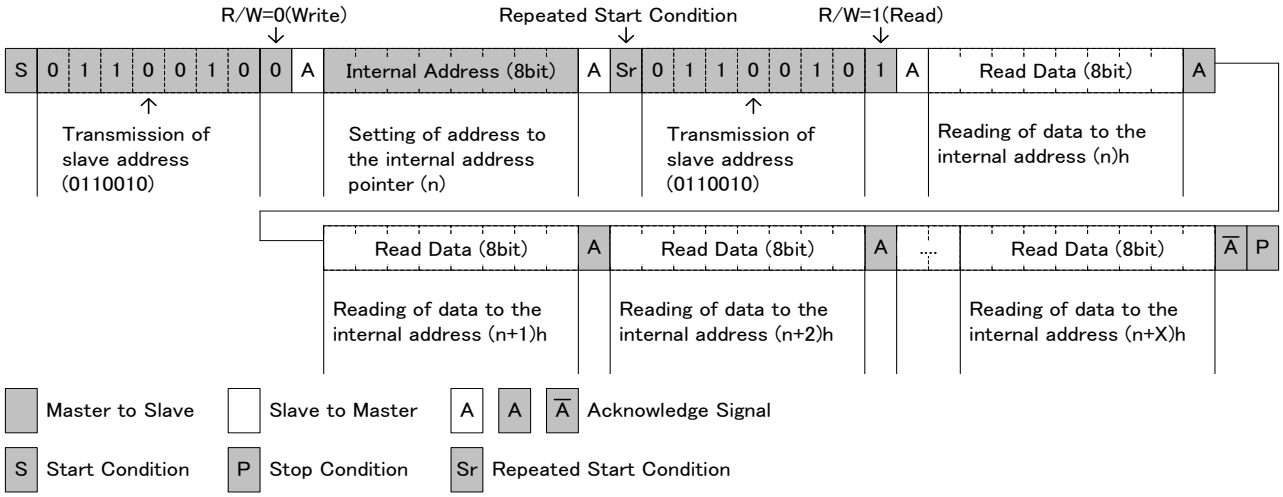
Note: A[3:1] of the slave address are programmable by OTP.

I²C-Bus Data Transmission Read Format (Fast Speed mode)

In order to read the internal register data:

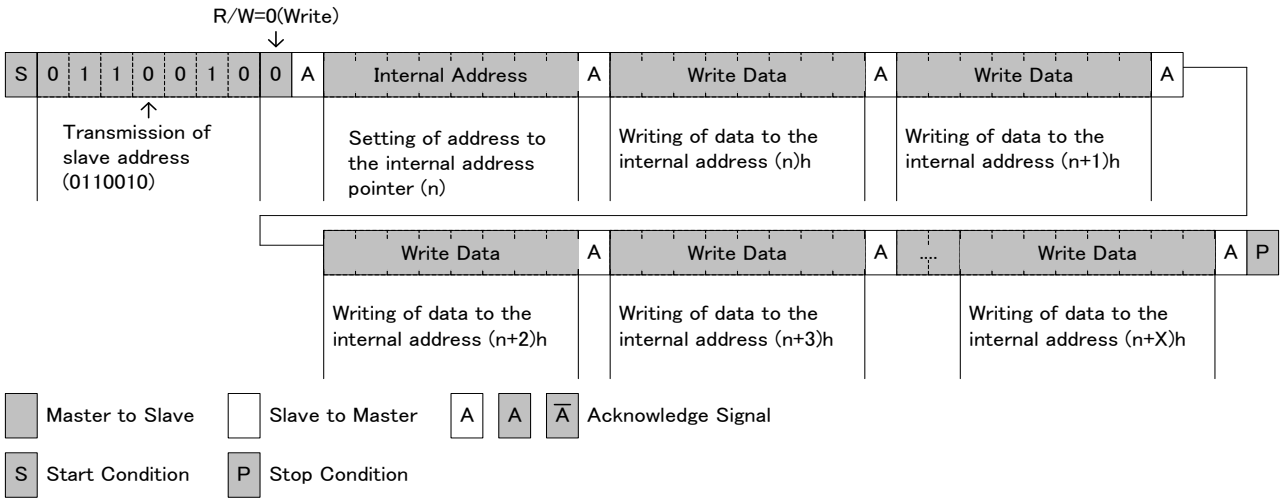
- Specify an internal address pointer (8 bits).
- Generate the repeated start condition to change the data transmission direction to read.

With a start of read mode, automatic increment in address pointers will be made. Read-mode is repeated until stop condition is initiated.

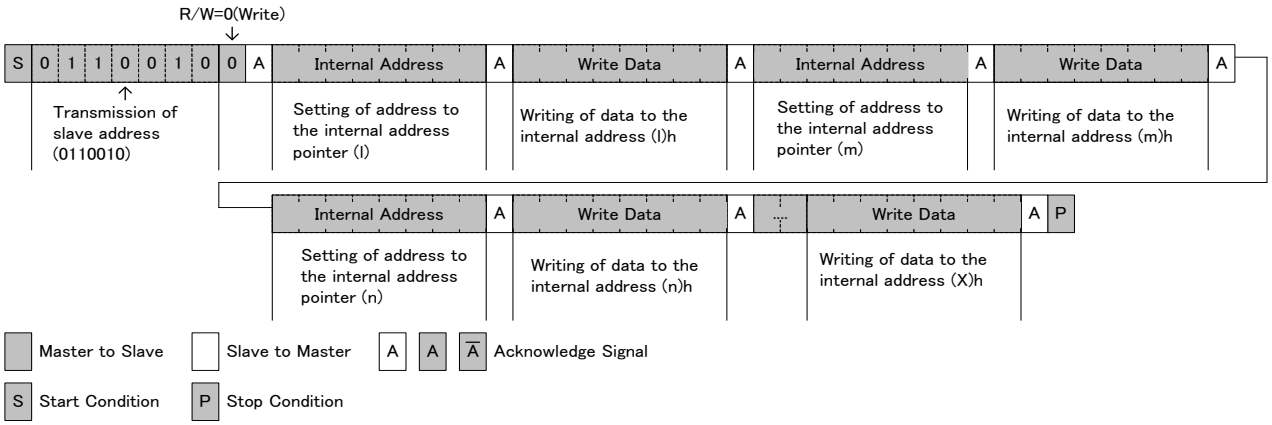


I²C-Bus Data Transmission Write Format (Fast Speed mode)

The transmission format for the slave address allocated to each IC is defined by I²C-Bus standard. However, transmission method of address information of each IC is not defined. This IC transmits command data. For the data transmission, please transmit MSB first from master and following data in sequence.

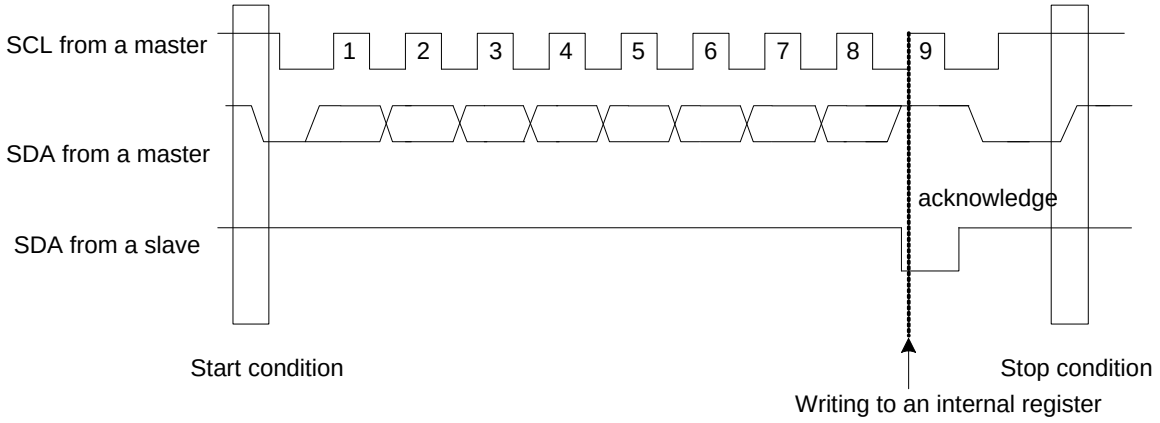


The format which supports the power I²C is shown below.

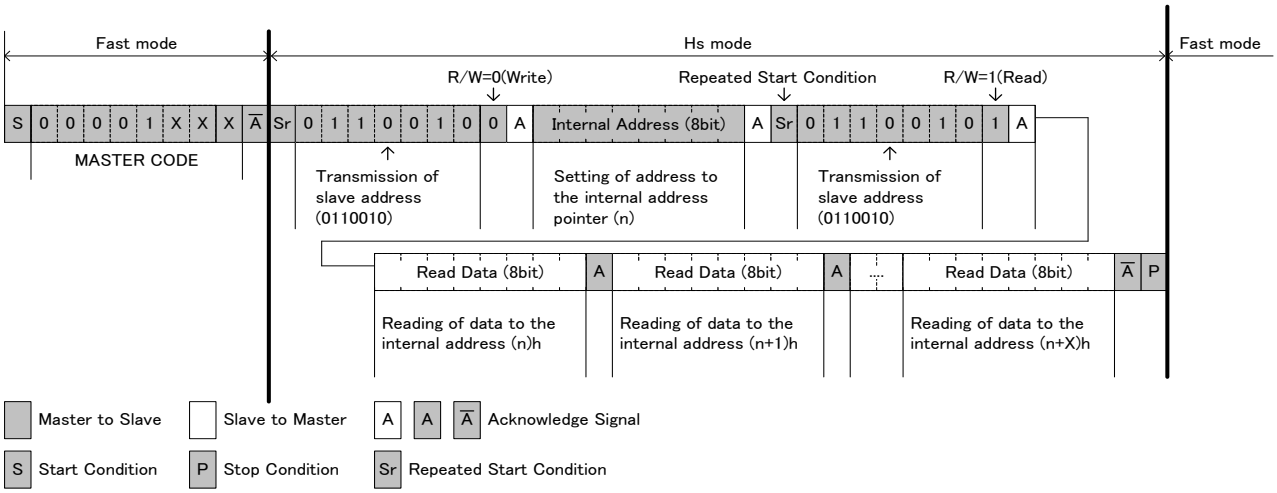


I²C-Bus Data Transmission Write Format (Power I²C)

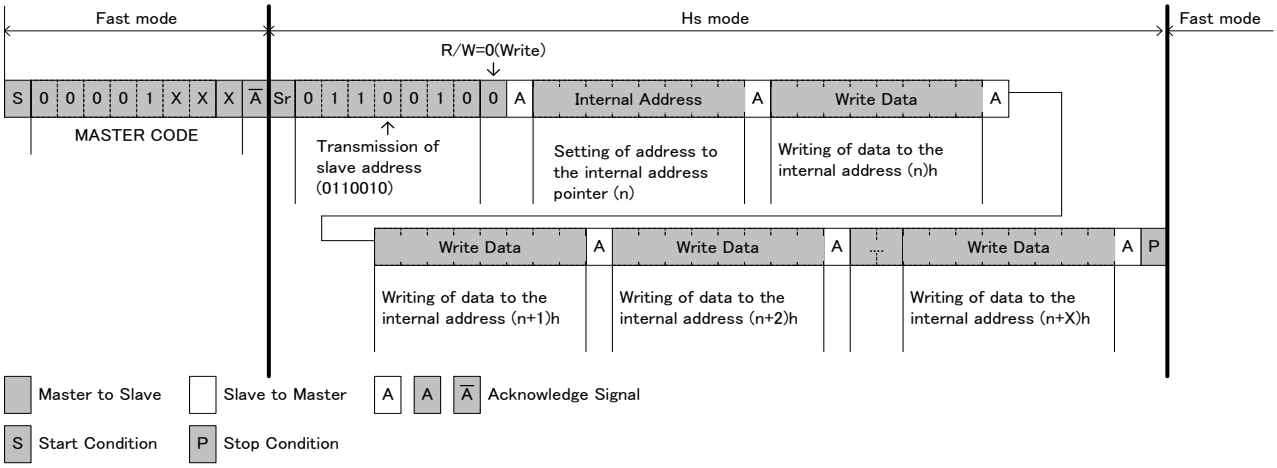
I²C-Bus Internal Register Write-in Timing (Fast Speed mode)



I²C-Bus Data Transmission Read Format (Hs mode)



I²C-Bus Data Transmission Write Format (Hs mode)

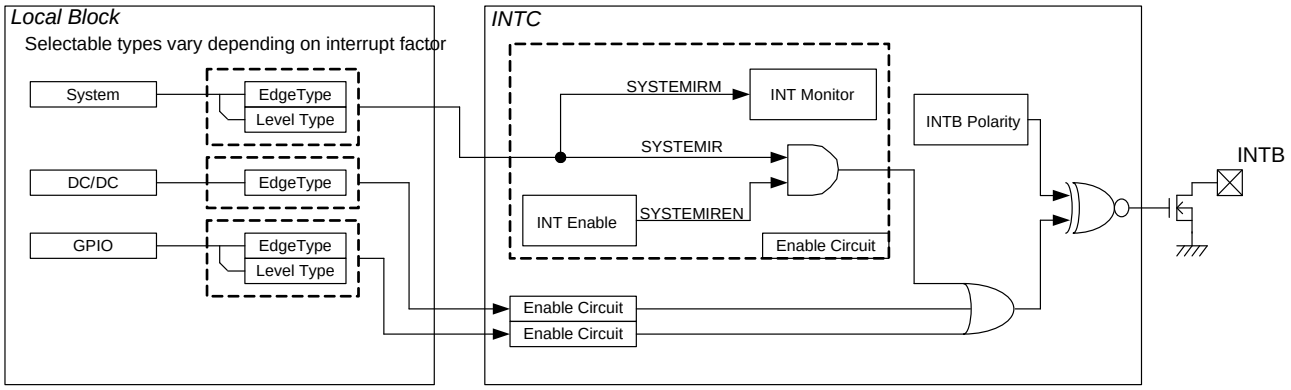


Note: Should have the interval of 100 µs or more at writing and reading the same address.

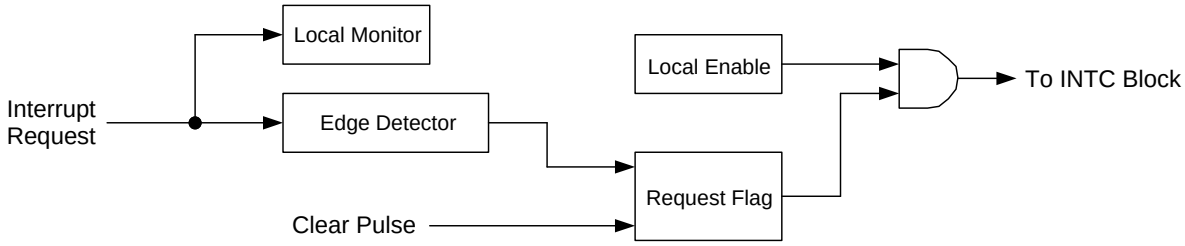
INTERRUPT CONTROLLER (INTC)

This IC has an interrupt controller. CPU can read all the permitted interrupt request flags coming from different functional blocks. When an interrupt occurs, CPU is informed by asserting INTB pin. CPU can identify block and factor which output interrupt by reading Monitor register of INTC and Local Block.

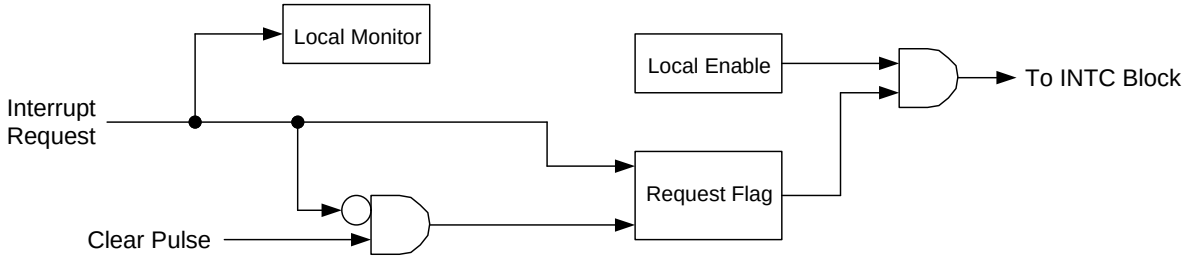
Monitor register is read-only. OR gate signal of each permitted interrupt request flag will be output from INTB pin. CPU can figure out the current state of this IC by reading Monitor register at power-on. To enable interrupt output through INTB pin, it is necessary to write “1” in Enable register.



Edge Type



Level Type



Interrupt Controller Block Diagram

REGISTERS

Registers Map

RSTB: Transition to PWROFF state or Shutdown factor detection

ERSTB: UVLO detection

Notes:

1. Do not set “1” to - bits. Do not write “1” or “0” to undefined registers
2. The default value of green hatch registers is set by the OTP memory (Subsequently referred to as “OTP”).
3. The default value of yellow hatch registers depends on the initial value of the other register programmed in the OTP.

Block	Address	Symbol Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Reset
SYSTEM	00	LSIVER	R	LSIVER[7:0]								01h	---
	01	OTPVER	R	OTPVER[7:0]								by OTP	---
	02	IODAC	R/W	---	---	IODAC[5:0]						by OTP	RSTB
	03	VINDAC	R/W	VINRRESET	---	---	VINHYS	---	VINDAC[2:0]			by OTP	ERSTB(VINRRESET), ERSTB/RSTB(Other)
	04	---	R/W	---	---	---	---	---	---	---	---	00h	RSTB
	05	OUT32KEN	R/W	---	---	---	OUT32KEN3	OUT32KEN2	OUT32KEN1	OUT32KEN0	---	by OTP	RSTB
I2C	06	CPUCNT	R/W	---	---	---	---	---	---	INCB	POWERI2C	00h	RSTB
Power Control	07	PSWR	R/W	RRESET	PSWR[6:0]							00h	ERSTB
	08	---	R	---	---	---	---	---	---	---	---	by OTP	---
	09	PONHIS	R	---	---	---	---	ON_EXTIN PON	---	REPWR PON	PWRON PON	*	ERSTB
	0A	POFFHIS	R	N_OE POFF	DCLIM POFF	WDG POFF	CPU POFF	IODET POFF	VINDET POFF	TSHUT POFF	PWRON POFF	00h	ERSTB
	0B	WATCHDOG	R/W	---	---	---	---	WDOG SLPEN	WDOGEN	WDOGTIM[1:0]		03h	RSTB
	0C	WATCHDOGCNT	R	WATCHDOGCNT[7:0]								*	RSTB
	0D	PWRFUNC	R/W	---	---	SLP_TO_ OFFSEQ	---	---	---	OFFSEQ_ SEL	---	00h	RSTB
	0E	SLPCNT	W	---	---	SLPEXIT	SLPENT	---	---	---	SWPWROFF	00h	RSTB
	0F	REPCNT	R/W	---	---	OFF_RESETO[1:0]		---	REPWRTIM[1:0]		REPWRON	00h	RSTB
	10	PWRONTIMSET	R/W	DIS_OFF_ PWRON_TIM	OFF_PRESS_PWRON[2:0]			OFF_JUDGE_ PWRON	ON_PRESS_PWRON[2:0]			by OTP	RSTB
	11	NOETIMSETCNT	R/W	---	---	---	---	DIS_OFF_ NOE_TIM	OFF_JUDGE_ NOE	OFF_PRESS_NOE[1:0]		05h	RSTB
	12	PWRIREN	R/W	---	EN_ WDOG	EN_ NOE_OFF	EN_ PWRON_OFF	EN_ OVTEMP	EN_ PRVINDT	EN_ EXTIN	EN_ PWRON	00h	RSTB
	13	PWRIRQ	R/W	---	IR_ WDOG	IR_ NOE_OFF	IR_ PWRON_OFF	IR_ OVTEMP	IR_ PRVINDT	IR_ EXTIN	IR_ PWRON	*	RSTB
	14	PWRMON	R	---	---	---	---	MON_ OVTEMP	MON_ PRVINDT	MON_ EXTIN	MON_ PWRON	*	RSTB
	15	PWRIRSEL	R/W	---	---	---	---	SEL_ OVTEMP	SEL_ PRVINDT	SEL_ EXTIN	SEL_ PWRON	0Fh	RSTB
	16	DC1_SLOT	R/W	DC1ONSLOT[3:0]				DC1SLPSLOT[3:0]				by OTP	RSTB
	17	DC2_SLOT	R/W	DC2ONSLOT[3:0]				DC2SLPSLOT[3:0]				by OTP	RSTB
	18	DC3_SLOT	R/W	DC3ONSLOT[3:0]				DC3SLPSLOT[3:0]				by OTP	RSTB
	19	DC4_SLOT	R/W	DC4ONSLOT[3:0]				DC4SLPSLOT[3:0]				by OTP	RSTB
	1A	---	---	---	---	---	---	---	---	---	---	00h	---
	1B	LDO1_SLOT	R/W	LDO1ONSLOT[3:0]				LDO1SLPSLOT[3:0]				by OTP	RSTB
	1C	LDO2_SLOT	R/W	LDO2ONSLOT[3:0]				LDO2SLPSLOT[3:0]				by OTP	RSTB
	1D	LDO3_SLOT	R/W	LDO3ONSLOT[3:0]				LDO3SLPSLOT[3:0]				by OTP	RSTB
	1E	LDO4_SLOT	R/W	LDO4ONSLOT[3:0]				LDO4SLPSLOT[3:0]				by OTP	RSTB
	1F	LDO5_SLOT	R/W	LDO5ONSLOT[3:0]				LDO5SLPSLOT[3:0]				by OTP	RSTB
	20	---	---	---	---	---	---	---	---	---	---	00h	---
	21	---	---	---	---	---	---	---	---	---	---	00h	---
	22	---	---	---	---	---	---	---	---	---	---	00h	---
	23	---	---	---	---	---	---	---	---	---	---	00h	---
	24	---	---	---	---	---	---	---	---	---	---	00h	---
	25	PSO0_SLOT	R/W	PSO0ONSLOT[3:0]				PSO0SLPSLOT[3:0]				by OTP	RSTB
	26	PSO1_SLOT	R/W	PSO1ONSLOT[3:0]				PSO1SLPSLOT[3:0]				by OTP	RSTB
	27	PSO2_SLOT	R/W	PSO2ONSLOT[3:0]				PSO2SLPSLOT[3:0]				by OTP	RSTB
	28	PSO3_SLOT	R/W	PSO3ONSLOT[3:0]				PSO3SLPSLOT[3:0]				by OTP	RSTB
	29	---	---	---	---	---	---	---	---	---	---	00h	---
	2A	LDORTC1_SLOT	R/W	LDORTC1ONSLOT[3:0]				LDORTC1SLPSLOT[3:0]				by OTP	RSTB
	2B	---	R/W	---	---	---	---	---	---	---	---	00h	---

Block	Address	Symbol Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Reset
DCDC	2C	DC1CTL	R/W	DC1MODE_SLP[1:0]		DC1MODE[1:0]		---	---	DC1DIS	DC1EN	by other bit or OTP	RSTB, ERSTB(only DC1DIS)
	2D	DC1CTL2	R/W	reserved		DC1SR[1:0]		---	DC1LIM[1:0]		DC1LIMSDEN	by other bit or OTP	RSTB
	2E	DC2CTL	R/W	DC2MODE_SLP[1:0]		DC2MODE[1:0]		---	---	DC2DIS	DC2EN	by other bit or OTP	RSTB, ERSTB(only DC2DIS)
	2F	DC2CTL2	R/W	reserved		DC2SR[1:0]		---	DC2LIM[1:0]		DC2LIMSDEN	by other bit or OTP	RSTB
	30	DC3CTL	R/W	DC3MODE_SLP[1:0]		DC3MODE[1:0]		---	---	DC3DIS	DC3EN	by other bit or OTP	RSTB, ERSTB(only DC3DIS)
	31	DC3CTL2	R/W	reserved		DC3SR[1:0]		---	DC3LIM[1:0]		DC3LIMSDEN	by other bit or OTP	RSTB
	32	DC4CTL	R/W	DC4MODE_SLP[1:0]		DC4MODE[1:0]		---	---	DC4DIS	DC4EN	by other bit or OTP	RSTB, ERSTB(only DC4DIS)
	33	DC4CTL2	R/W	reserved		DC4SR[1:0]		---	DC4LIM[1:0]		DC4LIMSDEN	by other bit or OTP	RSTB
	34	---	---	---	---	---	---	---	---	---	---	00h	---
	35	---	---	---	---	---	---	---	---	---	---	00h	---
	36	DC1DAC	R/W	DC1DAC[7:0]								by OTP	RSTB
	37	DC2DAC	R/W	DC2DAC[7:0]								by OTP	RSTB
	38	DC3DAC	R/W	DC3DAC[7:0]								by OTP	RSTB
	39	DC4DAC	R/W	DC4DAC[7:0]								by OTP	RSTB
	3A	---	---	---	---	---	---	---	---	---	---	00h	---
	3B	DC1DAC_SLP	R/W	DC1DAC_SLP[7:0]								by other bit or OTP	RSTB
	3C	DC2DAC_SLP	R/W	DC2DAC_SLP[7:0]								by other bit or OTP	RSTB
	3D	DC3DAC_SLP	R/W	DC3DAC_SLP[7:0]								by other bit or OTP	RSTB
	3E	DC4DAC_SLP	R/W	DC4DAC_SLP[7:0]								by other bit or OTP	RSTB
	3F	---	---	---	---	---	---	---	---	---	---	00h	---
	40	DCIREN	R/W	---	---	---	---	EN_ DC4LIM	EN_ DC3LIM	EN_ DC2LIM	EN_ DC1LIM	00h	RSTB
	41	DCIRQ	R/W	---	---	---	---	IR_ DC4LIM	IR_ DC3LIM	IR_ DC2LIM	IR_ DC1LIM	00h	RSTB
	42	DCIRMON	R	---	---	---	---	MON_ DC4LIM	MON_ DC3LIM	MON_ DC2LIM	MON_ DC1LIM	*	RSTB
	43	---	---	---	---	---	---	---	---	---	---	00h	---
LDO	44	LDOEN1	R/W	---	---	---	LDO5EN	LDO4EN	LDO3EN	LDO2EN	LDO1EN	by other bit or OTP	RSTB
	45	LDOEN2	R/W	---	---	LDORTC2EN	LDORTC1EN	---	---	---	---	by OTP	RSTB
	46	LDODIS1	R/W	---	---	---	LDO5DIS	LDO4DIS	LDO3DIS	LDO2DIS	LDO1DIS	1Fh	ERSTB
	47	---	---	---	---	---	---	---	---	---	---	00h	---
	48	---	---	---	---	---	---	---	---	---	---	00h	---
	49	---	---	---	---	---	---	---	---	---	---	00h	---
	4A	---	---	---	---	---	---	---	---	---	---	00h	---
	4B	---	---	---	---	---	---	---	---	---	---	00h	---
	4C	LDO1DAC	R/W	---	LDO1DAC[6:0]							by OTP	RSTB
	4D	LDO2DAC	R/W	---	LDO2DAC[6:0]							by OTP	RSTB
	4E	LDO3DAC	R/W	---	LDO3DAC[6:0]							by OTP	RSTB
	4F	LDO4DAC	R/W	---	LDO4DAC[6:0]							by OTP	RSTB
	50	LDO5DAC	R/W	---	LDO5DAC[6:0]							by OTP	RSTB
	51	---	---	---	---	---	---	---	---	---	---	00h	---
	52	---	---	---	---	---	---	---	---	---	---	00h	---
	53	---	---	---	---	---	---	---	---	---	---	00h	---
	54	---	---	---	---	---	---	---	---	---	---	00h	---
	55	---	---	---	---	---	---	---	---	---	---	00h	---
	56	LDORTC1DAC	R/W	---	LDORTC1DAC[6:0]							by OTP	RSTB
	57	LDORTC2DAC	R/W	---	LDORTC2DAC[6:0]							by OTP	RSTB
	58	LDO1DAC_SLP	R/W	---	LDO1DAC_SLP[6:0]							by OTP	RSTB
	59	LDO2DAC_SLP	R/W	---	LDO2DAC_SLP[6:0]							by OTP	RSTB
	5A	LDO3DAC_SLP	R/W	---	LDO3DAC_SLP[6:0]							by OTP	RSTB
	5B	LDO4DAC_SLP	R/W	---	LDO4DAC_SLP[6:0]							by OTP	RSTB
	5C	LDO5DAC_SLP	R/W	---	LDO5DAC_SLP[6:0]							by OTP	RSTB
	5D	---	---	---	---	---	---	---	---	---	---	00h	---
	5E	---	---	---	---	---	---	---	---	---	---	00h	---
	5F	---	---	---	---	---	---	---	---	---	---	00h	---
	60-8F	---	---	---	---	---	---	---	---	---	---	00h	---
GPIO	90	IOSEL	R/W	---	---	---		IO03	IO02	IO01	IO00	00h	RSTB
	91	IOOUT	R/W	---	---	---		IOOUT03	IOOUT02	IOOUT01	IOOUT00	00h	RSTB
	92	GPEDGE1	R/W	EDGE03[1:0]		EDGE02[1:0]		EDGE01[1:0]		EDGE00[1:0]		00h	RSTB
	93	---	---	---	---	---	---	---	---	---	---	00h	---
	94	EN_GPIR	R/W	---	---	---	---	EN_GP03IR	EN_GP02IR	EN_GP01IR	EN_GP00IR	00h	RSTB
	95	IR_GPR	R/W	---	---	---	---	IR_GP03R	IR_GP02R	IR_GP01R	IR_GP00R	00h	RSTB
	96	IR_GPF	R/W	---	---	---	---	IR_GP03F	IR_GP02F	IR_GP01F	IR_GP00F	00h	RSTB
	97	MON_IOIN	R	---	---	---	---	MON_ IOIN03	MON_ IOIN02	MON_ IOIN01	MON_ IOIN00	*	---
	98	GPLED_FUNC	R/W	---	GP1_LEDMODE	GP1_LEDFUNC[1:0]		---	GP0_LEDMODE	GP0_LEDFUNC[1:0]		by OTP	RSTB
	99	---	R/W	---	---	---	---	---	---	---	---	00h	RSTB
	9A	---	R/W	---	---	---	---	---	---	---	---	00h	RSTB
	9B	---	---	---	---	---	---	---	---	---	---	00h	---
INTC	9C	INTPOL	R/W	---	---	---	---	---	---	---	INTPOL	00h	RSTB
	9D	INTEN	R/W	---	---	---	GPIO IREN	---	---	DCDC IREN	SYSTEM IREN	00h	RSTB
	9E	INTMON	R	---	---	WDG IRM	GPIO IRM	---	---	DCDC IRM	SYSTEM IRM	*	---
	9F	---	---	---	---	---	---	---	---	---	---	00h	---
SYSTEM OPTION	B0	PREVINDAC	R/W	---	---	---	---	---	PREVINDACH	PREVINDAC[1:0]		by OTP	ERSTB
	B1	---	---	---	---	---	---	---	---	---	---	00h	---
	B2	---	---	---	---	---	---	---	---	---	---	00h	---
	B3	---	---	---	---	---	---	---	---	---	---	00h	---
	B4	---	---	---	---	---	---	---	---	---	---	00h	---
	B5	---	---	---	---	---	---	---	---	---	---	00h	---
	B6	---	---	---	---	---	---	---	---	---	---	00h	---
	B7	---	---	---	---	---	---	---	---	---	---	00h	---
	B8	---	---	---	---	---	---	---	---	---	---	00h	---
	B9	---	---	---	---	---	---	---	---	---	---	00h	---
	BA	---	---	---	---	---	---	---	---	---	---	00h	---
	BB	---	---	---	---	---	---	---	---	---	---	00h	---
	BC	OVTEMP	R/W	---	---	---	---	---	---	OVTEMP[1:0]		by OTP	ERSTB
	BD	---	---	---	---	---	---	---	---	---	---	00h	---
	BE	---	---	---	---	---	---	---	---	---	---	00h	---
	BF	---	---	---	---	---	---	---	---	---	---	00h	---
	C0-FF	---	---	---	---	---	---	---	---	---	---	00h	---

SYSTEM

LSIVER: LSI Version Register [Address 00h]

Bit	7	6	5	4	3	2	1	0
Symbol	LSIVER							
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Bit [7: 0]: LSIVER

This register indicates an LSI version.

OTPVER: OTP Version Register [Address 01h]

Bit	7	6	5	4	3	2	1	0
Symbol	OTPVER							
R/W	R	R	R	R	R	R	R	R
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP

Bit [7:0]: OTPVER

This register indicates a version of the OTP.

IODAC: IODET Detection Voltage Setting Register [Address 02h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	IODAC[5:0]					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP

Bit [5:0]: IODAC

Setting the detection voltage to IODET

The initial value of this register depends on the following values programmed in the OTP:
1.4V, 1.6V, 1.85V, 2.1V, 2.35V, 2.6V, 2.85V, 3.1V

IODET Detection Voltage Table (Step = 50mV)

IODAC[5:0]	Detection Voltage [V]
000000 (00h)	Prohibition
⋮	Prohibition
001100(0Ch)	1.40(↓)
⋮	⋮
010000(10h)	1.60(↓)
⋮	⋮
101000(28h)	2.80(↓)
⋮	⋮
110000(30h)	3.20(↓)
⋮	Prohibition
111111(3Fh)	Prohibition

VINDAC: VINDET Detection Voltage Setting Register [Address 03h]

Bit	7	6	5	4	3	2	1	0
Symbol	VINR RESET	-	-	VINHYS	-	VINDAC[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	0	0	By OTP	0	By OTP	By OTP	By OTP

Bit [7]: VINRRESET

Select the reset condition for the VINHYS and the VINDAC registers.

0: RSTB

1: ERSTB

Bit [4]: VINHYS

Setting the hysteresis voltage to VINDET

1: 200mV

0: 500mV

Bit [2:0]: VINDAC

Setting the detection voltage to VINDET

The initial value depends on values programmed in the OTP.

VINDET Detection Voltage Table (Step = 100mV)

VINDAC[2:0]	Detection Voltage [V]
000 (0h)	2.6(↓)
001 (1h)	2.7(↓)
010 (2h)	2.8(↓)
011 (3h)	2.9(↓)
100 (4h)	3.0(↓)
101 (5h)	3.1(↓)
110 (6h)	3.2(↓)
111 (7h)	3.3(↓)

OUT32KEN: C32KOUT Control Register [Address 05h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	OUT32KEN3	OUT32KEN2	OUT32KEN1	OUT32KEN0	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	By OTP	By OTP	By OTP	By OTP	0

This register is available when GPIO[0-3] function as C32KOUT[0-3].

Bit [4]: OUT32KEN3

Select the clock output control bit from GPIO3 (C32KOUT3) pin.
0: Disable
1: Enable

Bit [3]: OUT32KEN2

Select the clock output control bit from GPIO2 (C32KOUT2) pin.
0: Disable
1: Enable

Bit [2]: OUT32KEN1

Select the clock output control bit from GPIO1 (C32KOUT1) pin.
0: Disable
1: Enable

Bit [1]: OUT32KEN0

Select the clock output control bit from GPIO0 (C32KOUT0) pin.
0: Disable
1: Enable

I^2C

CPUCNT: CPUIF Control Register [Address 06h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INCB	POWER I2C
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [1]: INCB

Setting I^2C R/W format (Automatic increment in address pointers)
0: Enable (Automatic increment)
1: Disable

Bit [0]: POWERI2C

Setting power I^2C format
0: Disable
1: Enable

Power Control

PSWR: Power Supply Watch Register [Address 07h]

Bit	7	6	5	4	3	2	1	0
Symbol	RRESET	PSWR						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit [7]: RRESET

Select the reset condition of registers which is reset by RSTB during POWEROFF state.
Writing to this bit is prohibited in Parts Mode.
0: Reset by RSTB
1: Reset by ERSTB

Bit [6:0]: PSWR

This register is reset to “00h” by ERSTB. After this IC powers on, CPU writes some unique value except for “00h”.
Then CPU can recognize whether the register data of the power supply is maintained.

PONHIS: Power-on History Register [Address 09h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ON_EXTIN PON	-	REPWR PON	PWRON PON
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	0	Undefined	Undefined

CPU can recognize the power-on factor by reading this register. The power-on factor is set when the power-on sequence starts.

Bit [3]: ON_EXTINPON

Indicates that the power-on has occurred by detecting ON_EXTIN asserts.

Bit [1]: REPWRPON

Indicates that the repower-on has occurred by the power-off with setting REPWRON bit to 1
Same as repower-on by HRESET.

Bit [0]: PWRONPON

Indicates that the power-on has occurred by detecting PWRON asserts.

POFFHIS: Power-off History Register [Address 0Ah]

Bit	7	6	5	4	3	2	1	0
Symbol	N_OE POFF	DCLIM POFF	WDG POFF	CPU POFF	IODET POFF	VINDET POFF	TSHUT POFF	PWRON POFF
R/W	R	R	R	R	R	R	R	R
Default	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

CPU can recognize the power-off factor by reading this register. The power-off factor is set when the power-off sequence starts or the forcibly powers off.

Bit [7]: N_OEPOFF

Indicates that the power-off has occurred by N_OE asserts or HRESET asserts.

Bit [6]: DCLIMPOFF

Indicates that the power-off has occurred detecting the overcurrent of DCDC[1-4] by the current limit circuit.

Bit [5]: WDGPOFF

Indicates that the power-off has occurred by the watchdog function.

Bit [4]: CPUPOFF

Indicates that the power-off has occurred by the following conditions.

- SWPWROFF bit setting.
- PSHOLD(1) is low.
- PSHOLD(1) is timeout.

Bit [3]: IODETPOFF

Indicates that the power-off has occurred by IODET asserts.

Bit [2]: VINDETPOFF

Indicates that the forced power-off has occurred by detecting the low power condition in VINDET circuit.

Bit [1]: TSHUTPOFF

Indicates that the forced power-off has occurred by detecting an abnormal temperature in the thermal shutdown circuit.

Bit [0]: PWRONPOFF

Indicates that the power-off has occurred by PWRON assert.

(1) GPIO's optional function. Refer to the chapter *"GPIO"* for details.

WATCHDOG: Watchdog Timer Setting Register [Address 0Bh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	WDOG SLPEN	WDOG EN	WDOGTIM	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

The count value of watchdog timer is cleared by Read/Write access to this register.

Bit [3]: WDOGSLPEN

Valid/Invalid the watchdog timer during SLEEP state

0: Invalid (Stop the countdown)

1: Valid (Kept the countdown and generated the interrupt after expiring the timer)

Bit [2]: WDOGEN

Enable/Disable the power-off function by the watchdog timer

Writing to this bit is prohibited in Parts Mode.

0: Disable

1: Enable

This bit can restrict the writing by the OTP. It is whether it is possible to rewrite.

Bit [1:0]: WDOGTIM

Set the access monitoring time from CPU by watchdog timer.

WDOGTIM[1:0]	Timeout [sec]
00	1
01	8
10	32
11	128 (default)

WATCHDOGCNT: Watchdog Timer Count Register [Address 0Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDOGCNT							
R/W	R	R	R	R	R	R	R	R
Default	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit [7:0]: WATCHDOGCNT

Read the count value of watchdog timer.

The read value of this register is determined by the setting of WDOGTIM bits as indicated below.

WDOGTIM[1:0]	WATCHDOGCNT Read Value [msec/bit]
00	25
01	50
10	200
11	800

For example, If the value = 10h (16d) and the WDOGTIM bits = 11b, the power-off sequence starts by watchdog after the (16 × 800 msec + 1 sec).

In order to prevent malfunction of reading operation, read this register twice or more continuously, and if both count value data match, they are determined as the value is read accurately.

PWRFUNC: Power Control Function Register［Address 0Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SLP_TO_OFFSEQ	-	-	-	OFFSEQ_SEL	-
R/W	R	R	R/W	R	R	R	R/W	R
Default	0	0	0	0	0	0	0	0

Bit [5]: SLP_TO_OFFSEQ

Writing "1" to this bit enables this IC to be changed to POWEROFF SEQUENCE by detecting long press of PWRON pin or N_OE pin during SLEEP state. Writing to this bit is prohibited in Parts Mode.

0: Disable

1: Enable

Bit [1]: OFFSEQ_SEL

Power-off sequence timing select bit. Writing to this bit is prohibited in Parts Mode.

0: By ONSLOT registers

1: At Slot_15

SLPCNT: Sleep Control Register [Address 0Eh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SLPEXIT	SLPENT	-	-	-	SWPWR OFF
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Bit [5]: SLPEXIT

During SLEEP state, this IC changes to SLEEP EXIT SEQUENCE state by writing “1” in this bit. Writing to this bit is prohibited in Parts Mode.

Bit [4]: SLPENT

During POWERON state, this IC changes to SLEEP ENTRY SEQUENCE state by writing “1” in this bit. Writing to this bit is prohibited in Parts Mode.

Bit [0]: SWPWROFF

During POWERON state, this IC changes to POWEROFF SEQUENCE state by writing “1” in this bit.

REPCNT: Repower-on Control Register [Address 0Fh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	OFF_RESETO		-	REPWRTIM		RE PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [5:4]: OFF_RESETO

Setting time asserted RESETO pin. Writing to this bit is prohibited in Parts Mode.

OFF_RESETO[1:0]	Time [ms]
00	0 (default)
01	2
10	8
11	16

Bit [2:1]: REPWRTIM

Setting time between the power-off sequence finishes and the power-on sequence starts.

REPWRTIM[1:0]	Time [ms]
00	10 (default)
01	100
10	500
11	1000

Bit [0]: REPWRON

By setting this bit to “1”, this IC powers on after the power-off without the power-on factors. Writing to this bit is prohibited in Parts Mode.
0: Disable
1: Enable

PWRONTIMSET: PWRON Timer Setting Register [Address 10h]

Bit	7	6	5	4	3	2	1	0
Symbol	DIS_OFF_PWRON_TIM	OFF_PRESS_PWRON			OFF_JUDGE_PWRON	ON_PRESS_PWRON		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	by OTP	by OTP	by OTP

Bit [7]: DIS_OFF_PWRON_TIM

Clear and initialize the PWRON off_press timer value and over-flow flag.

0: Enable

1: Disable

Bit [6:4]: OFF_PRESS_PWRON

Setting of PWRON off_press timer. Writing to this bit is prohibited in Parts Mode.

OFF_PRESS_PWRON[2:0]	Timeout [sec]
000	0
001	1
010	2
011	4 (default)
100	6
101	8
110	10
111	12

Bit [3]: OFF_JUDGE_PWRON

Setting of PWRON judge timer. Writing to this bit is prohibited in Parts Mode.

OFF_JUDGE_PWRON	Timeout [sec]
0	0
1	1 (default)

Bit [2:0]: ON_PRESS_PWRON

Setting of PWRON on_press timer. Writing to this bit is prohibited in Parts Mode.

The selectable default times in the OTP are 0ms, 20ms, 1s, and 3s.

ON_PRESS_PWRON[2:0]	Timeout
000	0 ms
001	20 ms
010	128 ms
011	1 sec
100	2 sec
101	3 sec
110	Prohibition
111	Prohibition

NOETIMSET: N_OE Timer Setting Register [Address 11h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	DIS_OFF_NOE_TIM	OFF_JUDGE_NOE	OFF_PRESS_NOE	
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	1

Bit [3]: DIS_OFF_NOE_TIM

Clear and initialize the N_OE off_press timer value and over-flow flag.

0: Enable

1: Disable

Bit [2]: OFF_JUDGE_NOE

Setting of N_OE judge timer.

Writing to this bit is prohibited in Parts Mode.

Note: This bit becomes writable by writing “1” in DIS_OFF_NOE_TIM bit.

OFF_JUDGE_NOE	Timeout [sec]
0	0
1	1 (default)

Bit [1:0]: OFF_PRESS_NOE

Setting of N_OE off_press timer.

Writing to this bit is prohibited in Parts Mode.

Note: These bits become writable by writing “1” in DIS_OFF_NOE_TIM bit.

OFF_PRESS_NOE[1:0]	Timeout [sec]
00	128 ms
01	1 (default)
10	2
11	3

PWRIREN: Power Control Interrupt Factor Output Enable Register [Address 12h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	EN_ WDOG	EN_ NOE_OFF	EN_PWRO N_OFF	EN_ OVTEMP	EN_ PRVINDT	EN_ EXTIN	EN_ PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [6]: EN_WDOG

Enable the interrupt request output in the watchdog timer.
0: Disable
1: Enable
Note: Writing to this bit is prohibited in Parts Mode.

Bit [5]: EN_NOE_OFF

Enable the interrupt request output in the NOE timer.
0: Disable
1: Enable
Note: Power-off by long-press doesn't depend on EN_NOE_OFF bit setting.

Bit [4]: EN_PWRON_OFF

Enable the interrupt request output in the PWRON timer.
0: Disable
1: Enable
Note: Power-off by long-press doesn't depend on EN_PWRON_OFF bit setting.

Bit [3]: EN_OVTEMP

Enable the interrupt request output when detecting overheat temperature.
0: Disable
1: Enable

Bit [2]: EN_PRVINDT

Enable the interrupt request output when the power supply to VSYS is below the VINDET detection voltage.
0: Disable
1: Enable

Bit [1]: EN_EXTIN

Enable the interrupt request output when ON_EXTIN pin input signal changes.
0: Disable
1: Enable

Bit [0]: EN_PWRON

Enable the interrupt request output when PWRON pin input signal changes.
0: Disable
1: Enable

PWRIRQ: Power Control Interrupt Factor Register [Address 13h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	IR_ WDOG	IR_ NOE_OFF	R_PWRON _OFF	IR_ OVTEMP	IR_ PRVINDT	IR_ EXTIN	IR_ PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Each bit can be cleared by writing “0” but cannot be set by writing “1”.

Bit [6]: IR_WDOG

Store the interrupt request factor in the watchdog timer.
0: None
1: Requested

Bit [5]: IR_NOE_OFF

Store the interrupt request factor in the NOE timer.
0: None
1: Requested

Bit [4]: IR_PWRON_OFF

Store the interrupt request factor in the PWRON timer.
0: None
1: Requested

Bit [3]: IR_OVTEMP

Store the interrupt request factor in the detecting overheat temperature.
0: None
1: Requested

Bit [2]: IR_PRVINDT

Store the interrupt request factor in the power supply to VSYS below the VINDET detection voltage.
0: None
1: Requested

Bit [1]: IR_EXTIN

Store the interrupt request factor when ON_EXTIN pin input signal changes.
0: None
1: Requested

Bit [0]: IR_PWRON

Store the interrupt request factor when PWRON pin input signal changes.
0: None
1: Requested

PWRMON: Power Control Interrupt Factor Monitoring Register [Address 14h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON_ OVTEMP	MON_ PRVINDT	MON_ EXTIN	MON_ PWRON
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	Undefined	Undefined	Undefined

Bit [3]: MON_OVTEMP

Monitor a detection state of overheat circuit.
0: Normal temperature
1: Abnormal temperature

Bit [2]: MON_PRVINDT

Monitor the PREVINDET detection signal.
0: Over PREVINDET release voltage
1: Under PREVINDET detection voltage

Bit [1]: MON_EXTIN

Monitor the ON_EXTIN signal.
0: ON_EXTIN deassert
1: ON_EXTIN assert

Bit [0]: MON_PWRON

Monitor the PWRON signal.
0: PWRON is released
1: PWRON is held down

PWRIRSEL: Power Control Interrupt Type Setting Register [Address 15h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEL_ OVTEMP	SEL_ PRVINDT	SEL_ EXTIN	SEL_ PWRON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

For the details of interrupt, refer to the chapter of the interrupt controller (INTC).

Bit [3]: SEL_OVTEMP

Select an interrupt type by the overheat temperature detection.

Bit [2]: SEL_PRVINDT

Select an interrupt type by the Pre-VINDET detection signal.

Bit [1]: SEL_EXTIN

Select an interrupt type by the ON_EXTIN input signal changes.

Bit [0]: SEL_PWRON

Select an interrupt type by the PWRON input signal changes.

SEL_***	Type
0	Level
1	Both-edge

******_SLOT: Power-On/Off and Sleep Entry/Exit Sequence Setting Registers* [Address 16h - 2Ah]**
(*** = DC[1-4], LDO[1-5], LDORTC1, PSO[0-3])

DC1_SLOT [Address 16h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC1ONSLOT				DC1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

DC2_SLOT [Address 17h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC2ONSLOT				DC2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

DC3_SLOT [Address 18h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC3ONSLOT				DC3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

DC4_SLOT [Address 19h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC4ONSLOT				DC4SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDO1_SLOT [Address 1Bh]

Bit	7	6	5	4	3	2	1	0
Symbol	LDO1ONSLOT				LDO1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDO2_SLOT [Address 1Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	LDO2ONSLOT				LDO2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDO3_SLOT [Address 1Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	LDO3ONSLOT				LDO3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDO4_SLOT [Address 1E]

Bit	7	6	5	4	3	2	1	0
Symbol	LDO4ONSLOT				LDO4SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDO5_SLOT [Address 1F]

Bit	7	6	5	4	3	2	1	0
Symbol	LDO5ONSLOT				LDO5SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO0_SLOT [Address 25h]

Bit	7	6	5	4	3	2	1	0
Symbol	PSO0ONSLOT				PSO0SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO1_SLOT [Address 26h]

Bit	7	6	5	4	3	2	1	0
Symbol	PSO1ONSLOT				PSO1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO2_SLOT [Address 27h]

Bit	7	6	5	4	3	2	1	0
Symbol	PSO2ONSLOT				PSO2SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

PSO3_SLOT [Address 28h]

Bit	7	6	5	4	3	2	1	0
Symbol	PSO3ONSLOT				PSO3SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

LDORTC1_SLOT [Address 2Ah]

Bit	7	6	5	4	3	2	1	0
Symbol	LDORTC1ONSLOT				LDORTC1SLPSLOT			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	by OTP	by OTP	by OTP	by OTP	1	1	1	1

Bit [7:4]: ***ONSLOT (*** = DC[1-4], LDO[1-5], LDORTC1, PSO[0-3])

Setting on/off timing in the power-on/off sequence

Bit [3:0]: ***SLPSLOT (*** = DC[1-4], LDO[1-5], LDORTC1, PSO[0-3])

Setting on/off timing in the sleep entry/exit sequence

The following restrictions exist. If the value of DCnONSLOT (n:1 to 4) / LDOnONSLOT (n:1 to 5) register is “Fh”, the control of DCDCnEXON / LDOnEXON pin is disabled in Parts Mode.

***SLOT[3:0]	Power-on/off sequence timing slot number (***ONSLOT)	Sleep entry/exit sequence timing slot number (***SLPSLOT)
0000	Power-on/off Slot _0 (S0)	Sleep Slot _0 (SS0)
0001	Power-on/off Slot _1 (S1)	Sleep Slot _1 (SS1)
0010	Power-on/off Slot _2 (S2)	Sleep Slot _2 (SS2)
0011	Power-on/off Slot _3 (S3)	Sleep Slot _3 (SS3)
⋮	⋮	⋮
1011	Power-on/off Slot _11 (S11)	Sleep Slot _11 (SS11)
1100	Power-on/off Slot _12 (S12)	Sleep Slot _12 (SS12)
1101	Power-on/off Slot _13 (S13)	Sleep Slot _13 (SS13)
1110	Power-on/off Slot _14 (S14)	Sleep Slot _14 (SS14)
1111	Default Off	The state in POWERON state is maintained.

DCDC

DC1CTL: DCDC1 Control Register [Address 2Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	DC1MODE_SLP[1:0]		DC1MODE[1:0]		-	-	DC1DIS	DC1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit [7:6]: DC1MODE_SLP[1:0]

DCDC1 mode setting bit at the SLEEP state

DC1MODE_SLP [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [5:4]: DC1MODE[1:0]

DCDC1 mode setting bit at the POWERON state

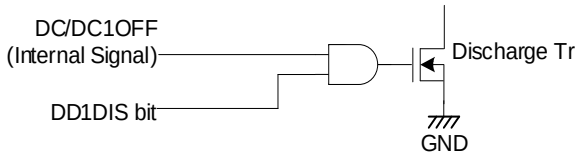
DC1MODE [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [1]: DC1DIS

DCDC1 discharge control bit. When DCDC1 is enabled, this bit becomes invalid even if set to “1”.

0: Off

1: On



Bit [0]: DC1EN

DCDC1 enable bit

0: Disable

1: Enable

The initial value of this register depends on the initial value of DC1ONSLOT register and Mode setting that are programmed in the OTP.

<Normal Mode> DC1ONSLOT = Fh: DC1EN = 0b

DC1ONSLOT = 0h-Eh: DC1EN = 1b

<Parts Mode> DC1EN = 1b

DC1CTL2: DCDC1 Control2 Register [Address 2Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC1SR[1:0]		-	DC1LIM[1:0]		DC1 LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit [7:6]: (reserved)

These bits are reserved. Writing these bits are prohibited.

Bit [5:4]: DC1SR

DCDC1 ramp rate of output voltage setting bit

DC1SR[1:0]	Voltage Slope [mV/ µs]
00	14 (default)
01	7
10	3.5
11	Prohibition

Note: Writing this register is prohibited during the ramp control.

Bit [2:1]: DC1LIM

DCDC1 minimum current limit setting bit

DC1LIM[1:0]	Current Limit [A]
00	No Limit
01	3.2
10	3.7
11	4.0

The default current can be set up all the above register values by the OTP.

Bit [0]: DC1LIMSDEN

Enable shutdown function from the current limit detection of DCDC1.

The current limit detection is to continue exceeding limit current during 2ms.

0: Disable

1: Enable

The initial value of this register depends on Mode setting that is programmed in the OTP.

<Normal Mode> DC1LIMSDEN = 1b

<Parts Mode> DC1LIMSDEN = 0b

DC2CTL: DCDC2 Control Register [Address 2Eh]

Bit	7	6	5	4	3	2	1	0
Symbol	DC2MODE_SLP[1:0]		DC2MODE[1:0]		-	-	DC2DIS	DC2EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit [7:6]: DC2MODE_SLP[1 :0]

DCDC2 mode setting bit at the SLEEP state

DC2MODE_SLP [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [5:4]: DC2MODE[1 :0]

DCDC2 mode setting bit at the POWERON state

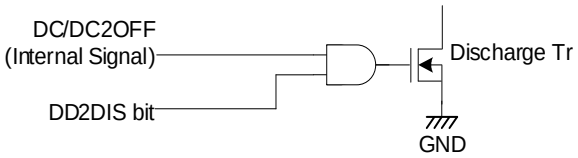
DC2MODE [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [1]: DC2DIS

DCDC2 discharge control bit. When DCDC2 is enabled, this bit becomes invalid even if set to “1”.

0: Off

1: On



Bit [0]: DC2EN

DCDC2 enable bit

0: Disable

1: Enable

The initial value of this register depends on the initial value of DC2ONSLOT register and Mode setting that are programmed in the OTP.

<Normal Mode> DC2ONSLOT = Fh: DC2EN = 0b

DC2ONSLOT = 0h-Eh: DC2EN = 1b

<Parts Mode>

DC2EN = 1b

DC2CTL2: DCDC2 Control2 Register [Address 2Fh]

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC2SR[1:0]		-	DC2LIM[1:0]		DC2 LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit [7:6]: (reserved)

These bits are reserved. Writing these bits are prohibited.

Bit [5:4]: DC2SR

DCDC2 ramp rate of output voltage setting bit

DC2SR[1:0]	Voltage Slope [mV/µs]
00	14 (default)
01	7
10	3.5
11	Prohibition

Note: Writing this register is prohibited during the ramp control.

Bit [2:1]: DC2LIM

DCDC2 minimum current limit setting bit

DC2LIM[1:0]	Current Limit [A]
00	No Limit
01	3.2
10	3.7
11	4.0

The default current can be set up all of the above register values by the OTP.

Bit [0]: DC2LIMSDEN

Enable shutdown function from the current limit detection of DCDC2.

The current limit detection is to continue exceeding limit current during 2ms.

0: Disable
1: Enable

The initial value of this register depends on Mode setting that is programmed in the OTP.

<Normal Mode> DC2LIMSDEN = 1b

<Parts Mode> DC2LIMSDEN = 0b

DC3CTL: DCDC3 Control Register [Address 30h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC3MODE_SLP[1:0]		DC3MODE[1:0]		-	-	DC3DIS	DC3EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit [7:6]: DC3MODE_SLP[1 :0]

DCDC3 mode setting bit at the SLEEP state

DC3MODE_SLP [1:0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [5:4]: DC3MODE[1 :0]

DCDC3 mode setting bit at the POWERON state

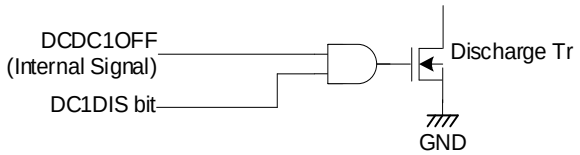
DC3MODE [1:0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [1]: DC3DIS

DCDC3 discharge control bit. When DCDC3 is enabled, this bit becomes invalid even if set to “1”.

0: Off

1: On



Bit [0]: DC3EN

DCDC3 enable bit

0: Disable

1: Enable

The initial value of this register depends on the initial value of DC3ONSLOT register and Mode setting that are programmed in the OTP.

<Normal Mode> DC3ONSLOT = Fh: DC3EN = 0b

DC3ONSLOT = 0h-Eh: DC3EN = 1b

<Parts Mode> DC3EN = 1b

DC3CTL2: DCDC3 Control2 Register [Address 31h]

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC3SR[1:0]		-	DC3LIM[1:0]		DC3 LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit [7:6]: (reserved)

These bits are reserved. Writing these bits are prohibited.

Bit [5:4]: DC3SR

DCDC3 ramp rate of output voltage setting bit

DC3SR[1:0]	Voltage Slope [mV/µs]
00	14 (default)
01	7
10	3.5
11	Prohibition

Note: Writing this register is prohibited during the ramp control.

Bit [2:1]: DC3LIM

DCDC3 minimum current limit setting bit

DC3LIM[1:0]	Current Limit [A]
00	No Limit
01	2.3
10	2.8
11	3.2

The default current can be set up all the above register values by the OTP.

Bit [0]: DC3LIMSDEN

Enable shutdown function from the current limit detection of DCDC3.

The current limit detection is to continue exceeding limit current during 2ms.

0: Disable

1: Enable

The initial value of this register depends on Mode setting that is programmed in the OTP.

<Normal Mode> DC3LIMSDEN = 1b

<Parts Mode> DC3LIMSDEN = 0b

DC4CTL: DCDC4 Control Register [Address 32h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC4MODE_SLP[1:0]		DC4MODE[1:0]		-	-	DC4DIS	DC4EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	By OTP

Bit [7:6]: DC4MODE_SLP[1:0]

DCDC4 mode setting bit at the SLEEP state

DC4MODE_SLP [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [5:4]: DC4MODE[1:0]

DCDC4 mode setting bit at the POWERON state

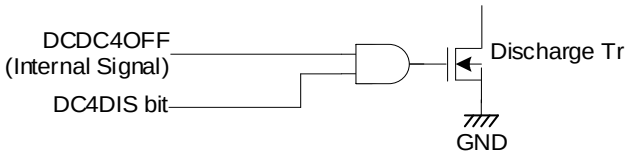
DC4MODE [1 :0]	Description
00	Auto mode
01	PWM mode
10	PSM mode
11	Auto mode

Bit [1]: DC4DIS

DCDC4 discharge control bit. When DCDC4 is enabled, this bit becomes invalid even if set to “1”.

0: Off

1: On



Bit [0]: DC4EN

DCDC4 enable bit

0: Disable

1: Enable

The initial value of this register depends on the initial value of DC4ONSLOT register and Mode setting that are programmed in the OTP.

<Norma Mode> DC4ONSLOT = Fh: DC4EN = 0b

DC4ONSLOT = 0h-Eh: DC4EN = 1b

<Parts Mode> DC4EN = 1b

DC4CTL2: DCDC4 Control2 Register [Address 33h]

Bit	7	6	5	4	3	2	1	0
Symbol	(reserved)		DC4SR[1:0]		-	DC4LIM[1:0]		DC4 LIMSDEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	0	0	0	By OTP	By OTP	By OTP

Bit [7:6]: (reserved)

These bits are reserved. Writing these bits are prohibited.

Bit [5:4]: DC4SR

DCDC4 ramp rate of output voltage setting bit

DC4SR[1:0]	Voltage Slope [mV/µs]
00	14 (default)
01	7
10	3.5
11	Prohibition

Note: Writing this register is prohibited during the ramp control.

Bit [2:1]: DC4LIM

DCDC4 minimum current limit setting bit

DC4LIM[1:0]	Current Limit [A]
00	No Limit
01	2.3
10	2.8
11	3.2

The default current can be set up all the above register values by the OTP.

Bit [0]: DC4LIMSDEN

Enable shutdown function from the current limit detection of DCDC4.

The current limit detection is to continue exceeding limit current during 2ms.

0: Disable

1: Enable

The initial value of this register depends on Mode setting that is programmed in the OTP.

<Normal Mode> DC4LIMSDEN = 1b

<Parts Mode> DC4LIMSDEN = 0b

DC1DAC: DCDC1 Output Voltage Control Register [Address 36h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC1DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC2DAC: DCDC2 Output Voltage Control Register [Address 37h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC2DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC3DAC: DCDC3 Output Voltage Control Register [Address 38h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC3DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC4DAC: DCDC4 Output Voltage Control Register [Address 39h]

Bit	7	6	5	4	3	2	1	0
Symbol	DC4DAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DCDC[1-4] Output Voltage Table (Step = 12.5 mV)

DCnDAC[7:0]	Output Voltage [V]
0000000 (00h)	0.6000
⋮	⋮
0011000 (18h)	0.9000
⋮	⋮
1011100 (5Ch)	1.7500
⋮	⋮
11101000 (E8h)	3.5000
⋮	Prohibition
11111111 (FFh)	Prohibition

The default voltage can be set up from 0.6V to 3.5V at 50mV/step that is programmed in the OTP.

DC1DAC_SLP: DCDC1 Output Voltage Control Register in Sleep [Address 3Bh]

Bit	7	6	5	4	3	2	1	0
Symbol	DC1DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC2DAC_SLP: DCDC2 Output Voltage Control Register in Sleep [Address 3Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	DC2DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC3DAC_SLP: DCDC3 Output Voltage Control Register in Sleep [Address 3Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	DC3DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DC4DAC_SLP: DCDC4 Output Voltage Control Register in Sleep [Address 3Eh]

Bit	7	6	5	4	3	2	1	0
Symbol	DC4DAC_SLP[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0	0

DCDC[1-4] Output Voltage Table (Step = 12.5 mV)

DCnDAC_SLP[7:0]	Output Voltage [V]
0000000 (00h)	0.6000
⋮	⋮
0011000 (18h)	0.9000
⋮	⋮
1011100 (5Ch)	1.7500
⋮	⋮
11101000 (E8h)	3.5000
⋮	Prohibition
11111111 (FFh)	Prohibition

The default voltage is set to the value in the DCnDAC register (n: 1 to 4).

DCIREN: DCDC Interrupt Enable Register [Address 40h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EN_ DC4LIM	EN_ DC3LIM	EN_ DC2LIM	EN_ DC1LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [3:0]: EN_DCnLIM (n:1 to 4)

DCDCn current limit interrupt enable bit

0: Disable
1: Enable

DCIRQ: DCDC Interrupt Flag Register [Address 41h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ DC4LIM	IR_ DC3LIM	IR_ DC2LIM	IR_ DC1LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Note: Each bit can be cleared by writing “0” but cannot be set by writing “1”.

Bit [3:0]: IR_DCnLIM (n:1 to 4)

DCDCn current limit flag bit

0: None
1: Requested

DCIRMON: DCDC Interrupt Monitor Register [Address 42h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON _ DC4LIM	MON _ DC3LIM	MON _ DC2LIM	MON _ DC1LIM
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [3:0]: MON_DCnLIM (n:1 to 4)

DCDCn current limit interrupt monitor bit

0: Undetected
1: Detected

LDO

LDOEN1: LDOs On / Off Control Register [Address 44h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	LDO5EN	LDO4EN	LDO3EN	LDO2EN	LDO1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	By OTP	By OTP	By OTP	By OTP	By OTP

Bit [4:0]: LDOnEN (n:1 to 5)

LDOn on/off control bit
0: Off
1: On

The initial value of this register depends on the initial value of the LDOnONSLOT register and Mode setting that are programmed in the OTP.

<Normal Mode> LDOnONSLOT = Fh: LDOnEN = 0b
LDOnONSLOT = 0h-Eh: LDOnEN = 1b
<Parts Mode> LDOnEN = 1b

LDOEN2: LDOs On / Off Control Register [Address 45h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	LDORTC2EN *1	LDORTC1EN *2	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	By OTP	By OTP	0	0	0	0

Bit [5:4]: LDORTCnEN (n:1,2)

LDOn on/off control bit
0: Off
1: On

Notes:

*1 Writing to this bit is prohibited when GPIO2 pin is not set as LDORTC2 output.

*2 The initial value of this register depends on the initial value of LDORTC1ONSLOT register, Mode setting and Always-on setting that are programmed in the OTP.

<Always-on> LDORTC1EN = 1b (without regard to the mode setting)
<Normal Mode> LDORTC1ONSLOT = Fh: LDORTC1EN = 0b
LDORTC1ONSLOT = 0h-Eh: LDORTC1EN = 1b

LDODIS: LDOs On / Off Control Register [Address 46h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	LDO5DIS	LDO4DIS	LDO3DIS	LDO2DIS	LDO1DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	1	1	1

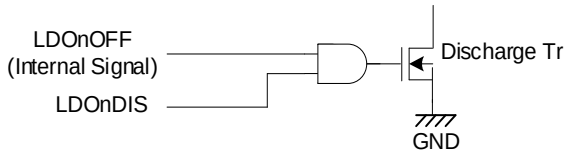
Bit [4:0]: LDOnDIS (n:1 to 5)

LDOn discharge Tr on/off control bit.

When LDOn is enabled, this bit becomes invalid even if set to “1”.

0: Off

1: On



LDO1DAC: LDO1 Output Voltage Control Register [Address 4Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO1DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO2DAC: LDO2 Output Voltage Control Register [Address 4Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO2DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO1-2 Output Voltage Table (Step = 50 mV)

LDOnDAC[6:0]	Output Voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
⋮	⋮
0100100 (24h)	1.800
⋮	⋮
1101000 (68h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage can be set up in the range from 0.9V to 3.5V (in 50mV step) that are programmed in the OTP.

LDO3DAC: LDO3 Output Voltage Control Register [Address 4Eh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO3DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO3 Output Voltage Table (Step = 50 mV)

LDO3DAC[6:0]	Output Voltage [V]
0000000 (00h)	0.600
0000010 (02h)	0.650
⋮	⋮
0110000 (30h)	1.800
⋮	⋮
1110100 (74h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage can be set up in the range from 0.6V to 3.5V (in 50mV step) that are programmed in the OTP.

LDO4DAC: LDO4 Output Voltage Control Register [Address 4Fh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO4DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO5DAC: LDO5 Output Voltage Control Register [Address 50h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO5DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO4-5 Output Voltage Table (Step = 50 mV)

LDOnDAC[6:0]	Output Voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
⋮	⋮
0100100 (24h)	1.800
⋮	⋮
1101000 (68h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage can be set up in the range from 0.9V to 3.5V (in 50mV step) that are programmed in the OTP.

LDORTCDAC: LDORTC Output Voltage Control Register [Address 56h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDORTCDAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDORTC Output Voltage Table (Step = 50 mV)

LDORTCDAC[6:0]	Output Voltage [V]
0000000 (00h)	1.200
0000010 (02h)	1.250
⋮	⋮
0011000 (18h)	1.800
⋮	⋮
1011100 (5Ch)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage can be set up in the range from 1.2V to 3.5V (in 50mV step) that are programmed in the OTP.

LDORTC2DAC: LDORTC2 Output Voltage Control Register [Address 57h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDORTC2DAC						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LCORTC2 Output Voltage Table (Step = 50 mV)

LDORTC2DAC[6:0]	Output Voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
⋮	⋮
0100100 (24h)	1.800
⋮	⋮
1101000 (68h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage can be set up in the range from 0.9V to 3.5V (in 50mV step) that are programmed in the OTP.

LDO1DAC_SLP: LDO1 Output Voltage Control Register in Sleep [Address 58h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO1DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO2DAC_SLP: LDO2 Output Voltage Control Register in Sleep [Address 59h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO2DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO[1-2] Output Voltage Table (Step = 50 mV)

LDOnDAC_SLP[6:0]	Output Voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
⋮	⋮
0100100 (24h)	1.800
⋮	⋮
1101000 (68h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage is set to the value in the LDOnDAC register (n:1, 2).

LDO3DAC_SLP: LDO3 Output Voltage Control Register in Sleep [Address 5Ah]

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO3DAC_SLP[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO3 Output Voltage Table (Step = 50 mV)

LDO3DAC_SLP[6:0]	Output Voltage [V]
0000000 (00h)	0.600
0000010 (02h)	0.650
⋮	⋮
0110000 (30h)	1.800
⋮	⋮
1110100 (74h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage is set to the value in the LDO3DAC register.

LDO4DAC_SLP: LDO4 Output Voltage Control Register in Sleep [Address 5Bh]

Bit	7	6	5	4	3	2	1	0
Symbol	-				LDO4DAC_SLP[6:0]			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO5DAC_SLP: LDO5 Output Voltage Control Register in Sleep [Address 5Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	-				LDO5DAC_SLP[6:0]			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	By OTP	By OTP	By OTP	By OTP	By OTP	By OTP	0

LDO[4-5] Output Voltage Table (Step = 50 mV)

LDOnDAC_SLP[6:0]	Output Voltage [V]
0000000 (00h)	0.900
0000010 (02h)	0.950
⋮	⋮
0100100 (24h)	1.800
⋮	⋮
1101000 (68h)	3.500
⋮	Prohibition
1111110 (7Eh)	Prohibition

The default voltage is set to the value in the LDOnDAC register (n:4, 5).

GPIO

IOSEL: GPIO Direction Setting Register [Address 90h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IO03	IO02	IO01	IO00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

IOSEL register can set the input/output of GPIO pin. Writing “0” in the register, the corresponding pin becomes input pin, and becomes output pin when writing “1”.

Bit	Symbol	R/W	Function	1	0	Initial Value
3	IO03	R/W	GPI03 Direction Setting bit	Output	Input	0
2	IO02	R/W	GPI02 Direction Setting bit	Output	Input	0
1	IO01	R/W	GPI01 Direction Setting bit	Output	Input	0
0	IO00	R/W	GPI00 Direction Setting bit	Output	Input	0

Notes:

1. IO0[3-0] are invalid when PSO mode.
2. PSO: Power-on Signal Output for the external devices.

IOOUT: GPIO Output Signal Register [Address 91h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IOOUT03	IOOUT02	IOOUT01	IOOUT00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

IOOUT register can set “Low” or "Hi-Z" of GPIO pin when GP pin is set as output.
By writing “0” in IOOUT register, the corresponding pin outputs “Low” and becomes “Hi-z” by writing “1”.

Bit	Symbol	R/W	Function	1	0	Initial Value
3	IOOUT03	R/W	GPI03 Output Setting bit	High	Low	0
2	IOOUT02	R/W	GPI02 Output Setting bit	High	Low	0
1	IOOUT01	R/W	GPI01 Output Setting bit	High	Low	0
0	IOOUT00	R/W	GPI00 Output Setting bit	High	Low	0

Notes:

1. Valid only in the output mode.
2. When the output circuit is set as Nch open-drain by the OTP, the output of GP pin becomes not “High” but “Hi-z”.

GPEDGE1: GPIO Interrupt Detection Type Setting Register [Address 92h]

Bit	7	6	5	4	3	2	1	0
Symbol	EDGE03		EDGE02		EDGE01		EDGE00	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

GPEDGE register can set GPIO interrupt detection type.

Bit	Symbol	R/W	Function	1	0	Initial Value
7-6	EDGE03	R/W	GPI03 Interrupt Detection Type Setting bit	As below		00
5-4	EDGE02	R/W	GPI02 Interrupt Detection Type Setting bit	As below		00
3-2	EDGE01	R/W	GPI01 Interrupt Detection Type Setting bit	As below		00
1-0	EDGE00	R/W	GPI00 Interrupt Detection Type Setting bit	As below		00

EDGE0x [1:0]	Detection Function
00	Level (default)
01	Rising Edge
10	Falling Edge
11	Both Edge

EN_GPIR: Interrupt Enable Register [Address 94h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EN_ GP03IR	EN_ GP02IR	EN_ GP01IR	EN_ GP00IR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Writing “1” enables the interrupt request.

Bit	Symbol	R/W	Function	1	0	Initial Value
3	EN_GP03IR	R/W	GPI03 interrupt enable bit	Enable	Disable	0
2	EN_GP02IR	R/W	GPI02 interrupt enable bit	Enable	Disable	0
1	EN_GP01IR	R/W	GPI01 interrupt enable bit	Enable	Disable	0
0	EN_GP00IR	R/W	GPI00 interrupt enable bit	Enable	Disable	0

IR_GPR: Rising Edge Interrupt Request Register [Address 95h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ GP03R	IR_ GP02R	IR_ GP01R	IR_ GP00R
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

In the rising edge or both edge mode, IR_GPR register can monitor the interrupt request of rising edge. The register is cleared by writing "0" in the corresponding bit but cannot be set by writing "1".
The function above-mentioned is operated in level mode as well. However, it cannot be cleared while the interrupt request signal is "High".

Bit	Symbol	R/W	Function	1	0	Initial Value
3	IR_GP03R	R/W	GPI03 Rising Edge Interrupt Request bit	Requested	None	0
2	IR_GP02R	R/W	GPI02 Rising Edge Interrupt Request bit	Requested	None	0
1	IR_GP01R	R/W	GPI01 Rising Edge Interrupt Request bit	Requested	None	0
0	IR_GP00R	R/W	GPI00 Rising Edge Interrupt Request bit	Requested	None	0

IR_GPF: Falling Edge Interrupt Request Register [Address 96h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IR_ GP03F	IR_ GP02F	IR_ GP01F	IR_ GP00F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

In the falling edge or both edge mode, IR_GPF can monitor the interrupt request of falling edge. It is cleared by writing "0" corresponding bit but cannot be set by writing "1".

Bit	Symbol	R/W	Function	1	0	Initial Value
3	IR_GP03F	R/W	GPI03 Falling Edge Interrupt Request bit	Requested	None	0
2	IR_GP02F	R/W	GPI02 Falling Edge Interrupt Request bit	Requested	None	0
1	IR_GP01F	R/W	GPI01 Falling Edge Interrupt Request bit	Requested	None	0
0	IR_GP00F	R/W	GPI00 Falling Edge Interrupt Request bit	Requested	None	0

MON_IOIN: GPIO Input Signal Read Register [Address 97h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MON_ IOIN03	MON_ IOIN02	MON_ IOIN01	MON_ IOIN00
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	Undefined	Undefined	Undefined	Undefined

MON_IOIN register can monitor the debounced signal from GP pin.

Bit	Symbol	R/W	Function	1	0	Initial Value
3	MON_IOIN03	R	GPI03 input status bit	High	Low	-
2	MON_IOIN02	R	GPI02 input status bit	High	Low	-
1	MON_IOIN01	R	GPI01 input status bit	High	Low	-
0	MON_IOIN00	R	GPI00 input status bit	High	Low	-

GPLED_FUNC: LED Function Setting Register [Address 98h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	GP1_LED MODE	GP1_LEDFUNC[1:0]		-	GP0_LED MODE	GP0_LEDFUNC[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	By OTP	0	0	0	By OTP	0	0

When set to LED function, GPIO0 and GPIO1 can be changed type of flicker for LED.

Bit	Symbol	R/W	Function	1	0	Initial Value
6	GP1_LEDMODE	R/W	GP1 LED_MODE Select bit	As below		OTP
5-4	GP1_LEDFUNC	R/W	GP1 Type of Flicker Select bit			0
2	GP0_LEDMODE	R/W	GP0 LED_MODE Select bit	As below		OTP
1-0	GP0_LEDFUNC	R/W	GP0 Type of Flicker Select bit			0

LED Mode (GPn_LEDMODE, n:0,1)	Power On/Off Status or Flicker Control (GPn_LEDFUNC, n:0,1)	GPIO	
		Mode	Flicker Type
0	Power Off	POWERON/OFF	Off
	Power On	POWERON/OFF	Always Turn-on
1	00b	LED	Off
	01b	LED	1Hz Flicker (25% Turn-on)
	10b	LED	4Hz Flicker (25% Turn-on)
	11b	LED	Always Turn-on

INTC

INTPOL: Interrupt Polarity Register [Address 9Ch]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	INTPOL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [0]: INTPOL

INTB pin polarity
0: Low-active
1: High-active

INTEN: Interrupt Output Control Register [Address 9Dh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	GPIO IREN	-	-	DCDC IREN	SYSTEM IREN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [4]: GPIOIREN

GPIO interrupt control
0: Disable
1: Enable

Bit [1]: DCDCIREN

DCDC interrupt control
0: Disable
1: Enable

Bit [0]: SYSTEMIREN

SYSTEM interrupt control
0: Disable
1: Enable

INTMON: Interrupt Monitor Register [Address 9Eh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	WDG IRM	GPIO IRM	-	-	DCDC IRM	SYSTEM IRM
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit [5]: WDGIRM

Watchdog interrupt flag monitor
0: None
1: Requested

Bit [4]: GPIOIRM

GPIO interrupt flag monitor
0: None
1: Requested

Bit [1]: DCDCIRM

DCDC interrupt flag monitor
0: None
1: Requested

Bit [0]: SYSTEMIRM

SYSTEM interrupt flag monitor
0: None
1: Requested

SYSTEM OPTION

PREVINDAC: PREVINDET Detection Voltage Setting Register [Address B0h]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	PREVINDACH	PREVINDAC[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	By OTP	By OTP	By OTP

The default voltage can be set up by OTP.

Bit [2]: PREVINDACH

Setting the detection voltage to PREVINDET

Bit [1:0]: PREVINDAC

Setting the detection voltage to PREVINDET

PREVINDET Detection Voltage Table

PREVINDACH	PREVINDAC[1:0]	Detection Voltage [V]
0	00 (0h)	2.75(↑)/2.7(↓)
0	01 (1h)	2.85(↑)/2.8(↓)
0	10 (2h)	2.95(↑)/2.9(↓)
0	11 (3h)	3.05(↑)/3.0(↓)
1	00 (0h)	3.30(↑)/3.2(↓)
1	01 (1h)	3.40(↑)/3.3(↓)
1	10 (2h)	3.50(↑)/3.4(↓)
1	11 (3h)	3.60(↑)/3.5(↓)

OVTEMP: Overheat Detection Temperature Setting Register [Address BCh]

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	OVTEMP[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	By OTP	

This register sets the detection temperature for Overheat temperature.

Bit [1:0]: OVTEMP[1:0]

Setting the detection temperature of overheat detection.

OVTEMP[1:0]	Temperature [°C] (Detection / Recovery)
00 (0h)	105 / 85
01 (1h)	115 / 95
10 (2h)	125 /105
11 (3h)	135 / 115

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

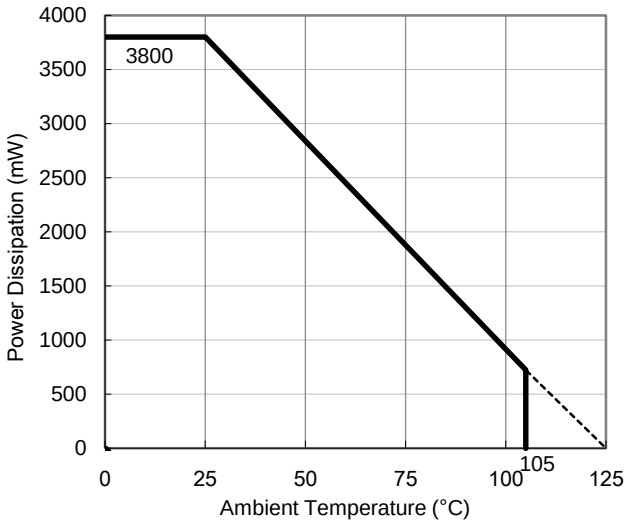
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 25 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

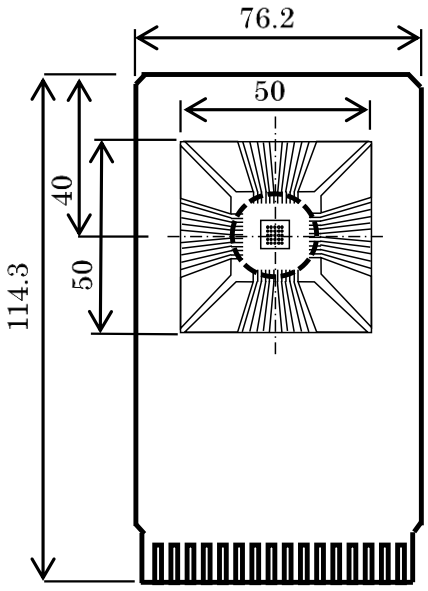
Item	Measurement Result
Power Dissipation	3800 mW
Thermal Resistance (θja)	θja = 26°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to–ambient thermal resistance.

ψjt: Junction–to-top of package thermal characterization parameter



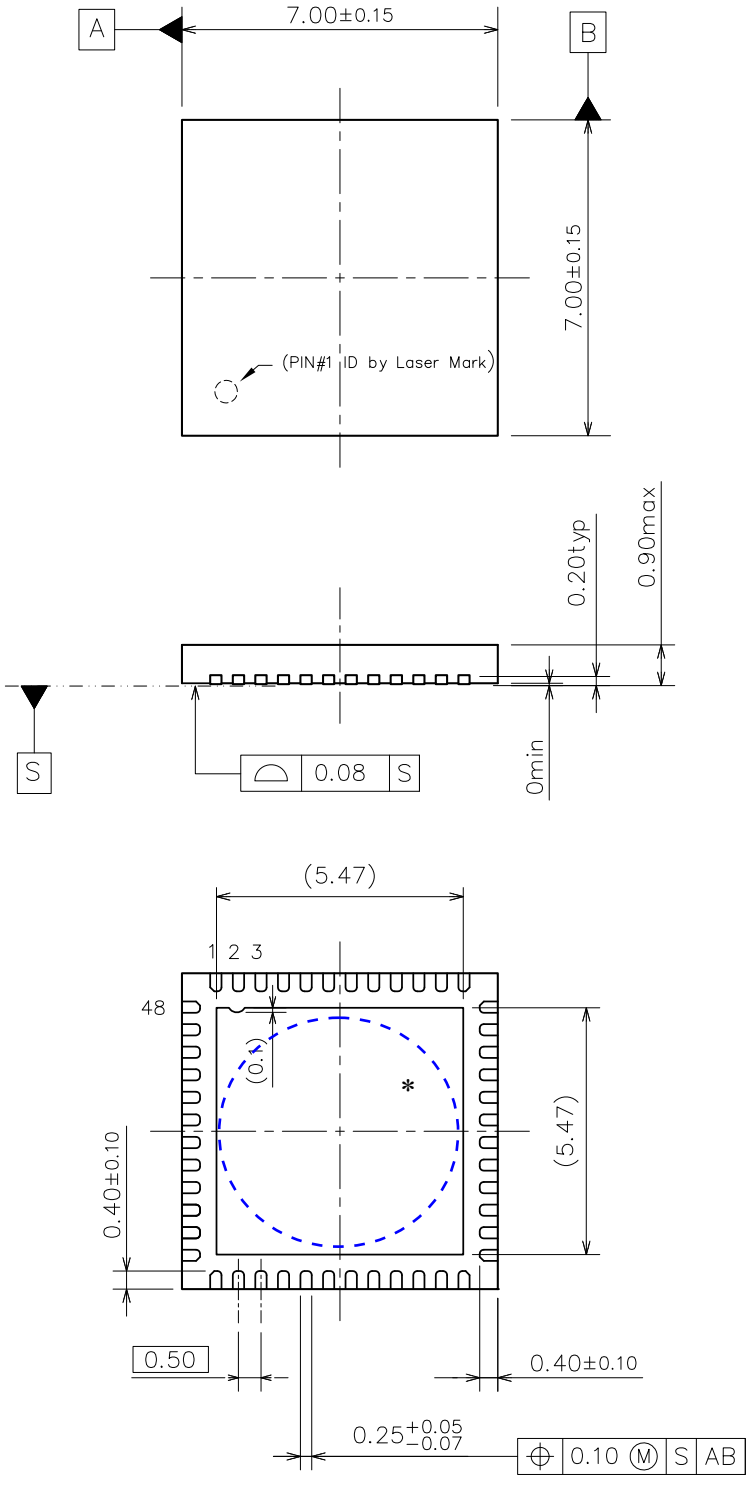
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. A



QFN0707-48-P25 Package Dimensions (Unit: mm)

*The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

RNT5610S OTP Settings

Normal mode, DCDC1-4 F_{OSC} = 1.80MHz

	OTP Function	Explanation	Related Register	Setting
System OTP Settings	I2CSLV	The settings of I2C slave address (A3-A1).	-	6: 36h
	ON_PRESS	The setting of PWRON pin power-on long press timer.	10h	2: 1sec
	SLEEPPOL	SLEEP pin polarity selection (Default High active)	-	0: Non-Inversion
	PWRONPOL	PWRON pin polarity selection (Default High active)	-	1: Inversion
	VINDAC	System Voltage Detection for Power-ON permit.	03h	2: 2.8V
	VINHYSSEL	Hysteresis Voltage for VINDET (System Voltage Detection for Power-ON permit)		0: 500mV
	VINRRESET	Select the reset condition(RSTB:Transition to PWROFF or ERSTB:UVLO detection) for VINHYS and VINDAC registers		1: ERSTB
	IODAC	Setting the detection voltage of IODET for Shutdown. IODET is invalid when VDDIO is not selected as the power supply	02h	0: 1.40V
	PREVINDAC	System Voltage Pre-Detection (Interrupt output)	B0h	5: 3.4(↑)/3.3(↓)
	OVTEMP	Initial temperature of Overheat Detection(Interrupt output)	BCh	2: 125/105℃

	OTP Function	Explanation	Related Register	Setting
Sequence OTP Settings	SLOTWID	Sequence Slot Timing Setting	-	1: 2.0ms
	LDORTC1AWON	LDORTC1 Always-ON or I2C Control	45h	1: AlwaysOn
	LDORTC1ONSLOT	The setting of LDORTC1 Power-ON sequence slot time (When selected I2C Control)	2Ah	Disable
	※ Be sure to reselect LDORTC1ONSLOT after LDORTC1AWON is changed.			
	LDO5ONSLOT	The setting of LDO5 Power-ON / OFF sequence slot time	1Fh	9: Slot_9
	LDO4ONSLOT	The setting of LDO4 Power-ON / OFF sequence slot time	1Eh	9: Slot_9
	LDO3ONSLOT	The setting of LDO3 Power-ON / OFF sequence slot time	1Dh	9: Slot_9
	LDO2ONSLOT	The setting of LDO2 Power-ON / OFF sequence slot time	1Ch	F: Slot_OFF
	LDO1ONSLOT	The setting of LDO1 Power-ON / OFF sequence slot time	1Bh	7: Slot_7
	DC4ONSLOT	The setting of DCDC4 Power-ON / OFF sequence slot time	19h	5: Slot_5
	DC3ONSLOT	The setting of DCDC3 Power-ON / OFF sequence slot time	18h	3: Slot_3
	DC2ONSLOT	The setting of DCDC2 Power-ON / OFF sequence slot time	17h	1: Slot_1
	DC1ONSLOT	The setting of DCDC1 Power-ON / OFF sequence slot time	16h	1: Slot_1
	RESETSLOT	Reset output signal sequence slot	-	F: Slot_15
	RESETHOLD	Reset output signal hold (Extend) time after Slot_15 (RESETO signal slot)	-	0: 0ms

	OTP Function	Explanation	Related Register	Setting
Initial VOUT OTP Settings	LRTCDAC	LDORTC1 Initial VOUT	56h	3.00V
	L5DAC	LDO5 Initial VOUT	50h	1.50V
	L4DAC	LDO4 Initial VOUT	4Fh	2.50V
	L3DAC	LDO3 Initial VOUT	4Eh	1.80V
	L2DAC	LDO2 Initial VOUT	4Dh	3.30V
	L1DAC	LDO1 Initial VOUT	4Ch	3.30V
	DD4DAC	DCDC4 Initial VOUT	39h	1.20V
	DD3DAC	DCDC3 Initial VOUT	38h	3.30V
	DD2DAC	DCDC2 Initial VOUT	37h	1.40V
	DD1DAC	DCDC1 Initial VOUT	36h	1.40V
	DD4LIM	DCDC4 Limit Current	33h	2: 2.8A
	DD3LIM	DCDC3 Limit Current	31h	3: 3.2A
	DD2LIM	DCDC2 Limit Current	2Fh	3: 4.0A
	DD1LIM	DCDC1 Limit Current	2Dh	3: 4.0A

	Function	Explanation	Related Register	Setting
GPIO Optional Functions OTP Settings	Use HRESET	Whether or not to use the HRESET (Hardware reset) function in the GPIO pin function.	-	1: Use
	※ Be sure to reselect all GPFUNC after USE_HRESET is changed.			

Ricoh Default	Setting	Selected Function	Power Supply's	Input Polarity	Input Type	Output Type	LED Function	LDORTC2 On/Off Control
GPIO0	27: ON1	ON_EXTIN	VSYS	Non-Inversion	NMOS	-	-	-
GPIO1	22: LD1	LED	VSYS	-	-	Nch Open Drain	Linked to PMU Status	-
GPIO2	29: PH1	PSHOLD	VSYS	Non-Inversion	NMOS	-	-	-
GPIO3	19: HR2	HRESET	VSYS	Inversion	NMOS	-	-	-

	Function	Explanation	Related Register	Setting
	PSO0ONSLOT	Power-ON output signal seqence slot (GPIO0 PSO function need)	25h	Disable
	PSO1ONSLOT	Power-ON output signal seqence slot (GPIO1 PSO function need)	26h	Disable
	PSO2ONSLOT	Power-ON output signal seqence slot (GPIO2 PSO function need)	27h	Disable
	PSO3ONSLOT	Power-ON output signal seqence slot (GPIO3 PSO function need)	28h	Disable
	LRTC2DAC	LDORTC2 Initial VOUT (GPIO2 function need)	57h	Disable

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