W600 Datasheet

V1.0.0

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Time	Modify content	Version	Author
2018-03-30	Initial	V 1.0.0	

Content

1 Features

- Chip appearance
  - QFN32 Package, 5mm x 5mm
- Chip integration

- Integrated 32-bit Cortex-M3 processor with 80MHz operating frequency;
- Integrated 288KB data storage;
- Integrated 1MB FLASH;
- Integrated 8-channel DMA controller, support any channel allocated for hardware use or software use, support 16 hardware applications, support software linked list management;
- Integrated 2.4G RF transceiver to meet IEEE802.11 specifications;
- Integrated PA/LNA/TR-Switch;
- Integrated 32.768KHz clock oscillator;
- Integrated voltage detection circuit;
- Integrated LDO;
- Integrated power control circuit;
- Integrated power-on reset circuit;
- Integrated Universal Encryption Hardware Accelerator Support PRNG(Pseudo random Number Genera tor)/ SHA1/MD5/RC4/DES/3DES/AES/CRC protocol

- Chip interface

- Integrated 1 SDIO2.0 Device controller, support SDIO1 bit / 4 bit / SPI three operating modes; working clock range 0~50MHz;
- Integrated 2 UART interfaces, support RTS/CTS, baud rate range 38Kbps~2Mbps;
- Integrated 1 high-speed SPI device controller with operating clock range 0~50MHz;
- Integrated with 1 SPI master/slave interface, the master device operating frequency supports 20Mpbs, and the slave device supports 6Mbps data transmission rate;
- Integrates an I2C controller to support 100/400Kbps speed;
- Integrated GPIO controller;
- Integrated PWM controller with for 5 PWM outputs or 2 PWM inputs. The highest output and input frequency is 20MHz.
- Integrated duplex I2S controller supporting 32KHz to 192KHz I2S interface codec;
- Integrated 7816 interface, support ISO-7816-3 T=0/1 mode, support EVM2000 specification,compatible with serial port function;

- Protocol and function
  - Support GB15629.11-2006、IEEE802.11 b/g/e/i/d/k/r/s/w/n;
  - Support WAPI2.0;
  - Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS;
  - Support Wi-Fi Direct;
  - Support EDCA channel access mode;
  - Support 20/40M bandwidth working mode;
  - Support STBC, GreenField, Short-GI, support reverse transmission;
  - Support RIFS frame interval;
  - Support AMPDU、AMSDU;
  - Support IEEE802.11n MCS 0~7, MCS32 physical layer transmission rate gear, the transmission rate is up to
  - 150Mbps;Short Preamble is supported when transmitting at 2/5.5/11 Mbps rate;
  - Support HT-immediate Compressed Block Ack, Normal Ack, No Ack response mode;

- Support CTS to self;
- Support AP function;
- Supported as both AP and STA at the same time;
- In the BSS network, multiple multicast networks are supported, and each multicast network is supported in different encryption modes. The maximum number of multicast networks and the STAs that are connected to the network can be up to 32.
- When the BSS network is used as an AP, the total number of supported sites and groups is 32, and 16 sites are supported in the IBSS network.
- Receive sensitivity:
  - 20MHz MCS7@-71dBm;
  - 40MHz MCS7@-68dBm;
  - 54Mbps@-73dBm;
  - 11Mbps@-86dBm;
  - 1Mbps@-95dBm;
- Allowed carrier frequency deviation：50ppm； Allowable sampling
- frequency deviation: 50ppm;
- Support different encryption mode STA communication;
- Support a variety of different receive frame filtering options;
- Support monitoring function;

- Power supply and power consumption
  - 3.3V single power supply;
  - Support PS-Poll, U-APSD power management;
  - Standby power consumption is less than 10uA;

2 Overview

This chip is a SoC chip that supports multi-interface, multi-protocol wireless LAN IEEE802.11n (1T1R). Applicable to IoT applications such as smart homes, wireless audio and video, smart toys, medical monitoring, industrial control, etc.

3 Chip characteristics

The SoC chip integrates Coertex-M3 core, built-in Flash, integrated RF transceiver front-end RF Transceiver, CMOS PA power amplifier, baseband processor/media access control, supports SDIO, SPI, UART, GPIO, I2C, PWM, I2S, 7816 and other interfaces. Support multiple encryption and decryption protocols, such as PRNG (Pseudo random Number Generator) / SHA1/ MD5 / RC4 / DES / 3DES / AES / CRC.

4 Chip structure

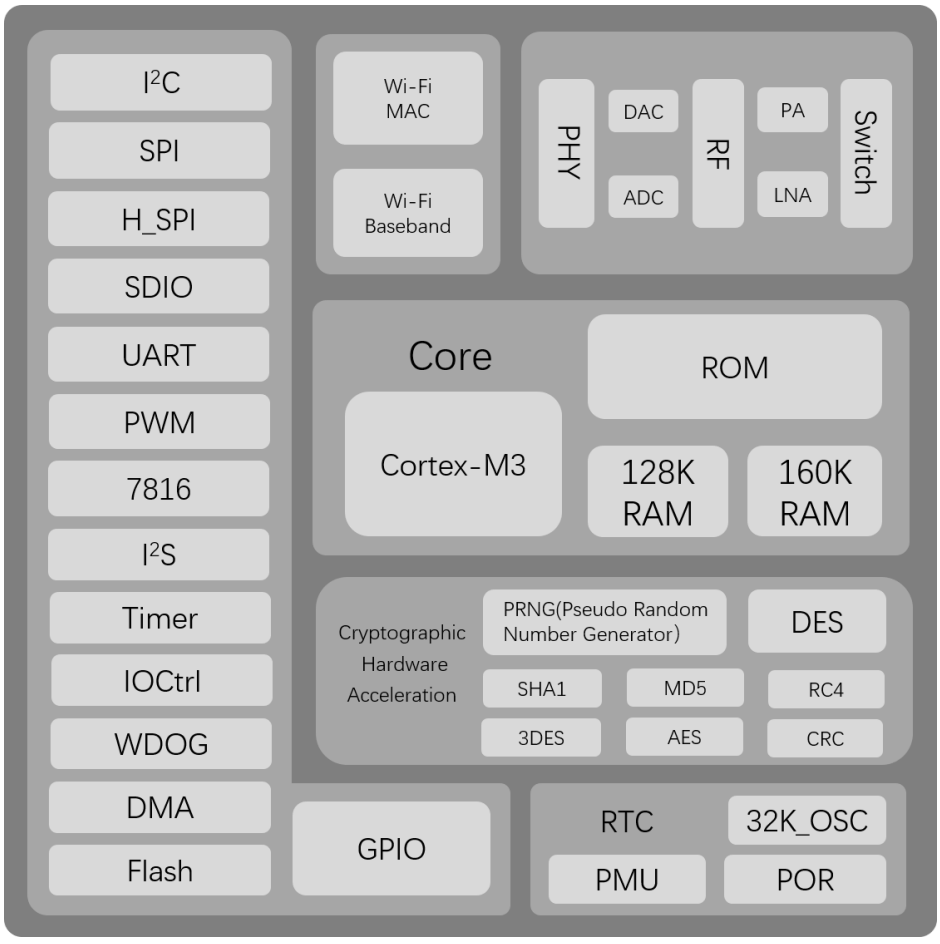

Figure 4-1 W600 chip structure

5 Address space division

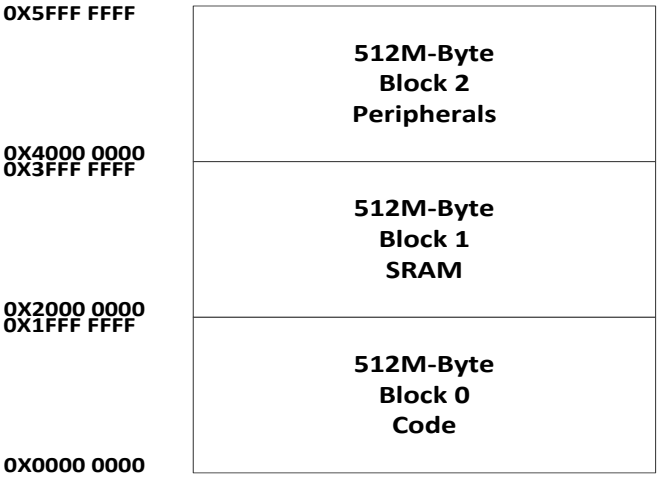

Figure 5-1 Address space mapping

Table 5-1 Detailed division of bus device address space

Bus slave Device	BootMode=0	BootMode=1	Address space segmentation	Remarks
ROM	0x00000000 ~ 0x0003FFFF	0x1FF00000 ~ 0x1FF3FFFF		Store the firmware code
FLASH	0x08000000 ~ 0x080FFFFF	0x00000000 ~ 0x000FFFFF		As a dedicated instruction memory.
SRAM	0x20000000 ~ 0x20027FFF	0x20000000 ~ 0x20027FFF		Firmware memory and instruction memory
MAC RAM	0x20028000 ~ 0x2003FFFF	0x20028000 ~ 0x2003FFFF		SDIO/H_SPI/UART Data cache
CONFIG	0x40000000 ~ 0x40001FFF	0x40000000 ~ 0x40001FFF	0x40000000 ~ 0x400001FF	SDIO configuration space
			0x40000200 ~ 0x400002FF	SPI configuration space
			0x40000300 ~ 0x400003FF	SDIO Wrapper configuration space
			0x40000400 ~ 0x400005FF	DMA configuration space
			0x40000600 ~ 0x400006FF	PMU configuration space
			0x40000700 ~ 0x400007FF	Clock and Reset configuration space
			0x40000800 ~ 0x400009FF	
			0x40000A00 ~ 0x400013FF	
			0x40001400 ~ 0x400017FF	
			0x40001800 ~ 0x40001FFF	
			0x40002000 ~ 0x400021FF	FLASH Controller configuration space
			0x40002200 ~ 0x400028FF	RSA configuration space
			0x40003200 ~ 0x400033FF	GPSEC configuration space
APB	0x40010000 ~ 0x4003C000	0x40010000 ~ 0x4003C000	0x40010000 ~ 0x400101FF	I²C Master
			0x40010200 ~ 0x400103FF	
			0x40010400 ~ 0x400107FF	SPI Master
			0x40010800 ~ 0x400109FF	UART0
			0x40010A00 ~ 0x40010BFF	UART1
			0x40010C00 ~ 0x40010DFF	GPIOA
			0x40010E00 ~ 0x40010FFF	Timer
			0x40011000 ~ 0x400111FF	WDOG

			0x40011200 ~ 0x400113FF	GPIOB
			0x40011400 ~ 0x400115FF	
			0x40011600 ~ 0x400117FF	
			0x40011800 ~ 0x400119FF	PWM
			0x40011A00 ~ 0x40011BFF	I²S
			0x40011C00 ~ 0x40011DFF	7816/UART2
			0x40014000 ~ 0x4000BFFF	
			0x4001C000 ~ 0x4003BFFF	
			0x40013C00 ~ 0x5FFFFFFF	RSV

6 Function Description

6.1 SDIO Device Controller

The SDIO2.0 device-side interface completes the interaction with the host data. Internally integrate 1024Byte asynchronous FIFO to complete data interaction between host and chip.

- Compatible with SDIO Card Specification 2.0
- Support host rate 0~50MHz
- Support for blocks up to 1024 bytes
- Support soft reset function
- Supports SPI, 1-bit SD, and 4-bit SD modes

6.2 High speed SPI device controller

Compatible with the universal SPI physical layer protocol, the host supports high-speed access to the device through a data format that interacts with the host. The maximum supported operating frequency is 50Mbps.

- Compatible with the general SPI protocol;
- Selectable level interrupt signal;
- Supports up to 50Mbps rate;
- Simple frame format, full hardware resolution and DMA

6.3 DMA Controller

Supports up to 8 channels, 16 DMA request sources, and supports linked list structure and register control.

- Amba2.0 standard bus interface, 8 DMA channels;
- Support DMA operations based on memory linked list structure;
- The software configures 16 hardware request sources;
- Support 1,4-burst mode of operation;
- Support byte, half-word, word operation;
- The source and destination addresses are unchanged or sequentially incremented configurable or cyclically within a predefined address range;

- Synchronous DMA request and DMA response hardware interface timing

6.4 Clock and Reset

Support chip clock and reset system control, clock control includes clock frequency conversion, clock shutdown and adaptive gating; reset control includes system and sub-module soft reset control.。

6.5 Memory manager

Supports the configuration of sending buffer and receiving buffer size, as well as the control information such as the base address of the MAC access buffer, the number of caches, and the upper limit of the frame aggregation.

6.6 Digital baseband

Support IEEE802.11a/b/g/e/n(1T1R) transmission and receiver algorithm implementation, main parameters:

- Data rate：1~54Mpbs（802.11a/b/g）， 6.5~150Mbps(802.11n)；
- MCS format：MCS0~MCS7，MCS32(40MHz HT Duplicate Mode)；
- Supports 40MHz bandwidth non-HT Duplicate mode, 6M ~ 54M;
- Signal bandwidth：20MHz, 40MHz；
- Modulation：DSSS(DBPSK,DQPSK,CCK) and OFDM(BPSK,QPSK,16QAM,64QAM)；
- Implement 1T1R MIMO-OFDM spatial multiplexing；
- Support Short GI mode;
- Support Legacy mode and Mixed mode;
- Supports transmission and reception of 20M upper and lower sideband signals at 40MHz bandwidth;
- Support STBC reception of MCS0~7, 32;
- Support Green Field mode;

6.7 MAC controller

Supports IEEE802.11a/b/g/e/n MAC sublayer protocol control. Specific specifications include:

- Support EDCA channel access mode;
- Support CSMA/CA, NAV and TXOP protection mechanisms;
- Beacon, Mng, VO, VI, BE, BK five-way send queue and QoS;
- Support single and wide group wave frame reception and transmission;
- Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame sequence;
- Support retransmission mechanism and retransmission rate and power control;
- Support MPDU hardware aggregation and de-aggregation,support Immediate BlockAck mode;
- Support RIFS，SIFS，AIFS；
- Support reverse transmission mechanism;
- Supports TSF timing and it is software configurable;

- Support MIB statistics;

6.8 Security system

Supports the security algorithm specified by the IEEE802.11a/b/g/e/n protocol, and cooperates with the encryption and decryption of transmitting and receiving data frames.

- The encryption and decryption throughput rate is greater than 150MHz;
- Amba2.0 standard bus interface;
- Support WAPI security mode 2.0;
- Support WEP security mode - 64-bit encryption;
- Support WEP security mode - 128 bit encryption;
- Support TKIP security mode;
- Support CCMP security mode;

6.9 FLASH controller

- Provide bus access FLASH interface;
- Provide system bus and data bus access arbitration;
- Implement CACHE cache system to improve FLASH interface access speed;
- Provide compatibility with different QFlash;

6.10 RSA encryption module

The RSA Computation Hardware Coprocessor provides Montgomery (FIOS Algorithm) modular multiplication. The RSA algorithm is implemented in conjunction with the RSA software library. Supports 128-bit to 2048-bit modular multiplication.

6.11 Universal hardware encryption module

The encryption module automatically completes the encryption of the source address space data of a specified length, and automatically writes the encrypted data back to the specified destination address space after completion; supports PRNG (Pseudo random Number Generator)/SHA1/MD5/RC4/DES/3DES/AES/ CRC.

6.12 I^2C Controller

APB bus protocol standard interface, only supports the main device controller, I2C working frequency support can be configured, 100K-400K.

6.13 Master/slave SPI controller

Synchronous SPI master-slave function is supported. Its working clock is the system internal bus clock. Its characteristics are as follows:

- The transmit and receive paths each have a FIFO of 8 words deep;

- Master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing;
- The slave supports four formats of the Motorola SPI (CPOL, CPHA);
- Support full duplex and half duplex;
- The master device supports bit transmission and supports up to 65535bit transmission.
- The slave device supports transmission modes of various length bytes;
- The maximum clock frequency of the slave device input SPI_Clk is 1/6 of the system clock;

6.14 UART controller

- The device end complies with the APB bus interface protocol;
- Support interrupt or polling mode of operation;
- Support DMA transfer mode, send and receive each 32-byte FIFO;
- The baud rate is programmable;
- 5-8bit data length, and parity polarity configurable;
- 1 or 2 stop bits are configurable;
- Support RTS/CTS flow control;
- Support for Break frame transmission and reception;
- Overrun, parity error, frame error, rx interrupt indication
- Maximum 16-burst byte DMA operation;

6.15 GPIO controller

48-bit configurable GPIO, software-controlled I/O, hardware-controlled I/O, configurable interrupt mode. The GPIOA and GPIOB registers have different start addresses but are functionally identical.

6.16 Timer

Microseconds and milliseconds (the number of counts configured according to the clock frequency) implements six configurable 32-bit counters that generate a corresponding interrupt when the count of the corresponding calculator configuration is completed.

6.17 Watchdog controller

Support for the "watchdog" function. Observe the correctness of the software and allow a global reset after the system crashes. The "watchdog" generates a periodic interrupt, the system software must respond to this interrupt and clear the interrupt flag; if the interrupt flag has not been cleared for a long time due to a system crash, a hard reset will be generated to perform a global reset of the system.

6.18 RF configurator

A synchronized SPI master function is implemented. Its working clock is the system internal bus clock. The characteristics are as follows:

- The transmit and receive paths each have a FIFO of 1 word depth;

6.19 RF transceiver

- The RF transceiver section includes power amplifiers, transmit paths, receive paths, phase-locked loops, and SPI modules. Change the working state of the chip by adjusting the control ports SHDN, RXEN and TXEN;
- The receiving path uses a zero-IF structure to directly convert the RF signal into two baseband I and Q outputs. The RF front-end operates at 2.4 GHz and includes low noise amplifier and quadrature mixers; the baseband consists of a low-pass filter and a variable gain amplifier for channel filtering and gain control; and the driver amplifier provides different DC outputs for the ADC interface;
- The transmit path consists of a programmable control filter, an upconverting mixer, a variable gain amplifier and a power amplifier. The transmit path is also a direct conversion structure. The output signal of the DAC passes through a low-pass filter to filter out the image frequency and out-of-band noise. The PA output is a differential output driver for the off-chip antenna;

6.20 PWM Controller

- 5-channel PWM signal generation function;
- 2 channel input signal capture function (PWM0 and PWM4 two channels);
- Frequency range: 3Hz~160KHz;
- Maximum duty cycle accuracy 1/256, the width of the counter inserted into the dead zone: 8bit;

6.21 I²S Controller

- Support AMBA APB bus interface, 32bit single read and write operations;
- Support master, slave mode, can work duplex;
- Support 8/16/24/32 bit width, the highest sampling frequency is 128KHz;
- Supports mono and stereo modes;
- Compatible with I2S and MSB justified data formats, compatible with PCM A/B format;
- Support DMA request read and write operations. Only word-based operations are supported.

6.22 7816/UART Controller

- The device end complies with the APB bus interface protocol;
- Support interrupt or polling mode of operation;
- Support DMA transfer mode, send and receive each have a 32-byte FIFO;
- DMA can only operate in bytes, with a maximum 16-burst byte DMA operation;

Compatible with UART and 7816 interface functions:

Serial port function:

- The baud rate is programmable;
- 5-8bit data length, and parity polarity configurable;
- 1 or 2 stop bits which is configurable;
- Support RTS/CTS flow control;
- Support for Break frame transmission and reception;
- Overrun, parity error, frame error, rx break frame interrupt indication

7816Interface function:

- Compatible with ISO-7816-3 T=0.T=1 mode;

- Compatible with EVM2000 protocol;
- Configurable guard time (11 ETU-267 ETU);
- Forward/reverse conventions are software configurable;
- Support for send/receive parity and retransmission functions;
- Support 0.5 and 1.5 stop bit configuration;

7 Pin definition

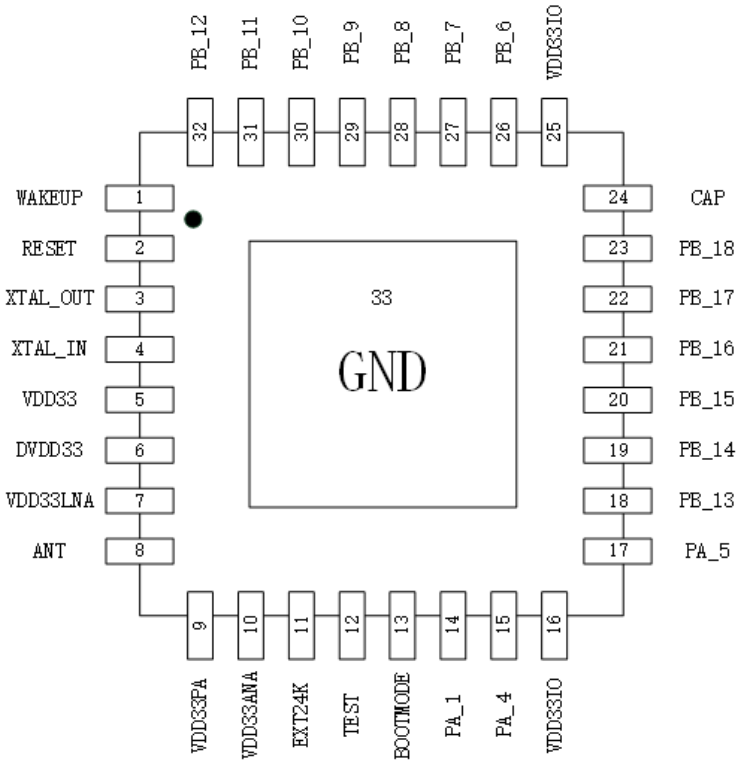

Figure 7-1 Pin Layout (QFN32)

Table 7-1 Pin Assignment Definition (QFN32)

Number	Pin name	Type	Pin function	Pin multiplexing
1	WAKEUP	I	WAKEUP	
2	RESET	I	RESET	
3	XTAL_OUT	O	External crystal output	
4	XTAL_IN	I	External crystal intput	
5	VDD33	P	Chip power,3.3V	
6	DVDD33	P	Digital circuit power,3.3V	
7	VDD33LNA	P	LNA power,3.3V	
8	ANT	I/O	Radio frequency antenna	
9	VDD33PA	P	PA power, 3.3V	
10	VDD33ANA	P	Analog power supply,3.3V	
11	EXT24K	I	Series 24KΩ+-1% precision resistor to GND	
12	TEST	I	Test function configuration pin	
13	BOOTMODE	I/O	BOOTMODE	PWM_1、GPIOPA_0
14	PA_1	I/O	Reserved	SIM_DATA、PWM_2、SPI(M/S)_CK、GPIOPA_1

15	PA_4	I/O	UART0_TX	PWM_5、SPI(M/S)_DO、I²S_M_SCL、GPIOPA_4
16	VDD33IO	P	IO power, 3.3V	
17	PA_5	I/O	UART0_RX	PWM_1、SPI(M/S)_DI、I²S_M_EXTCLK、GPIOPA_5
18	PB_13	I/O	PWM_2	I²C_SCL、SDIO_CMD、GPIOPB_13
19	PB_14	I/O	H_SPI_INT	PWM_5、I²C_DAT、I²S_S_SDA、GPIOPB_14
20	PB_15	I/O	H_SPI_CS	PWM_4、SPI(M/S)_CS、I²S_S_SCL、GPIOPB_15
21	PB_16	I/O	H_SPI_CK	PWM_3、SPI(M/S)_CK、I²S_S_RL、GPIOPB_16
22	PB_17	I/O	H_SPI_DI	PWM_2、SPI(M/S)_DI、UART1_RX、GPIOPB_17
23	PB_18	I/O	H_SPI_DO	PWM_1、SPI(M/S)_DO、UART1_TX、GPIOPB_18
24	CAP	I	External capacitor, 1μF	
25	VDD33IO	P	IO power, 3.3V	
26	PB_6	I/O	Reserved	SWDAT、UART0_RX、PWM_4、SIM_CLK、GPIOPB_6
27	PB_7	I/O	Reserved	SWCK、UART0_TX、SDIO_CMD、SPI(M/S)_CS、GPIOPB_7
28	PB_8	I/O	PWM_5	H_SPI_CK、SDIO_CK、I²S_M_SCL、GPIOPB_8
29	PB_9	I/O	UART1_CTS	H_SPI_INT、SDIO_DAT0、I²S_M_SDA、GPIOPB_9
30	PB_10	I/O	UART1_RTS	H_SPI_CS、SDIO_DAT1、I²S_M_RL、GPIOPB_10
31	PB_11	I/O	UART1_RX	H_SPI_DI、SDIO_DAT2、I²C_SCL、GPIOPB_11
32	PB_12	I/O	UART1_TX	H_SPI_DO、SDIO_DAT3、I²C_DAT、GPIOPB_12
33	GND	P	connect to GND	

Note：1. I = Input O = Output, P = Power

8 Electrical characteristics

8.1 Limit parameter

Table 8-1 Limit parameters

Parameter	Name	Minimum value	Typical value	Maximum value	Unit
Supply voltage	VDD		3.3		V
Input logic level low	V_{IL}	-0.3		0.8	V
Input logic level high	V_{IH}	2.0		VDD+0.3	V
Inputt pin capacitance	C_{pad}			2	pF
Output logic level low	V_{OL}			0.4	V
Output logic level high	V_{OH}	2.4			V
Output maximum drive	I_{MAX}			24	mA
Storage temperature range	T_{STR}	-40℃		+125℃	℃
Working temperature range	T_{OPR}	-40℃		+80℃	℃

8.2 RF power consumption parameters

Table 8-2 RF power consumption parameters

Mode	Typical Value	unit
Send IEEE802.11b, CCK 11Mbps, POUT = +19 dBm	230	mA
Send IEEE802.11g, OFDM 54Mbps, POUT = +13.5 dBm	210	mA
Send IEEE802.11n, OFDM MCS7, POUT = +12dBm	210	mA
Receive IEEE802.11b/g/n	100-110	mA

8.3 Wi-Fi Radio

Table 8-3 Wi-Fi RF parameters

Parameter	Typical Value	Unit
Input frequency	2.4GHz~2.4835MHz	
output Power		
72.2 Mbps PA Output Power	12	dBm
11b Mode PA Output Power	19	dBm
Sensitivity		
DSSS, 1 Mbps	-95	dBm
CCK, 11 Mbps	-86	dBm
OFDM, 6 Mbps	-89	dBm

OFDM, 54 Mbps	-73	dBm
HT20, MCS0	-89	dBm
HT20, MCS7	-71	dBm
HT40, MCS0	-85	dBm
HT40, MCS7	-68	dBm
Adjacent channel suppression		
OFDM, 6 Mbps	32	dB
OFDM, 54 Mbps	15	dB
HT20, MCS0	29	dB
HT20, MCS7	10	dB

9 Package information

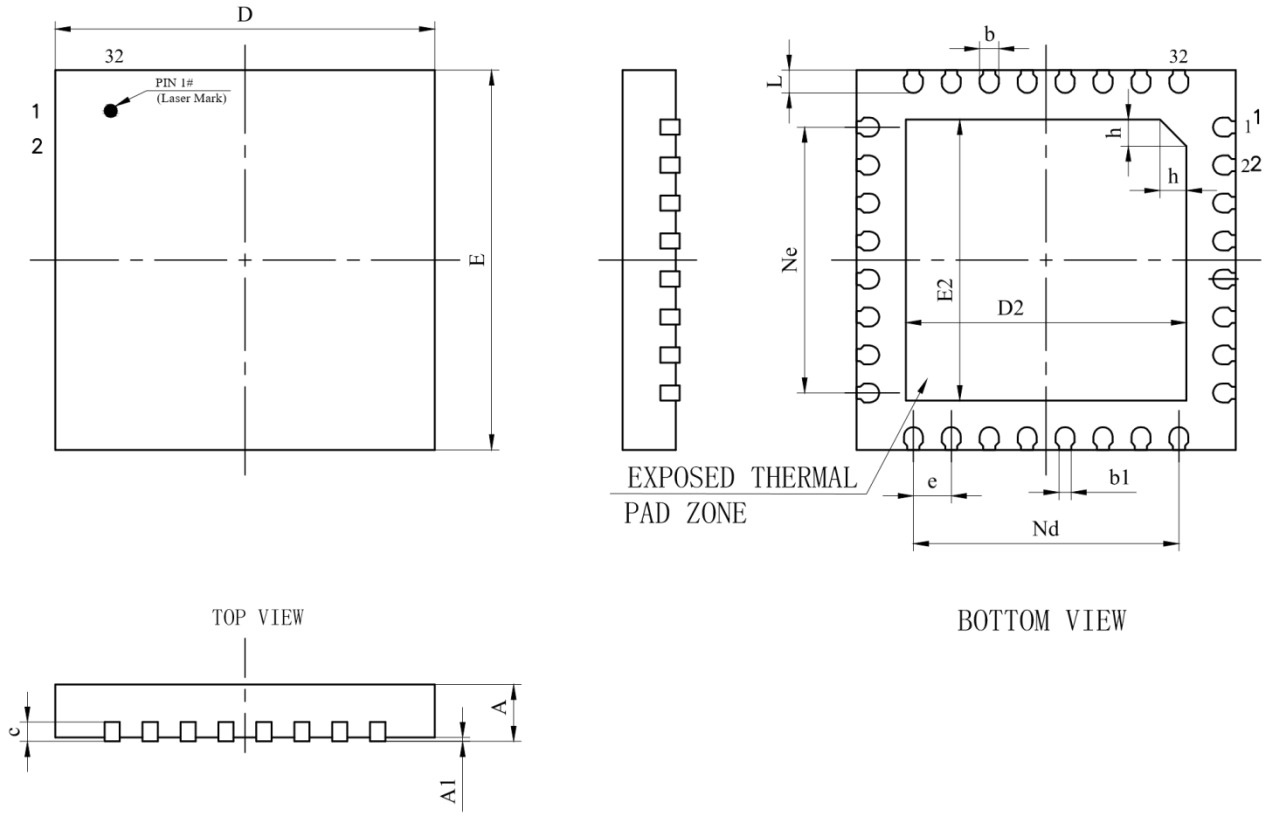

Figure 9-1 W600 package parameters

Table 9-1 W600 Package Parameter Table

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
e	0.50BSC		
Ne	3.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10

E2	3.70	3.80	3.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size	4.10x4.10		

10 Product model definition

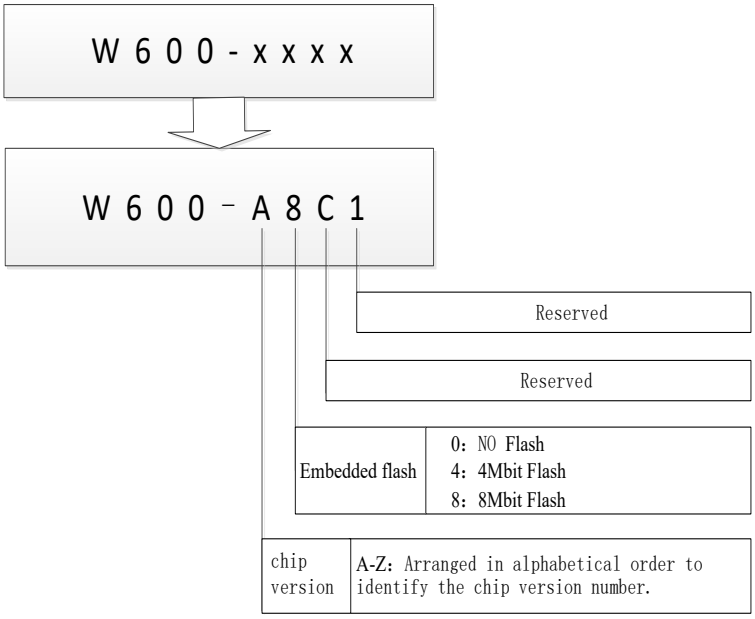

Figure 10-1 Chip Model Naming Reference