2ED24427N01F

10 A dual-channel low-side gate driver IC

Features

- 10 A sink and 10 A source driver capability
- 11.5 V under voltage lockout
- 24 V maximum supply voltage
- Enable function
- CMOS Schmitt-triggered inputs
- Output in phase with input
- 3.3 V, 5 V and 15 V input logic compatible
- 2 kV ESD HBM
- RoHS compliant

Product summary

V_{CC} = 12.5 V to 24 V
I_{o+pk} / I_{o-pk}(typ.) =+ 10 A/ - 10 A
t_{ON} / t_{OFF} (max.) = 40 ns/ 55 ns

Package

Power Pad DSO-8

Potential applications

Driving high current IGBTs, enhancement mode N-Channel MOSFETs directly or through a gate drive transformer in various power electronic applications in single or parallel combinations
Typical Infineon recommendations are as below:

- Electric vehicle (EV) charging stations and battery management systems
- DC-DC converters
- Industrial Drives
- Industrial SMPS
- Motor control
- Industrial applications
- General purpose low-side gate driver

Product validation

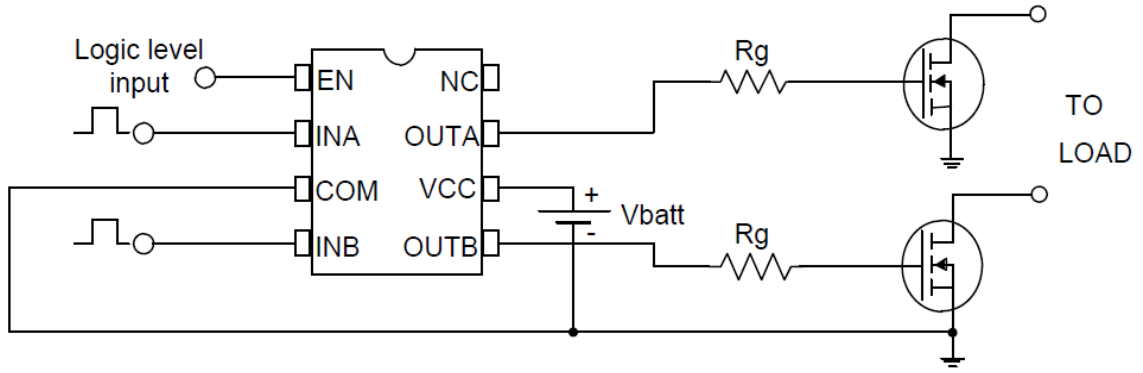
Qualified for industrial applications according to the relevant tests of JEDEC JESD47/22 and J-STD-020.

Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED24427N01F	PG-DSO-8-900	Tape and Reel	2500	2ED24427N01FXUMA1

Description

The 2ED24427N01F is a low-voltage, power MOSFET and IGBT non-inverting gate driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output driver features a current buffer stage. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched. Internal circuitry on VCC pin provides an under voltage lockout protection that holds output low until Vcc supply voltage is within operating range.



* This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application block diagram

1 Table of contents

2 Block diagram

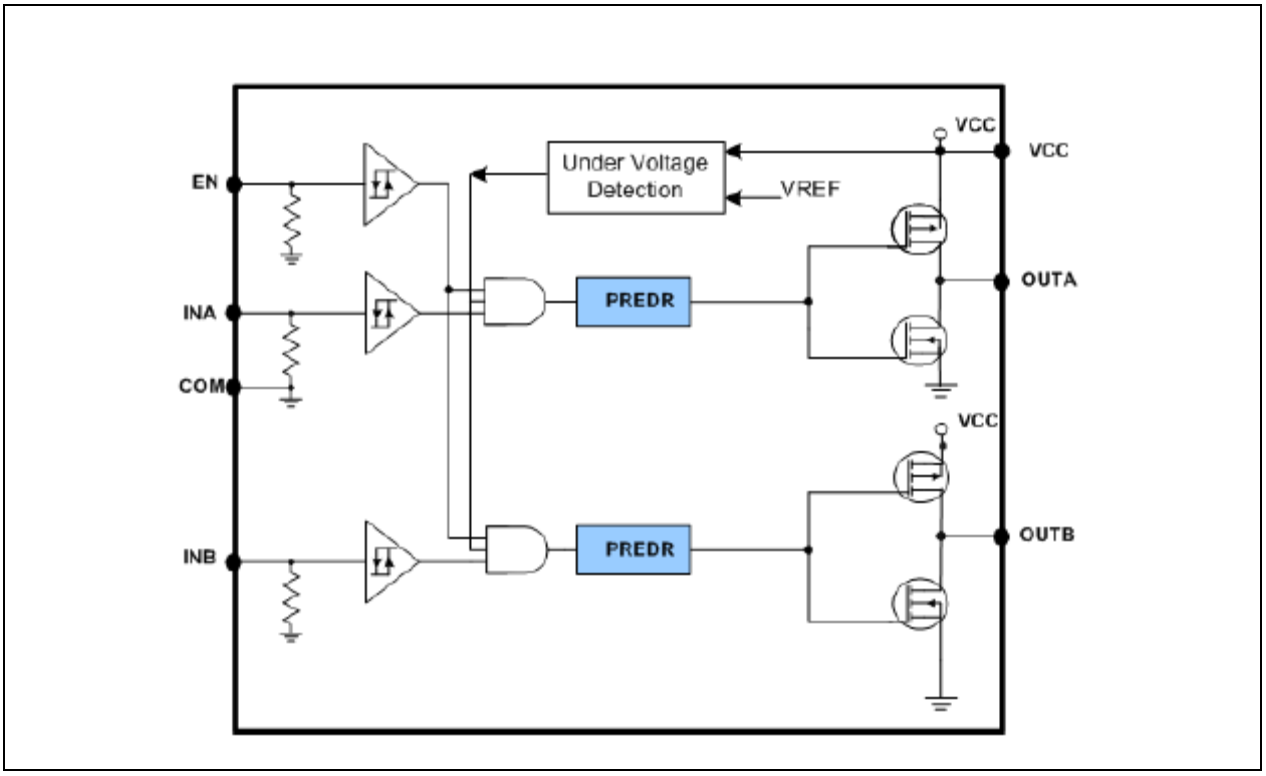


Figure 2 Block diagrams

3 Pin configuration, functionality and logic truth-table

3.1 Pin configuration

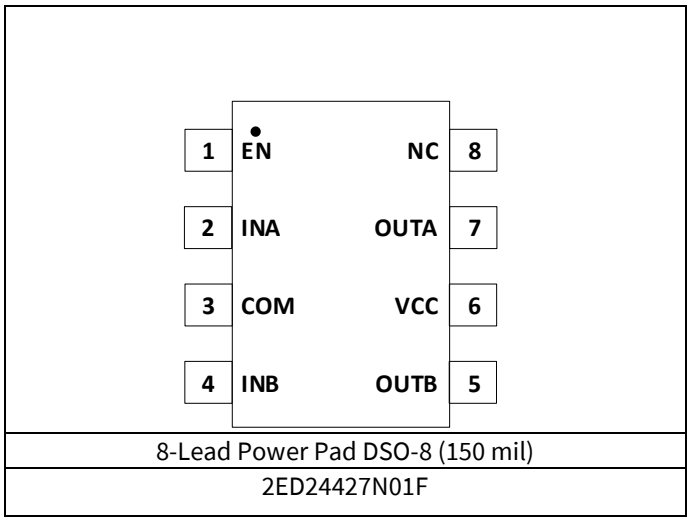


Figure 3 2ED24427N01Fpin assignments (top view)

3.2 Pin functionality

Table 1

Pin no.	Symbol	Description
1	EN	Enable pin
2	INA	Logic input for gate driver output (OUTA), in phase
3	COM	Ground
4	INB	Logic input for gate driver output (OUTB), in phase
5	OUTB	Gate drive output B
6	VCC	Supply voltage
7	OUTA	Gate drive output A
8	NC	No connection

3.3 Input/output logic truth table

Table 2 Input/output logic truth table

EN	INA	INB	OUTA	OUTB
L	X		L	L
L	X		L	L
H	L	L	L	L
H	H	H	H	H

This table is held true in the voltages ranges defined in the recommended conditions section.

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the ―Recommended Operating Conditions‖ is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Table 3 Absolute maximum ratings

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	– 0.3	24	V
V_O	Output voltage	– 0.3	24	
V_{IN}	Logic input voltage	– 0.3	5.5	
V_{EN}	Logic enable voltage	– 0.3	5.5	
Rth_{JC}	Thermal resistance, junction to case	—	4	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	– 55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM.

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	5	20	V
V_O	Output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	5	
V_{EN}	Logic enable voltage	0	5	
T_A	Ambient temperature	– 40	125	°C
R_G	External gate resistance	2.5		Ω
C_{BP}	VCC to COM bypass capacitance – X7R dielectric type	1		µF

4.3 Static electrical characteristics

Unless otherwise specified, these specifications apply for an operating junction temperature range of Ta = 25°C and power supply V_{CC}=15 V. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to COM and are applicable to the output leads: OUTA and OUTB.

Table 5 Static electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IL}	Logic “0” input voltage	—	—	0.8	V	
V_{IH}	Logic “1” input voltage	2.5	—	—		
V_{HYS-IH}	Input voltage hysteresis	0.8	—	—		
V_{ENL}	Logic “0” enable voltage	—	—	0.8		
V_{ENH}	Logic “1” enable voltage	2.5	—	—		
V_{HYS-EN}	Enable voltage hysteresis	0.8	—	—		
ROH	Source output resistance	—	—	450	mΩ	Ta = +25°C
ROL	Sink output resistance	—	—	450		
VOH	Output high level voltage (V_{CC} – V_O)	—	—	450	mV	Ta = +25°C , I_O = 100 mA
VOL	Output low level voltage V_O	—	—	450		
I_{IN+}	Logic “1” input bias current	—	25	50	µA	V_{IN} = 5 V, V_{CC} = 15 V
I_{IN-}	Logic “0” input bias current	—	—	1		V_{IN} = 0 V, V_{CC} = 15 V
I_{QCC}	Quiescent supply current	0.5	1.2	2.4	mA	V_{CC} = 15 V, INA & INB not switching
V_{CCUV+}	Vcc supply undervoltage turn on threshold	10.5	11.5	12.6	V	
V_{CCUV-}	Vcc supply undervoltage turn off threshold	9.0	10.0	11.0		
V_{CCUVH}	Vcc supply undervoltage lockout hysteresis	—	1.5	—		
I_{O+}	Output sourcing short circuit pulsed current	—	10	—	A	V_{CC} = 15 V PW ≤ 10 µs
I_{O-}	Output sinking short circuit pulsed current	—	10	—		

4.4 Dynamic electrical characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of Ta = 25°C with bias conditions of V_{CC} = 15 V, C_L = 4700 pF. Refer to Figure T2 for switching time definition and to Figure T3 for switching time test circuit.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	—	40	ns	C_{BP} = 10 µF
t_{off}	Turn-off propagation delay	—	—	55		
t_{on-en}	Enable turn-on propagation delay	—	—	40		
t_{off-en}	Enable turn-off propagation delay	—	—	55		
t_r	Turn-on rise time	—	—	33		
t_f	Turn-off fall time	—	—	33		

5 Application information and additional details

Information regarding the following topics is included as subsections within this section of the datasheet.

- Gate driver
- Bridge tied gate transformer driver (BT-GTD)
- Driving circuitry design: thermal considerations
- Bias and transient conditions
- System functionality with improved thermal behavior
- Square input pulse distortion
- Bypass capacitor
- Additional information

5.1 Gate driver

The 2ED24427N01F is a high current gate driver for single ended applications. Due to its very high output current and low thermal resistance vs. pcb, it is capable to drive Mosfets with very large input capacitance at frequencies up to fsw = 200 kHz or higher without the need of negative supply. The following Figure 4 shows the typical application schematic:

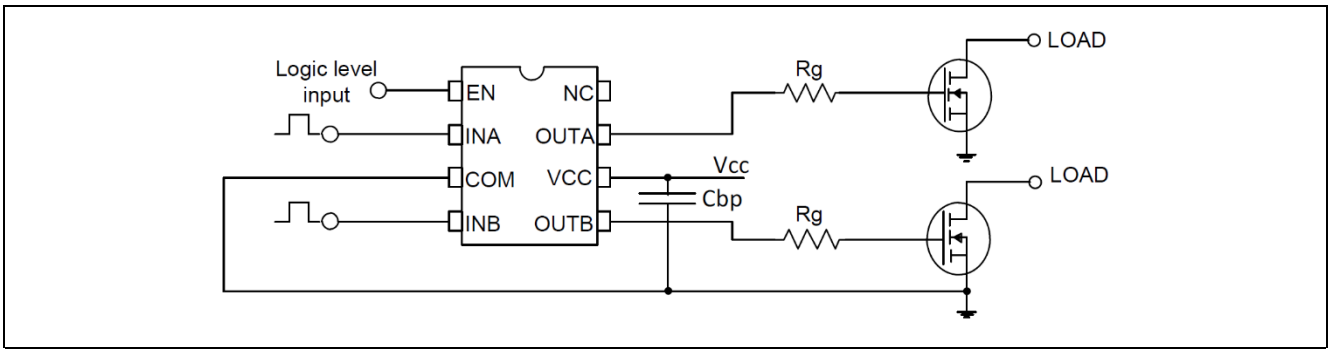


Figure 4 Typical gate driver application

Rg values have to be selected based on the requested tr and tf of the application and may vary between 2.5 Ω and 20 Ω, while the input capacitance of the fets can go up to 20 nF or more depending on the switching frequency. Since the very high peak output current, the bypass capacitor Cpb has to be mounted in the close proximityof the Vcc and COM pins and a ceramic type with low ESR has to be chosen.

5.2 Bridge tied gate transformer driver (BT-GTD)

This is a popular configuration that allows driving high side fets using a low side gate driver, the Figure 5 shows the typical schematic for a single fet drive:

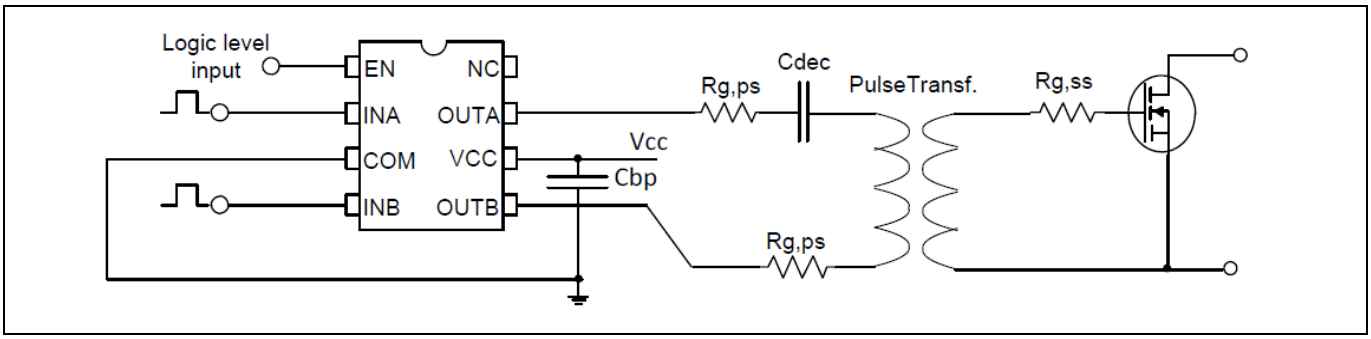


Figure 5 Bridge tied gate driver configuration

In this configuration the gate transformer parameters have a very important role, most manufacturers indicate the following in their datasheets:

- V*µs ratings: this factor must be respected, in bipolar drive application (like the one shown in Figure 5) a maximum of up to twice that parameter is still acceptable for most manufacturers, this factor then must be chosen accordingly to the following formula:

$$V * \mu s\ rating\ (*2) \geq \frac{Vprim*\delta}{fsw} \quad (1)$$

  where Vprim is the voltage applied to the primary, δ is the duty cycle and fsw the switching frequency of the application.

- N, turns ratio: usually 1:1, in some cases 1:2 or 1:1:1 (dual driver) this determines the voltage ratio between primary and secondary.

- Lp, primary inductance: this value determines the magnetizing inductance as follows:

$$Lm = Lp * K \quad (2)$$

  where K is the coupling factor between primary and secondary windings.

- L_{LK}, leakage inductance: this parameter, usually indicated at primary, is equal to:

$$L_{LK} = Lp * (1 - K) \quad (3)$$

The higher Lm is, the lower is the magnetizing current flowing into the transformer and consequent power losses into the driver. On the other hand the lower L_{LK} is, the lower and shorter will be the ringing of the secondary LC network created by L_{LK}, and Ciss of the fet, damped by Rgss and much lower overshot will appear on the Vgs across the Fet during transition. Then a too high Lm requires a very good mechanical construction of the gate transformer to achieve high K and consequent low L_{LK}.

In a gate driver application running in the range of 50 kHz-200 kHz and using the 2ED24427N01F, a good choice is usually a Lm between 300 µH and 2 mH and a L_{LK} < 1µH. This translate for the formula (2) and (3) above in a coupling factor K between 0.9940 and 0.9995

For good operation and to reduce unneeded power losses into the 2ED24427N01F driver, the magnetizing current has to be kept I_{LM} < 0.5 A, from this then derives a minimum Lm to be calculated as follows:

$$Lm_{min} = \frac{Vg}{0.5} * \frac{\delta}{fsw} \quad (4)$$

Where Vg is the gate driving voltage of the Fet

Figure 6 shows a good design waveform obtained with the following parameters:
Vg =+/-15 V, Lm = 400 µH, L_{LK} = 0.4 µH, N = 1, fsw = 100 kHz, $Ciss_{FET}$ = 10 nF, Rg,ps = 3Ω, Rg,ss = 4Ω, and Cdec = 1 µF

Cdec is the AC coupling capacitor needed to reset the driver transformer flux, its value has to be calculated in a way that the voltage across it can be considered constant during normal operation. The higher the fsw the smaller will be Cdec. A ceramic capacitor is normally used.

Figure 6 Bridge Tied Gate Driver waveforms

The waveforms in Figure 6 show that:

- The lower L_{LK} is, the lower and shorter is the ringing on the Fets gate voltage, particular care must be paid to guarantee that the max Vgs voltage of the Fet is not exceeded during operation.
- The lower L_{LK} is, the shorter the propagation delay is from the driver to the gate of the Fet and the higher the peak current is into its gate.
- The higher Lm is, the lower I_{LM} is; at the primary side the gate peak current, summed to ILM, constitute the total current flowing out of the gate driver.

5.3 Driving circuitry design: thermal considerations

The following design example shows how to get a proper design of the gate driving circuitry considering the following target application data:

- Switching frequency 150 kHz
- Load capacitance range [10-100] nF
- Supply voltage Vcc = 12 V

The switching losses due to the charge/discharge of the capacitive load CL represent the main component of the IC power dissipation. These losses are proportionally shared between the IC output resistance and the external gate resistance Rg.

As a consequence the thermal behavior of the IC, with the constraint of a maximum junction temperature equal to 150°C, is one of the key points in dimensioning the system parameters. 0 shows the power that is dissipated inside the IC as a function of load capacitance CL. The external resistance Rg has been chosen in order to keep the product RL*Cg as constant and equal to 300 ns (refer to Figure 4 for switching circuit schematic).

For a given parameter sizing the value of Pow allows to calculate the junction temperature Tj as:

$$T_J = T_A + Pow * R_{th-JA} \quad (5)$$

Where T_A is the ambient temperature and R_{thJA} is the junction to ambient thermal resistance.

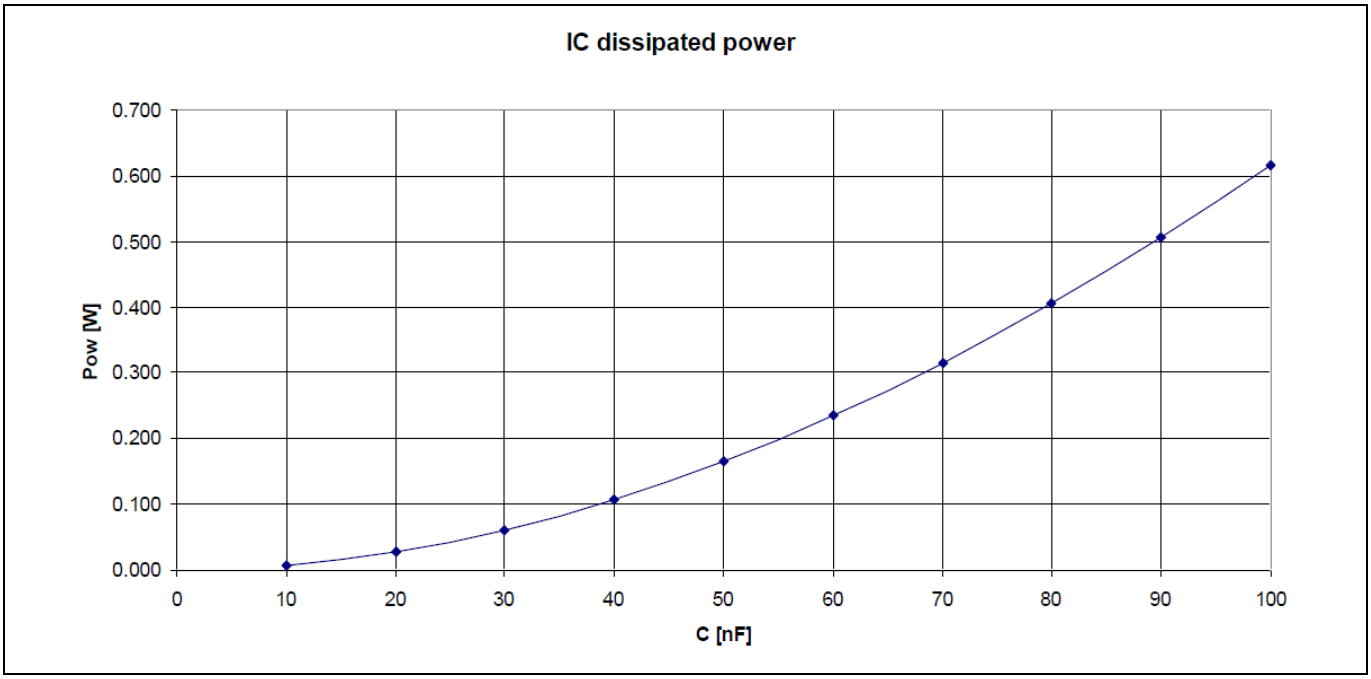


Figure 7 Simulated IC power dissipation as a function of load capacitance.

5.4 Bias and transient conditions

The input pins of the IC are protected by ESD events with the circuitry shown into —"Functional block diagram" section at par. Input/Output/Enable Pin Equivalent Circuit Diagrams. This shows that an ESD diode is placed in between each of these pins and Vcc.

In case Vcc voltage will be lower than one of the voltage applied to these pins the diode will conduct. Because of its power dissipation the junction temperature will increase. In order to avoid dangerous working conditions it is recommended to keep the Vcc voltage always higher or equal to the INA/INB/Enable pin voltages; it is remind that input voltage must respect the defined absolute maximum rating limits.

5.5 System functionality with improved thermal behavior

The PG-DSO8-900 package is characterized by a metal thermal pad whose functionality is to reduce the junction to case thermal resistance. In order to better exploit this feature it is necessary to reduce as much as possible the thermal pad to PCB thermal resistance (RthTP-PCB in 0).

Two possible ways are suggested:

a. Foresee a footprint on layout that allows to solder the thermal pad to the PCB.
b. Use thermal material filling the air gap in between the thermal pad and the PCB.

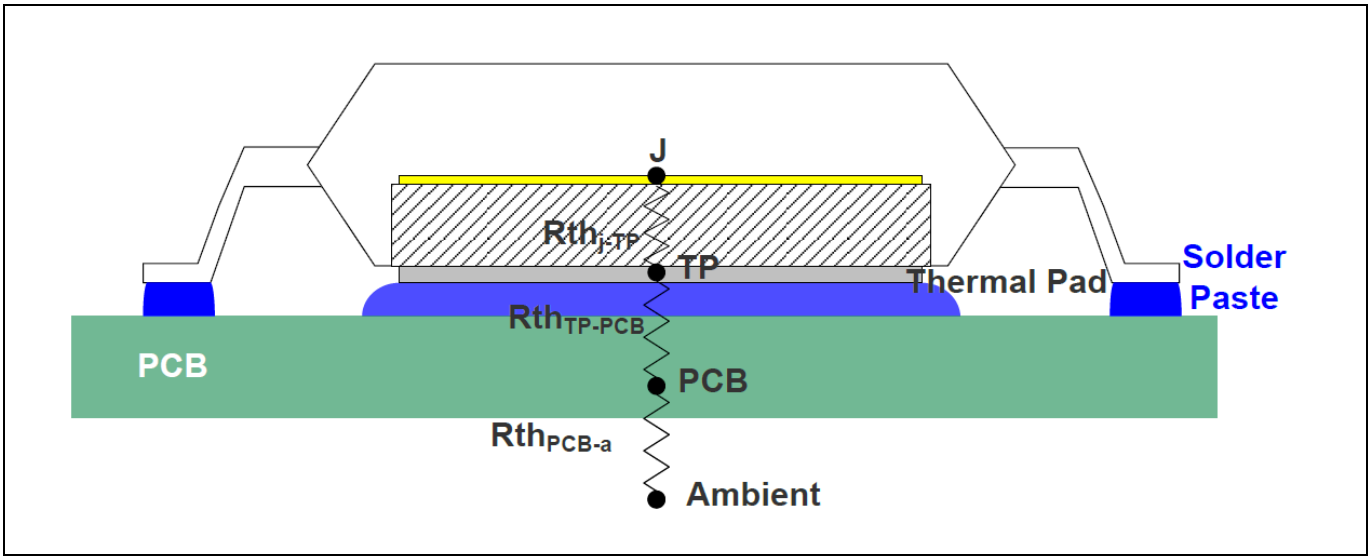


Figure 8 Steady state equivalent thermal circuit

5.6 Square input pulse distortion

The following chapter provides a characterization of pulse width distortion. This is defined as the ratio between the output pulse width with respect to input pulse width. Characterization is done with no load on OUTA and OUTB and it is applicable to both INA, INB and EN input pulses.

Figure 9 and Figure 10 show the output pulse length with respect to input pulse length. In particular, Figure 10 describes the pulse distortion in case of a short turn-on input pulse (e.g. low duty cycle condition); while Figure 11 shows the pulse distortion in case of a turn-off input pulse (e.g. high duty cycle condition).

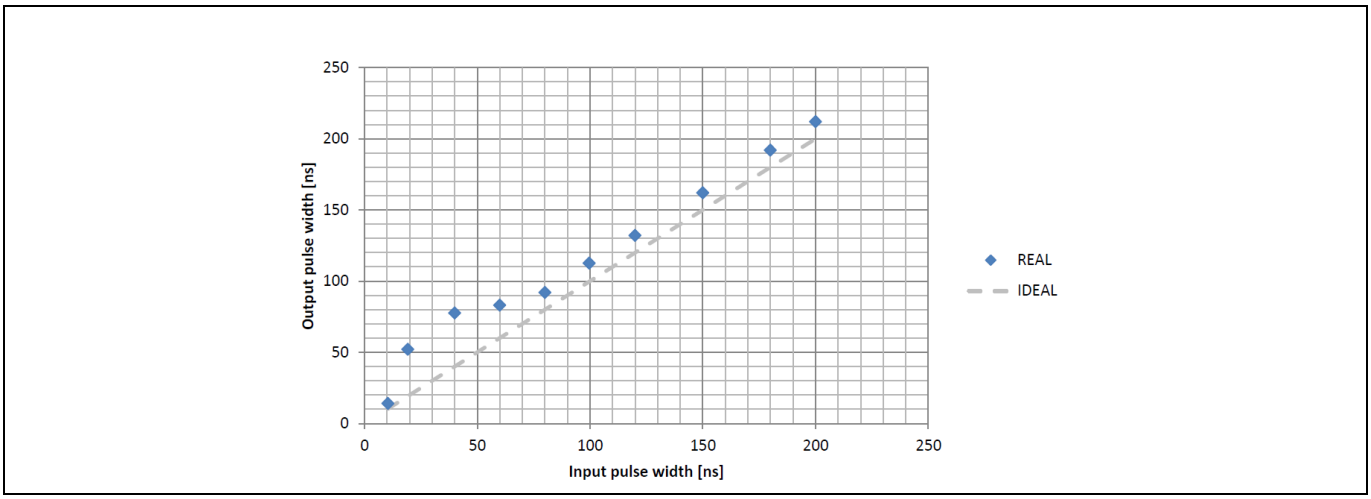


Figure 9 Output pulse distortion in case of a short turn-on input pulse

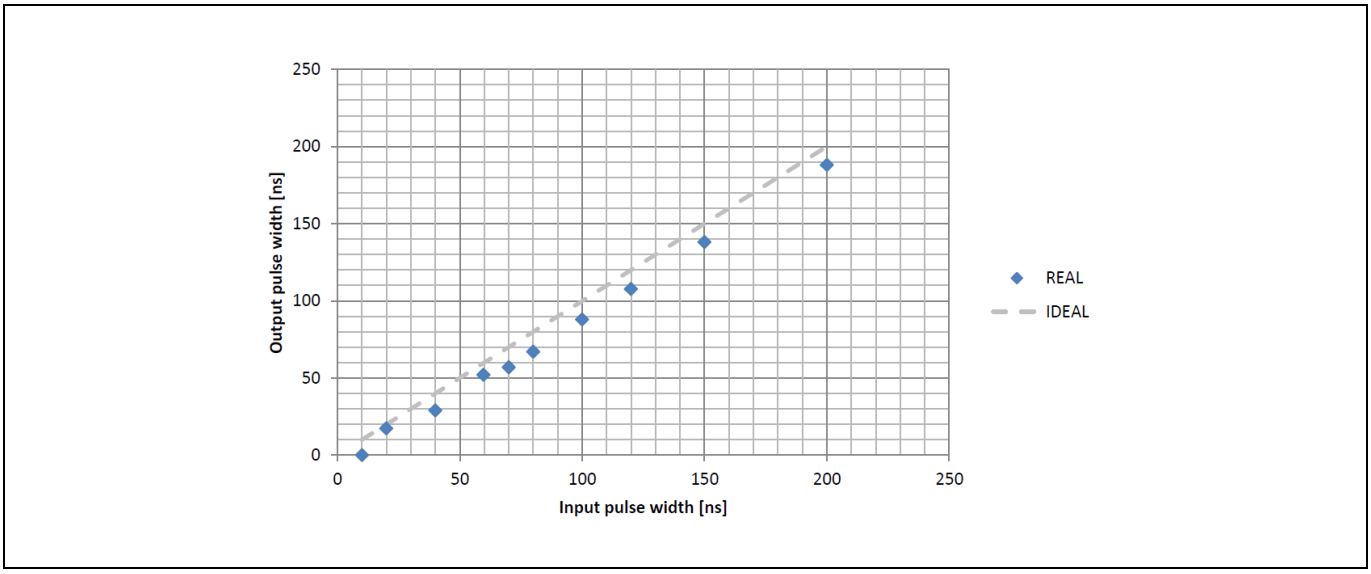


Figure 10 Output pulse distortion in case of a short turn-off input pulse

5.7 Bypass capacitor

The bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply source and it minimizes the noise generated by the switching of the outputs. It is recommended to place the bypass capacitor as close as possible to the gate driver in order to improve its effectiveness by reducing the effect of parasitic inductance of PCB lines.

The value of bypass capacitor is related to:

a. The current that the gate driver has to provide to the OUTA/B loads during turn-on switching condition;
b. The speed at which the output pin is driven;
c. The maximum allowed drop on power supply pins.

For instance, if it considered that outputs OUTA and OUTB provide 6 A source current with 20 ns rise time and the maximum wished drop on VCC pin is 0.1 V, then the bypass capacitance can be calculated as:

$$C = n * I \frac{\Delta T}{\Delta V} = 2 * 6\,A \frac{20\,ns}{0.1\,V} = 2.4\,\mu F \quad (6)$$

5.8 Additional Details

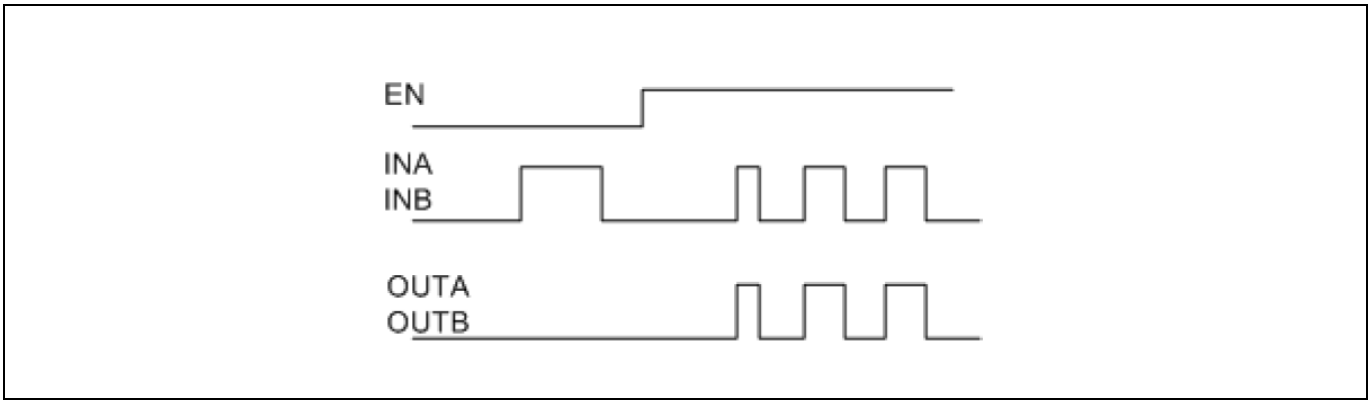


Figure 11 Input/output Timing Diagram

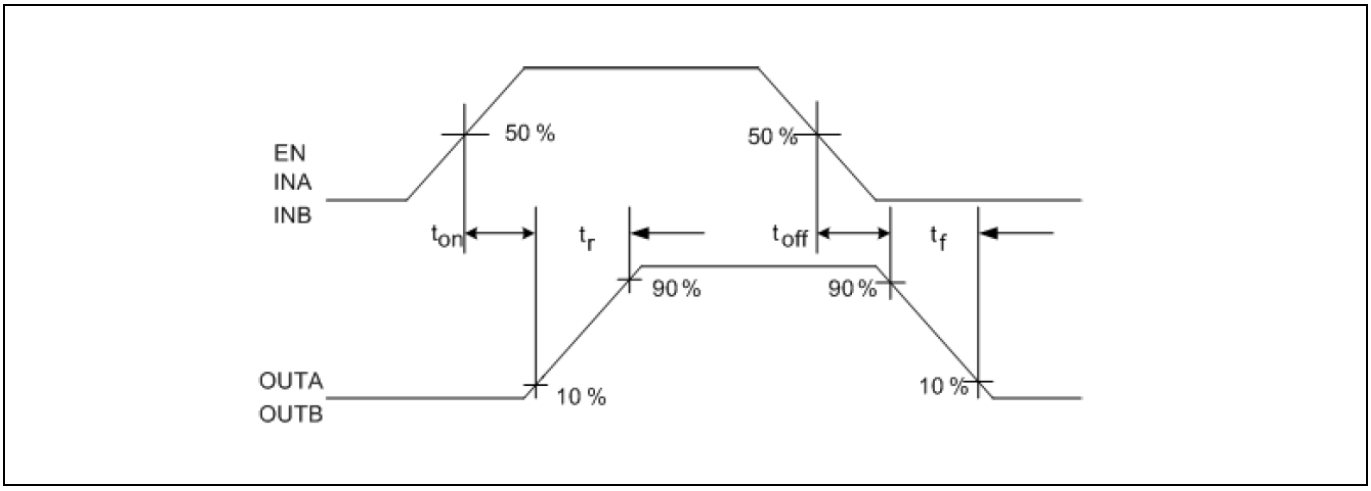
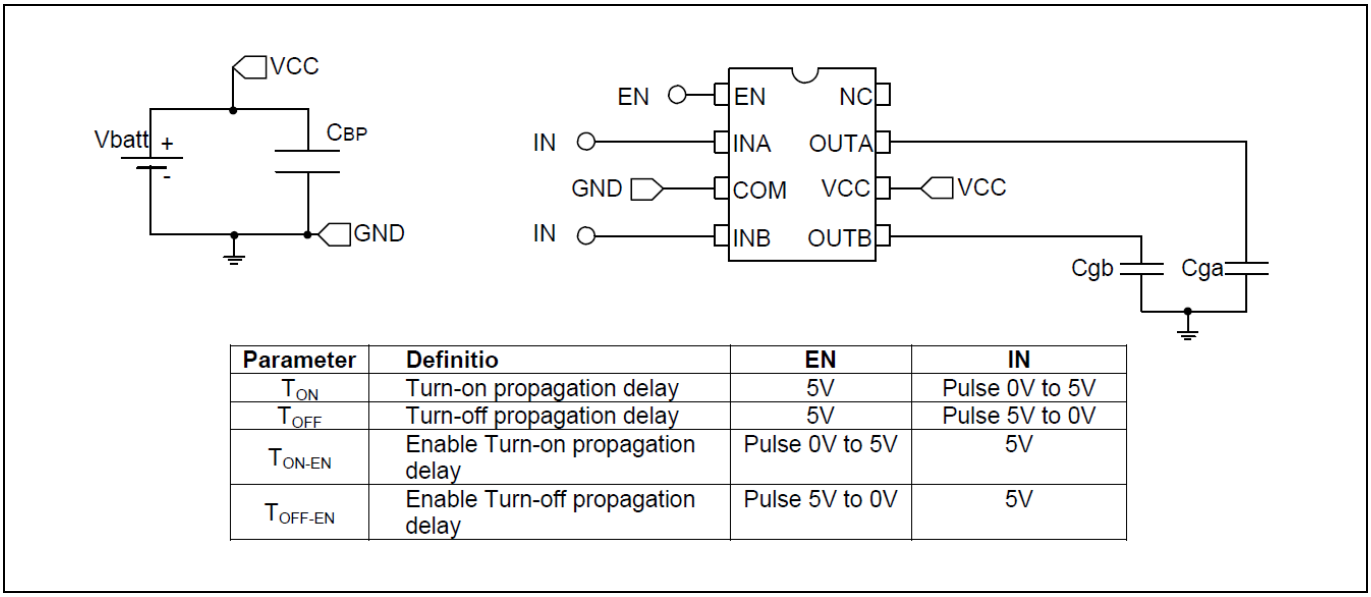


Figure 12 Switching Time Waveform Definitions



Parameter	Definitio	EN	IN
T_{ON}	Turn-on propagation delay	5V	Pulse 0V to 5V
T_{OFF}	Turn-off propagation delay	5V	Pulse 5V to 0V
T_{ON-EN}	Enable Turn-on propagation delay	Pulse 0V to 5V	5V
T_{OFF-EN}	Enable Turn-off propagation delay	Pulse 5V to 0V	5V

Figure 13 Switching time test circuit and test conditions

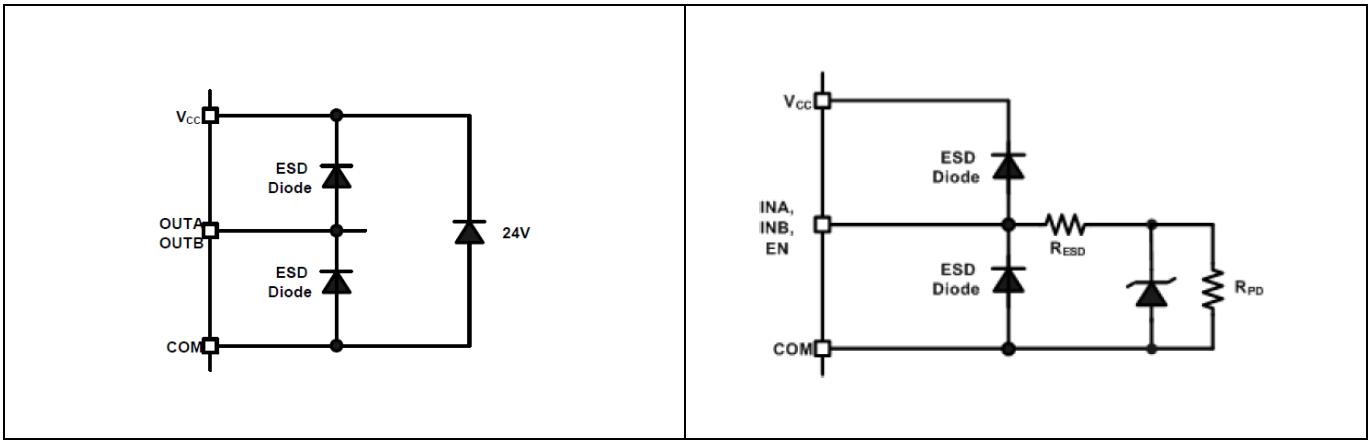


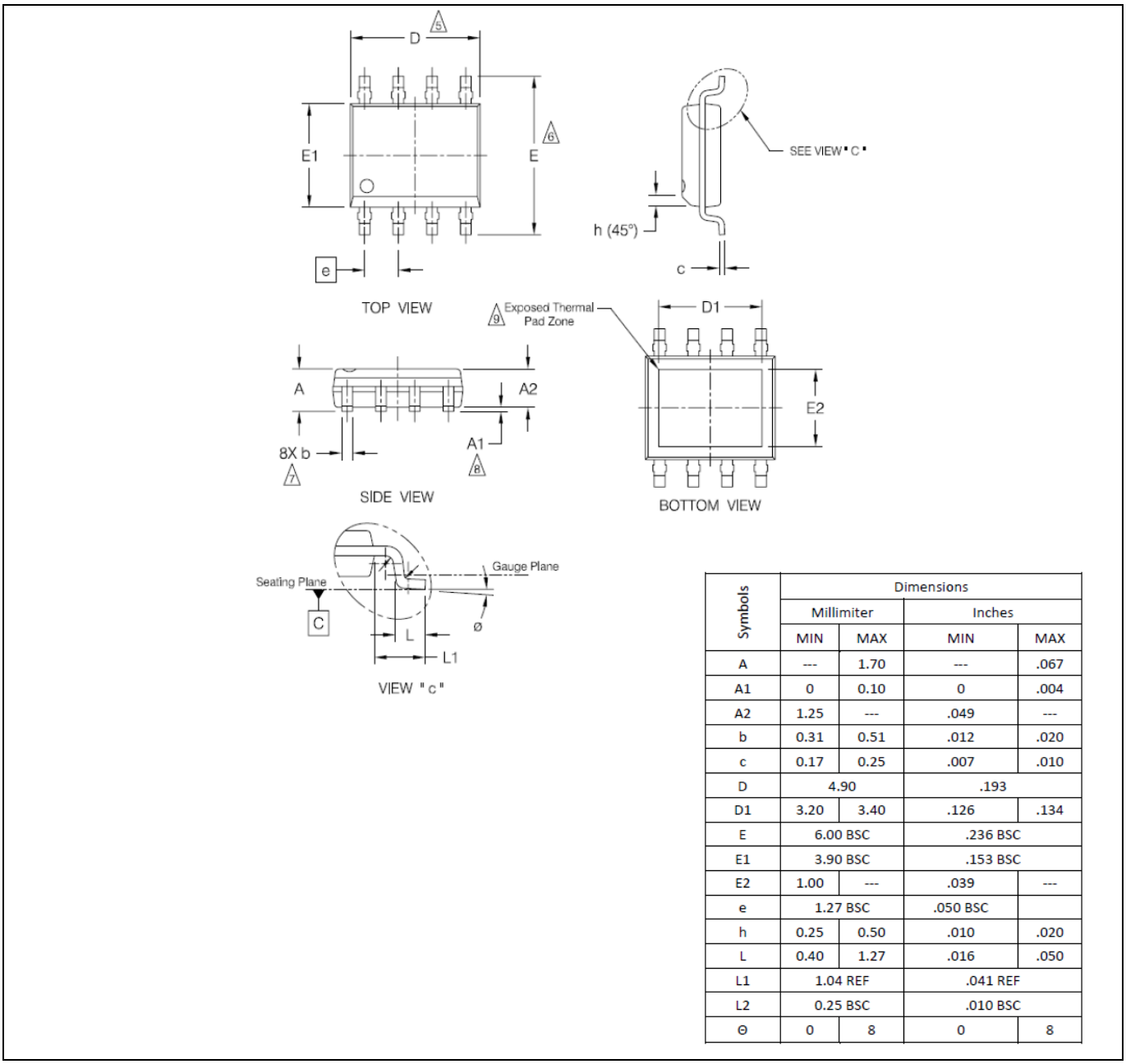
Figure 14 Input/Output/Enable pin equivalent circuit diagrams

6 Qualification information

Qualification level		Industrial [1)] Comments: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.
Moisture sensitivity level		MSL3 [2)] 260°C (per JEDEC standard J-STD-020)
ESD	Charged device model	1000 V (Class C3) (per ANSI/ESDA/JEDEC standard JS-002)
	Human body model	2 kV (per ANSI/ESDA/JEDEC standard JS-001)
IC latch-up test		Class II, Level A (per JESD78)
RoHS compliant		Yes

1) Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
2) Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

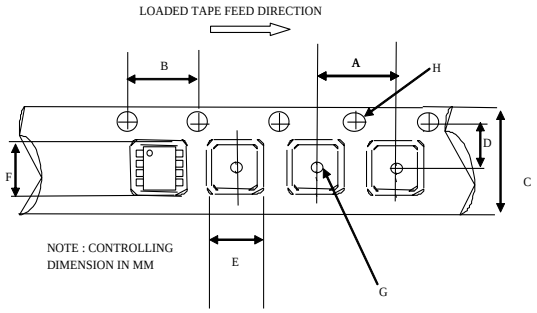
7 Package details



Symbols	Dimensions			
	Millimiter		Inches	
	MIN	MAX	MIN	MAX
A	---	1.70	---	.067
A1	0	0.10	0	.004
A2	1.25	---	.049	---
b	0.31	0.51	.012	.020
c	0.17	0.25	.007	.010
D	4.90		.193	
D1	3.20	3.40	.126	.134
E	6.00 BSC		.236 BSC	
E1	3.90 BSC		.153 BSC	
E2	1.00	---	.039	---
e	1.27 BSC		.050 BSC	
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
L1	1.04 REF		.041 REF	
L2	0.25 BSC		.010 BSC	
Θ	0	8	0	8

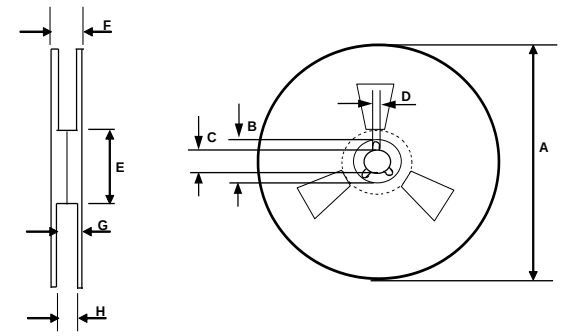
Figure 15 8 - Lead Power Pad DSO (2ED24427N01F)

7.1 Tape and reel details: PG-DSO8-900



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 16 Tape and reel details

7.2 Part marking information

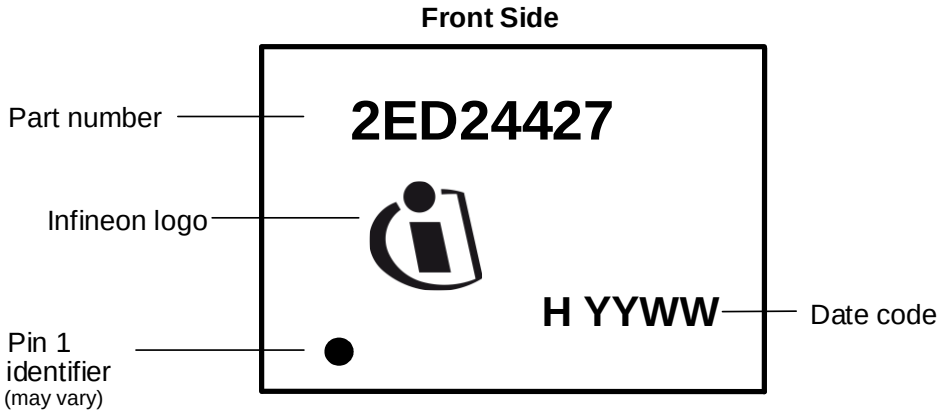


Figure 17 Marking information PG-DSO-900 (Power Pad-DSO-8)

8 Related products

Channels	Typ. gate drive (Io+/Io-)	Part number	Max supply voltage	UVLO (on/off)	Typ. prop. delay (on/off)	Logic	Package options
	A		V	V	ns		
1	0.3 / 0.5	IR44252L	20	5 / 4.15	50 / 50	Single non-inverting channel Dual OUT pins	SOT23-5L
	1.5 / 1.5	IRS44273L	25	10.2 / 9.2	50 / 50	Single non-inverting channel Dual OUT pins	SOT23-5L
		IR44273L	20	5 / 4.15	50 / 50	Single non-inverting channel Dual OUT pins	SOT23-5L
		IR44272L	20	5 / 4.15	50 / 50	Single non-inverting channel ENABLE	SOT23-5L
	0.8 / 1.75	1ED44176	25	11.9/11.4	50 / 50	Single non-inverting channel OCP (+CS), fault out and ENABLE	PG-DSO-8
	2.6 / 2.6	1ED44175	25	11.9/11	50 / 50	Single non-inverting channel OCP, fault out and ENABLE	PG-SOT23-6-2
		1ED44173	25	8 / 7.3	34 / 34	Single non-inverting channel OCP, fault out and ENABLE	PG-SOT23-6-2
2	2.3 / 3.3	IRS4426S	25		50 / 50	Dual inverting channels	SOIC-8L
		IRS44262S	20	10.2 / 9.2	50 / 50	Dual inverting channels	SOIC-8L
		IRS4427S	25		50 / 50	Dual non-inverting channels	SOIC-8L
		IRS4428S	25		50 / 50	Single inverting channel Single non-inverting channel	SOIC-8L

9 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs

9.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

10 Revision history

Document version	Date of release	Description of changes
2.00	November 10, 2019	Final Datasheet

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