RAA271050

4A, High Efficiency Synchronous Buck Regulator for Automotive Applications

The RAA271050 is an automotive grade (AEC Q-100 Grade 1) 4A synchronous step down voltage regulator with integrated high-side and low-side MOSFETs. The output voltage of this buck regulator is fixed to either 5.0V/3.3V. With an input voltage range of 4.5V to 42V it provides a high-efficiency solution for a variety of point of load applications.

The RAA271050 works as a primary regulator and companion product with the RAA271000 system PMIC, whose target application is the R-CAR V3H processor, where a high performance complete power solution is required.

The RAA271050 uses peak current mode control and this coupled with the high 2.2MHz fixed frequency provide component selection flexibility to minimize the total solution size. For applications where solution size is flexible, a 440kHz fixed frequency option is available which provides higher efficiency.

The RAA271050 protection features include over -current, UVLO, output over-voltage, under-voltage, and thermal overload protection.

The RAA271050 implements safety monitoring features that ensure that the output voltage and temperature are all within their expected ranges of operation. This IC also implements dual bandgaps/reference voltages to ensure that the monitoring systems have a reference, which is separate to the reference that the regulator is using.

Features

- AEC-Q100 qualified, Grade 1: -40°C to +125°C
- Supports ASIL C Systems
- V_{IN} operating range from 4.0V to 42V
- V_{OUT} = 5.0V or 3.3V (factory programmable)
- High efficiency synchronous buck regulator with efficiency up to:
  - 95%; V_{IN} = 12V; V_{OUT} = 5V; F = 440kHz
  - 92%; V_{IN} = 12V; V_{OUT} = 5V; F = 2.2MHz
- 2% V_{OUT} accuracy over temperature, load, line
- Factory programmable soft-start
- Soft-stop output discharge during disable
- RSTb output which doubles as Monitor fault or Buck Fault Indicator
- Fixed switching frequency: 2.2MHz or 440kHz
- Spread Spectrum Modulation (SSM), pseudo-random frequency and dwell time
  - Enable/disable
  - Frequency modulation ±1%, ±2%, ±3%,
  - Upward/centered/downward modulation
- Boot UVLO

Applications

- Automotive power
- R-CAR processor PMICs
- DC/DC POL modules

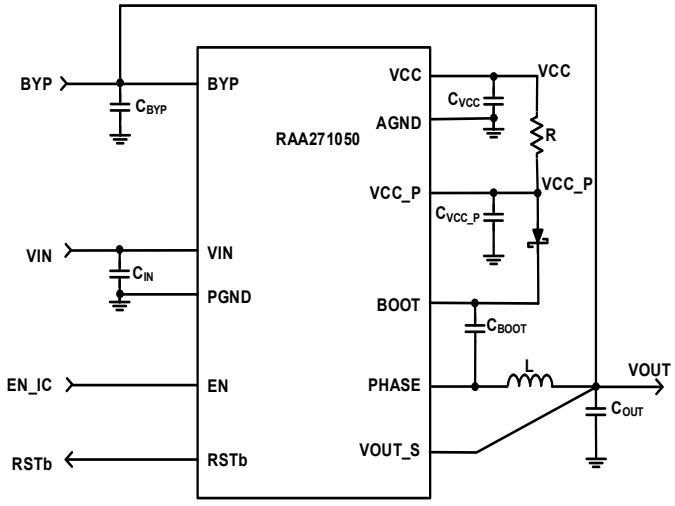


Figure 1. Typical Application Diagram

1. Overview

1.1 Typical Application Schematic - 2.2MHz Switching Frequency

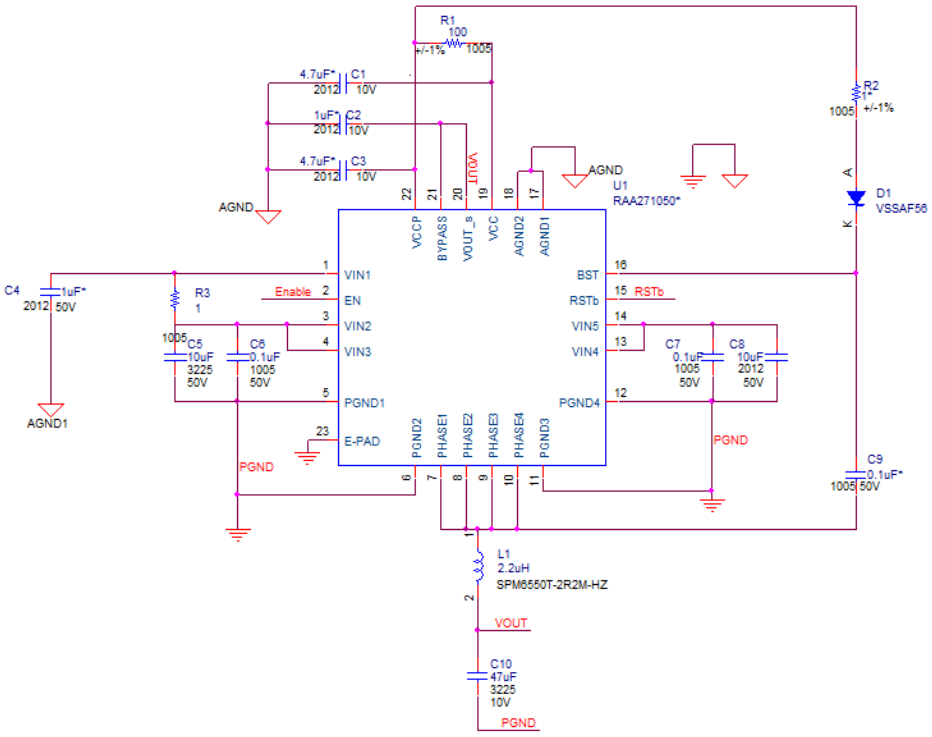


Figure 2. 2.2MHz Switching Frequency Schematic

1.2 Typical Application Schematic - 440kHz Switching Frequency

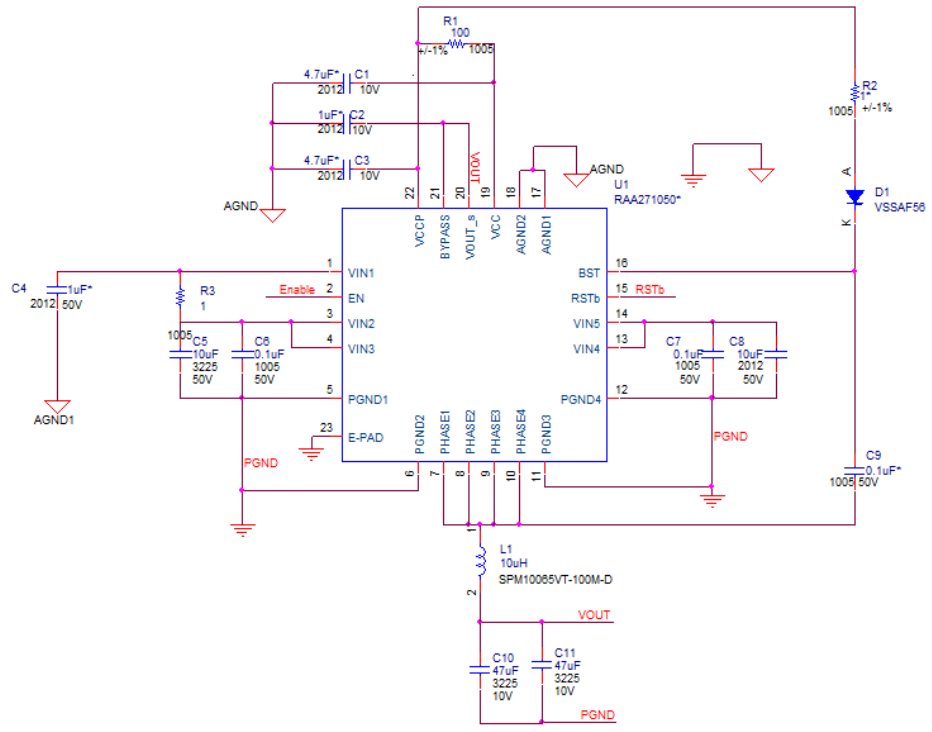


Figure 3. 440kHz Switching Frequency Schematic

1.3 Target Application

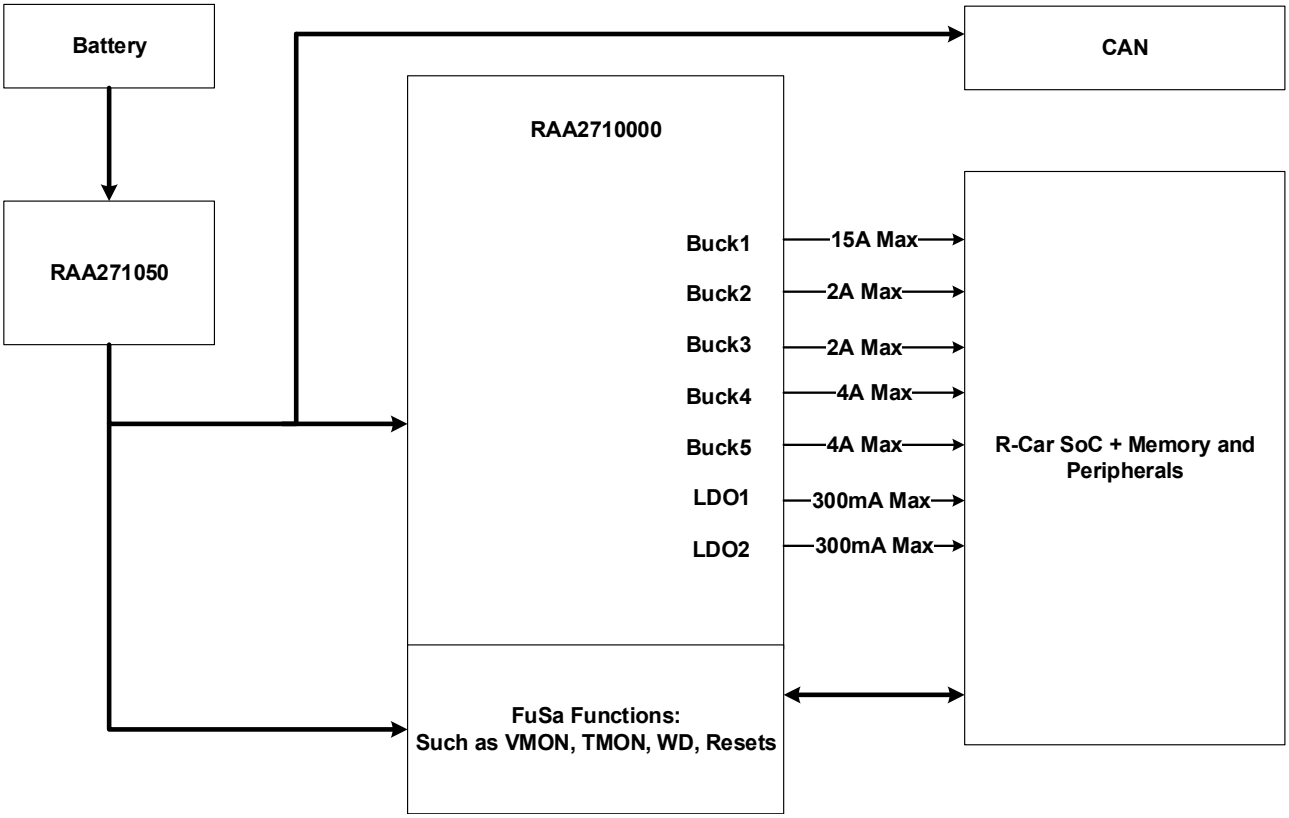


Figure 4. Target Application

1.4 Block Diagram

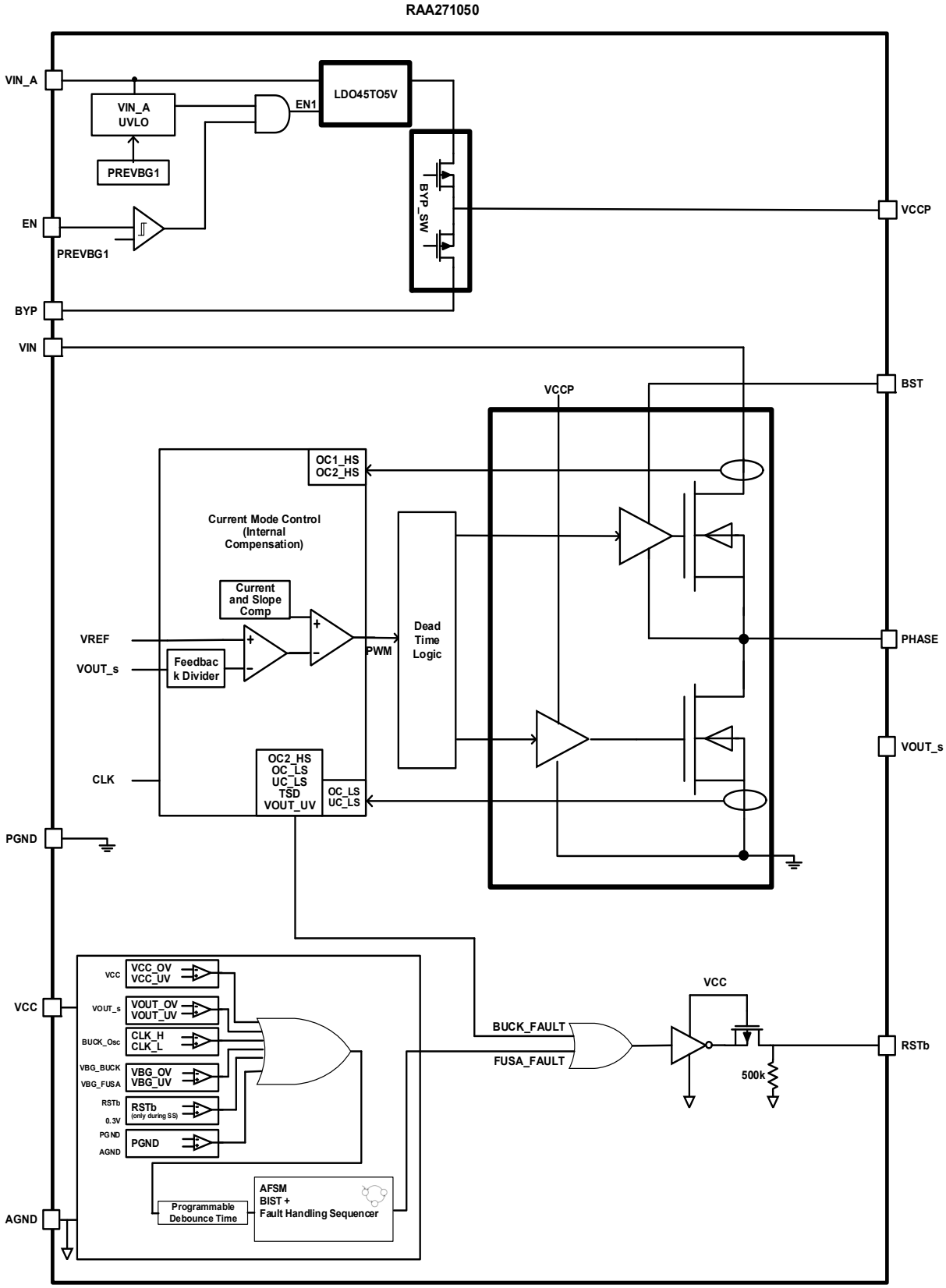
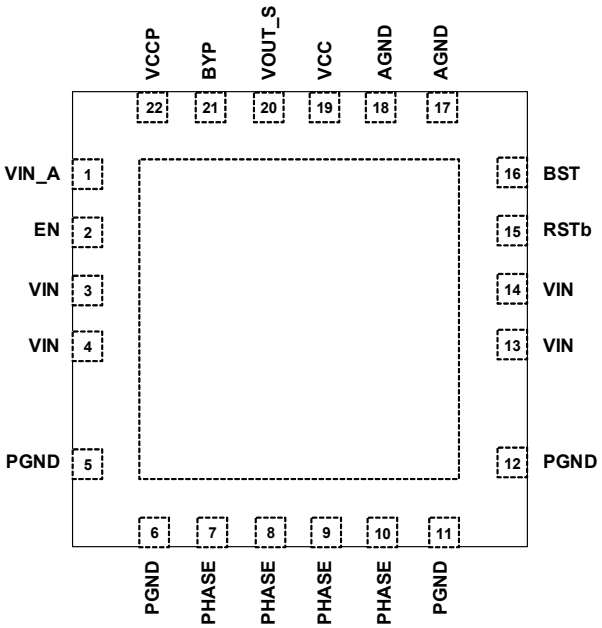


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Configurations

22 Ld QFN
Top View



2.2 Pin Descriptions

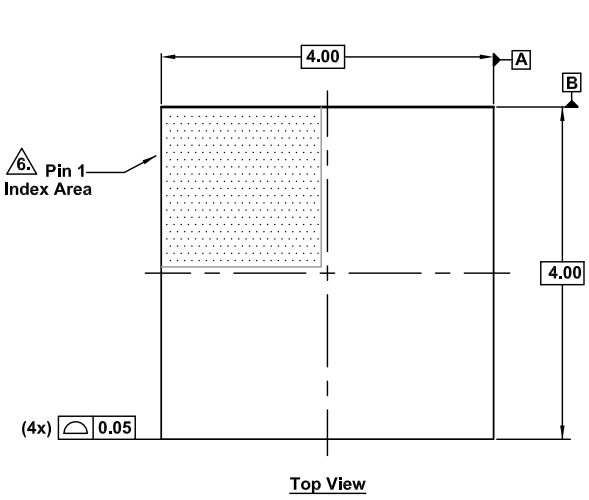
Pin Number	Pin Name	Description
1	VIN_A	Input supply voltage for the internal LDO (VCCP). Connect through 1 Ohm resistor to VIN pin, and place 1µF capacitor for filtering.
2	EN	Enable control input. EN is a threshold-sensitive enable input to the chip. When EN > 1.2V (typical), the VCCP LDO is activated and IC circuits are powered-up, and the device goes into standby and no switching occurs. When EN > 1.85V (typical), buck begins switching. When EN falls below 0.45V, the IC is disabled and all fault states are cleared. EN can be tied to VIN for automatic startup.
3, 4, 13, 14	VIN	Supply input for the IC and Buck switching regulator. VIN supplies the high-side MOSFET of the Buck switching regulator and also supplies the internal VCCP regulator that powers IC circuits. Place a 10µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor from VIN to PGND and as close as possible to the IC for minimum switching loop and smallest spikes due to fast switching.
5, 6, 11, 12	PGND	Provides the return path for the low-side MOSFET. This pin carries a noisy driving current, so the traces connecting from this pin to the low-side MOSFET source and VCC decoupling capacitor ground pad should be as short as possible. All the sensitive analog signal traces should not share common traces with this driver return path. Connect this pin to the ground copper plane (wiring away from the IC instead of connecting through the IC bottom PAD) through several vias as close as possible to the IC.
7, 8, 9, 10	PHASE	Switching node of Buck. PHASE is the connection point of the high-side N-channel MOSFET and low-side N-channel MOSFET switches of Buck that drive the Buck inductor. PHASE is a high-dV/dt node that should be isolated from sensitive traces as much as possible.
15	RSTb	System reset output. The RSTB is an active low/active high output that provides a hard reset-low signal to the system MCU when an output fault occurs. Faults that trigger the RSTB output are listed in “RSTB” on page xx. Note: When the RSTB output is high, it is internally driven to the a diode below the VCC voltage.

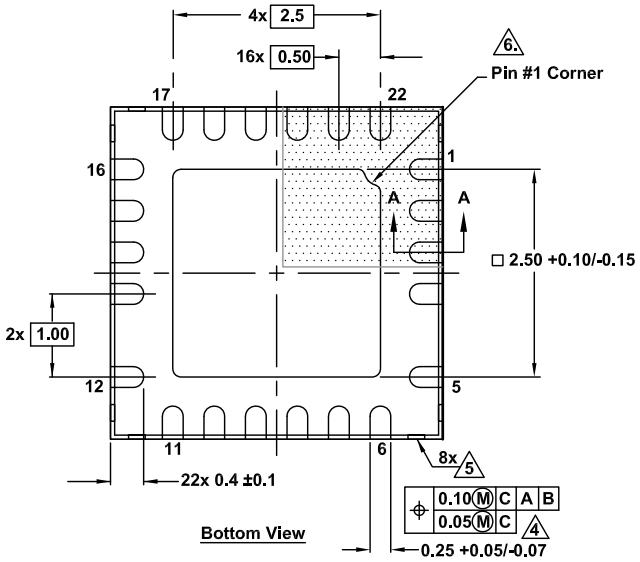
Pin Number	Pin Name	Description
16	BST	Buck high-side MOSFET driver supply. BST provides bias voltage for the Buck high-side MOSFET driver. An internal bootstrap circuit creates a voltage between BST and PHASE suitable to drive the Buck internal high-side N-channel MOSFET. Renesas recommends placing a 0.1µF ceramic capacitor between the BST and PHASE pins. The internal bootstrap circuit recharges the boot capacitor when the Buck low-side switch is on. BST is a high-dV/dt node that should be isolated from sensitive traces as much as possible. Provides bias voltage to the high-side MOSFET driver. The VCCP (internal LDO) provides the bias to BST through a fast switching diode.
17	AGND	Analog ground connection for internal VCCP regulator
18	AGND	Analog ground connection for VCC Monitor bias supply
19	VCC	Monitor bias supply. The VCC operating range is 3.3V to 5.5V. A 100Ω resistor between VCCP and VCC along with a minimum 10µF decoupling ceramic capacitor should be used between VCC and PGND
20	VOUT_s	Buck output voltage feedback input. Connect VOUT_s to the output of Buck to provide the feedback sense voltage for the Buck regulator. An internal resistor divider at FB sets the output voltage. The Buck output voltage is factory-programmable to either be 3.3V or 5V. Route the VOUT_s trace away from noisy or high-dV/dt signals. This pin is discharged by a 100Ω pull-down resistor when the device is disabled
21	BYP	Bypass/output node of the internal linear regulator that supplies the bias voltage for the IC, including Buck drivers, BST capacitor, and most of the internal circuits. The BYP operating range is typically 3V to 5.5V, nominally 4.3V. Use a minimum 1µF decoupling ceramic capacitor between this pin to ground plane close to PGND1. If BYP is not used, connect to GND.
22	VCCP	Output of the internal linear regulator that provides bias for the low-side driver, high-side driver (VCCP to connected to BST through a diode).
E-pad		E-pad must be soldered to a large ground plane on the PCB that does not contain noisy power flow. Use as many vias as possible in PAD to help reduce the θ_{JA} of the IC package. E-pad does not have an electrical connection.

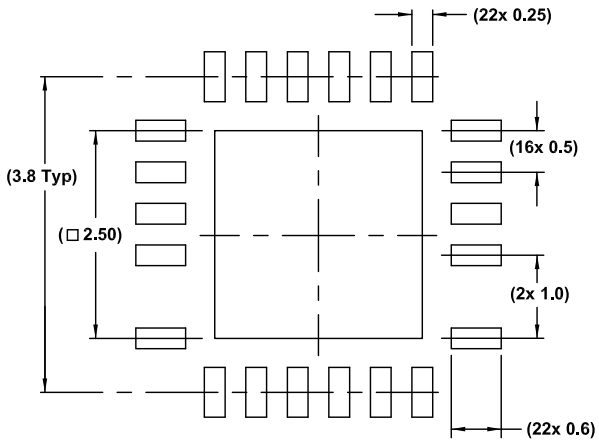
3. Package Outline Drawing

For the most recent package outline drawing, see L22.4x4.

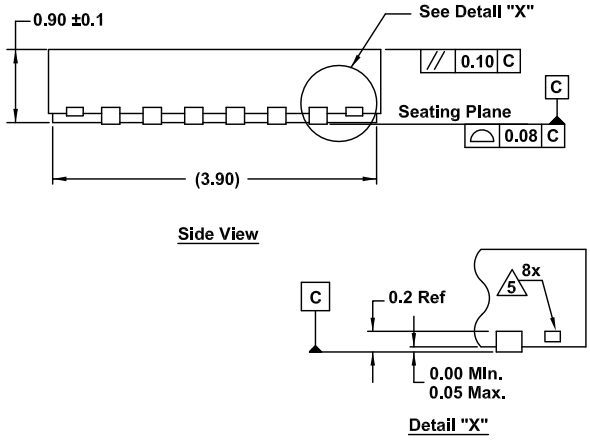
L22.4x4
22 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 0, 1/19





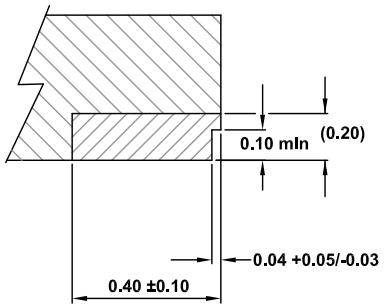


Typical Recommended Land Pattern



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



Section : A-A
Scale : NTS

4. Revision History

Rev.	Date	Description
1.0	Mar 26, 2021	Initial release

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