RYZ014A

LTE Category M1 Module

Description

The RYZ014A is a complete certified LTE Category M1 module including base-band, RF and memory, for the design of connected machine-to-machine devices, and other Internet-of-Things devices with embedded LTE connectivity. This document provides technical information about RYZ014A LGA module.

This document is intended for engineers who are developing User Equipment (UE) for LTE systems.

Functions

Renesas RYZ014A module includes Monarch SQN3330 Cat-M1 baseband, a complete dual band RF front end, memory and required circuitry to meet 3GPP E-UTRA (Long Term Evolution - LTE, Release 13) Cat-M1 UE specifications.

For more information on the core technology specifications see the section References on page 31. The term RYZ014A module refers to the hardware and the associated embedded software.

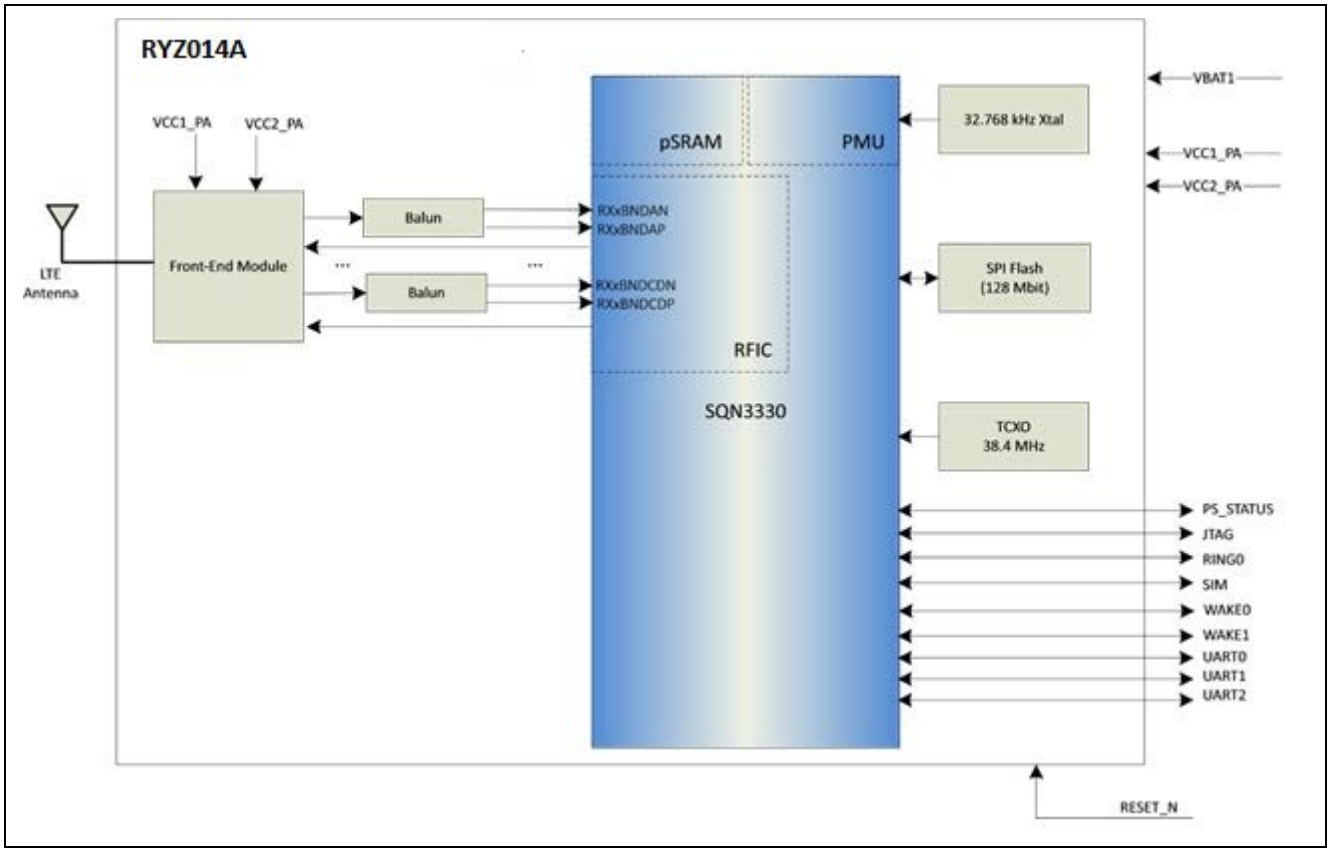

Figure 1. RYZ014A Block Diagram

Table 1 provides detail on general features of the RYZ014A.

Table 2 provides detail for the LTE-related features of the RYZ014. The module's ECCN and part number are detailed in the section ECCN and Part Number on page 15.

Table 1. General Features

Feature	Description
General interfaces	• JTAG • I2C (reserved) • USIM • SPI (reserved) • GPIO • UART (x3, including one reserved) • RING • WAKE • ADC • 32 kHz
Supported Frequency Bands	1, 2, 3, 4, 5, 8, 12, 13, 14, 17, 18, 19, 20, 25, 26, 28, 66, 85
Operation voltages	Vbat1 (range from 3.1 V to 5.5 V) operational Vbat1 (range from 3.1 V to 4.5 V) recommended for performance
Packaging	LGA module 108 pads (21.35 x 20.25 x 1.79 mm) RoHS compliant, halogen-free
Operating temperature	RF compliant -30°C to +85°C (measured on board thermistor) Operational: -40°C to +95°C (measured on board thermistor) See also section Environmental Operating Conditions on page 17.
Humidity	• 10% to 85% See also section Environmental Operating Conditions on page 17.

Table 2. LTE Features

Feature	Description
Standard compliance	• 3GPP E-UTRA Release 13 compliant
PHY	• One UL and one DL transceiver • Support of HD-FDD Duplexing • Category M1 UE • Channel 1.4 MHz bandwidth • Normal and extended cyclic prefix • Support of MPDCCH • Modulation • DL: QPSK, 16QAM • UL: QPSK, 16QAM • All coding schemes corresponding to modulations • All channel coding (turbo-coding with interleaver, tail biting convolutional coding, block and repetition coding) and CRC lengths • Sounding (including in special subframes) • Control and data in special subframes • All power control schemes and DL power allocation schemes • HARQ Incremental Redundancy and Chase Combining, with bundling or multi-plexing • Measurements and computations related to CQI (Channel Quality Indicator), PMI • (Pre-coding Matrix Indicator) and RI (Rank Indicator), RSRP, and RSRQ • UEPCOP (from 3GPP Release 12) Power Saving Mode

Feature	Description
MAC	• Random Access procedure in normal and special subframes • Scheduling Request, Buffer Status Reporting, and Power Headroom Reporting • Discontinuous reception (DRX, eDRX) with long and short cycles • Fast scanning • Hosted configuration • IPv4, IPv6 • RoHC • Location based services • Advanced QoS features
RLC	• ARQ modes: UM, AM, and TM
PDCP	• Ciphering and deciphering: NULL, AES (128-bit), SNOW 3G (128-bit) • Integrity and protection: AES (128-bit), SNOW 3G (128-bit)
RRC	• MIB and new SIB1bis • Intra and inter-frequency measurements and handover • Up to 8 Data Radio Bearers supported • Support of CE (Coverage Extension) Mode
NAS and above	• NAS • SMS over SG • LWM2M Client

Pin Description

Table 3. Pad Name and Function

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
1	GND	N/A	All GND pads shall be connected to the same copper.	
2	GPIO3/STATUS_LED	In	Reserved for future use. Do not connect.	status LED (STATUS_LED, OUT) in option
3	1V8	O (power)	1.8 V reference voltage for IOs.	
4	GNSS_VINB	N/A	Reserved, do not use. Do Not Connect	
5	RESERVED/FFF_FFH	I/O	Reserved pad: it must be Pulled Up and connected to a Test Point. FFF_FFH: Active high by default (FFF: Firmware From Flash). Firmware From Host if driven low.	

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
6	GPIO2/PS_STATUS	I/O	GPIO2: Reserved, no function. PS_STATUS: High = modem active / low = modem in low power modes.	Power Saving status of the module: a high level indicates that module is in active mode. A low level indicates that module is in low power modes (sleep mode or deep sleep mode) to minimize power consumption. This signal can be used to inform a host that the module needs to be waken-up with either RTS0, WAKE0 or WAKE1 signal before sending data or commands through one of the UART interface.
7	GPIO19/CLK0	I/O	Reserved for future use. Do not connect.	
8	GPIO27/CTS2	I/O	UART2/CTS (OUT). It is recommended to pull-up this pad with the application host processor supply as this pad will become high impedance when module is in low power mode. If not used, it should be connected to a Test Point (for debug). CTS2 is active low.	
9	3V0	O (power)	3.0 V power supply	
10	GPIO28/RTS2	I/O	UART2/RTS (IN). Host board shall drive this signal. See Module integration Guide for details. RTS2 is active low.	
11	3V0	O (power)	3.0 V power supply	
12	SIM_RESETN	O	SIM card interface: reset output pin for the SIM card	
13	DNC	Do not connect	Do not connect	
14	SIM_CLK	O	SIM card interface: clock output pin for the SIM card	
15	DNC	Do not connect		
16	SIM_DETECT	I/O	SIM card presence indication (input). GPIO in option. Active high = SIM card inserted / low = no SIM card inserted. Note: It is recommended to use an USIM connector with hardware removal and insertion detection capability, connected to SIM_DETECT signal.	

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
17	SIM_IO	I/O	SIM card bidirectional data input/output (SIM card output must be open-drain). A 4.7 kOhm pull-up resistor on SIM_VCC is mandatory.	
18	SIM_VCC	O (power)	SIM card supply voltage (1.8 V or 2.95V controlled by software). ON when a SIM card is detected.	
19	GNSS_TXD3	N/A	Reserved, do not use. Do Not Connect	
20	GND	N/A	All GND pads shall be connected to the same copper.	
21	GNSS_RXD3	N/A	Reserved, do not use. Do Not Connect	
22	GND	N/A	All GND pads shall be connected to the same copper.	
23	GNSS_BOOT0	N/A	Reserved, do not use. Do Not Connect	
24	GND	N/A	All GND pads shall be connected to the same copper.	
25	GNSS_RSTN	N/A	Reserved, do not use. Do Not Connect	
26	GND	N/A	All GND pads shall be connected to the same copper.	
27	GNSS_STDBY_OUT	N/A	Reserved, do not use. Do Not Connect	
28	GND	N/A	All GND pads shall be connected to the same copper.	
29	GNSS_WAKEUP	N/A	Reserved, do not use. Do Not Connect	
30	GND	N/A	All GND pads shall be connected to the same copper.	
31	GND	N/A	All GND pads shall be connected to the same copper.	
32	GND	N/A	All GND pads shall be connected to the same copper.	
33	GND	N/A	All GND pads shall be connected to the same copper.	
34	GND	N/A	All GND pads shall be connected to the same copper.	
35	GNSS_STDBYN	N/A	Reserved, do not use. Do Not Connect or tie to low.	
36	GNSS_GPIO28	N/A	Reserved, do not use. Do Not Connect	
37	GNSS_GPIO1_PPSOUT	N/A	Reserved, do not use. Do Not Connect	
38	GNSS_GPIO0/BLANKING	N/A	Reserved, do not use. Do Not Connect	
39	RFDATA12	I/O	Reserved for future use. Do not connect.	-
40	RFDATA16	I/O	Reserved for future use. Do not connect.	-
41	RFDATA17	I/O	Reserved for future use. Do not connect.	-
42	GND	N/A	All GND pads shall be connected to the same copper.	
43	GND	N/A	All GND pads shall be connected to the same copper.	
44	GNSS_ANT1	N/A	Reserved, do not use. Do Not Connect	

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
45	GND	N/A	All GND pads shall be connected to the same copper.	
46	GND	N/A	All GND pads shall be connected to the same copper.	
47	RESETN	I	Module HW reset signal. This shall be driven high (1V8). Active low (check the datasheet for the minimum duration).	
48	JTAG_TDO	O	JTAG active	
49	JTAG_TRSTN	I	Active low. JTAG active	
50	JTAG_TMS	I	JTAG active	
51	JTAG_TDI	I	JTAG active	
52	JTAG_TCK	I	JTAG active	
53	GND	N/A	All GND pads shall be connected to the same copper.	
54	LTE_ANT	Analog	LTE antenna	
55	GND	N/A	All GND pads shall be connected to the same copper.	
56	RXD2	O	UART2/RXD (OUT), if not used should be connected to a Test Point.	
57	ADC	Analog	Analog Digital Converter	
58	TXD2	I	UART2/TXD (IN), if not used should be connected to a Test Point.	
59	SPI_SDI	I/O	Reserved for future use. Do not connect.	-
60	SPI_CSN	I/O	Reserved for future use. Do not connect.	-
61	SPI_CLK	I/O	Reserved for future use. Do not connect.	-
62	GND	N/A	All GND pads shall be connected to the same copper.	
63	GND	N/A	All GND pads shall be connected to the same copper.	
64	GND	N/A	All GND pads shall be connected to the same copper.	
65	GND	N/A	All GND pads shall be connected to the same copper.	
66	GND	N/A	All GND pads shall be connected to the same copper.	
67	SPI_SDO	I/O	Reserved for future use. Do not connect.	-
68	GND	N/A	All GND pads shall be connected to the same copper.	
69	GND	N/A	All GND pads shall be connected to the same copper.	
70	GND	N/A	All GND pads shall be connected to the same copper.	
71	GND	N/A	All GND pads shall be connected to the same copper.	

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
72	GND	N/A	All GND pads shall be connected to the same copper.	
73	GND	N/A	All GND pads shall be connected to the same copper.	
74	GND	N/A	All GND pads shall be connected to the same copper.	
75	RTS0	I	UART0/RTS (IN). Active low (wake-up function).	
76	CTS0	O	UART0/CTS (OUT). It is recommended to pull-up this pad with the application host processor supply as this pad will become high impedance when module is in low power mode. CTS0 is active low.	
77	TXD0	I	UART0/TXD (IN)	
78	GPIO14/TXD1	I/O	UART1/TXD (IN); If not used should be connected to a Test Point.	
79	RXD0	O	UART0/RXD (OUT)	
80	GPIO15/RXD1	I/O	UART1/RXD (OUT); If not used should be connected to a Test Point.	
81	GPIO17/CTS1	I/O	GPIO17: Reserved, no function. CTS1 active low. No Flow control by default.	UART1/CTS (OUT)
82	GPIO38/CLK1	I/O	Reserved for future use. Do not connect.	
83	GPIO16/RTS1	I/O	GPIO16: Reserved, no function. RTS1 active low (wake-up function). No Flow control by default.	UART1/RTS (IN)
84	GPIO41/DTR0	I/O	Reserved for future use. Do not connect.	-
85	GPIO39/DSR0	I/O	Reserved for future use. Do not connect.	-
86	GND	N/A	All GND pads shall be connected to the same copper.	
87	GND	N/A	All GND pads shall be connected to the same copper.	
88	GPIO23/DCD0	I/O	Reserved for future use. Do not connect.	-
89	GPIO25/RING0	I/O	RING0 (OUT); it is recommended to pull-up this pin with the application host processor supply as it will become high impedance when module is in deep sleep mode. RING0 is active low (from high to low).	
90	GPIO40/EMGCY_SHDN	I/O	Reserved for future use. Do not connect.	-
91	GPIO26/CLK2	I/O	Reserved for future use. Do not connect.	

Pad#	Pad Name	Direction Capability	Default Function Description	Alternate Function Description (Contact Renesas Support Team for detail on persistent AT Commands availability)
92	I2C_SDA	I/O	Reserved for future use. Do not connect.	-
93	GPIO24	I/O	Reserved for future use. Do not connect.	
94	I2C_SCL	I/O	Reserved for future use. Do not connect.	-
95	GPIO21	I/O	Reserved for future use. Do not connect.	
96	WAKE1	I/O	Reserved, no function. Not set as a wake-up source by default. Active high or low level during 100 µs depending on software.	Wake input (WAKE1). Note: WAKE inputs are detected on level (configurable by software to 0 or 1) that must last at least 100 µs.
97	VCC1_PA	I (power)	Power supply for LTE RF front end; 2.9 V to 3.1 V.	
98	VCC2_PA	I (power)	Power supply for LTE RF front end; 2.9 V to 3.1 V.	
99	VCC2_PA	I (power)	Power supply for LTE RF front end; 2.9 V to 3.1 V.	
100	GNSS_VCC1	N/A	Reserved, do not use. Do Not Connect	
101	GNSS_VCC2	N/A	Reserved, do not use. Do Not Connect	
102	GNSS_VCC3	N/A	Reserved, do not use. Do Not Connect	
103	GPIO29/32KHZ_CLK_OUT	O	Reserved for future use. Do not connect.	
104	WAKE0	I	Reserved, no function. Not set as a wake-up source by default. Active high or low level during 100 µs depending on software.	Wake input (WAKE0). Note: WAKE inputs are detected on level (configurable by software to 0 or 1) that must last at least 100 µs.
105	GPIO42/SAR_DETECT	I/O	Reserved for future use. Do not connect.	
106	POWER_EN	I	Reserved, no function.	Connect to a 470 kOhm Pull Down when no used.
107	VBAT1	I (power)	Power supply for Baseband, voltage level 3.1 V to 5.5 V (operational) or 4.5 V (recommended for performance)	
108	VBAT1	I (power)	Power supply for Baseband, voltage level 3.1 V to 5.5 V (operational) or 4.5 V (recommended for performance)	
T1-T30	GND	N/A	T1 to T30 pads are used as both GND and thermal drops.	T1 to T30 pads are used as both GND and thermal drops.

Table 4. Other Pad Properties

Pad#	Pad Name	IO Power Group	Pad Type	Drive (mA)	Max drive strength that will be used (mA)	Max toggling freq (all modes) (MHz)	State @reset
1	GND	N/A	N/A	N/A	N/A	N/A	N/A
2	GPIO3/STATUS_LED	VBAT1	BIDIR_WAKE	N/A	N/A	N/A	In, HiZ
3	1V8	N/A	N/A	N/A	N/A	N/A	N/A
4	GNSS_VINB	N/A	N/A	N/A	N/A	N/A	N/A
5	RESERVED/FFF_FFH	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
6	GPIO2/PS_STATUS	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
7	GPIO19/CLK0	1V8	BIDIR	2	4	6.25	In, PU
8	GPIO27/CTS2	1V8	BIDIR	2	4	6.25	In, PU
9	3V0	N/A	N/A	N/A	N/A	N/A	N/A
10	GPIO28/RTS2	1V8	BIDIR	2	4	6.25	In, PU
11	3V0	N/A	N/A	N/A	N/A	N/A	N/A
12	SIM_RESETN	SIM_VCC	BIDIR	2	4	1	In, HiZ
13	DNC	N/A	N/A	N/A	N/A	N/A	N/A
14	SIM_CLK	SIM_VCC	BIDIR	2	4	1	In, PU
15	DNC	N/A	N/A	N/A	N/A	N/A	N/A
16	SIM_DETECT	VBAT1	BIDIR_WAKE	N/A	N/A	N/A	In, HiZ
17	SIM_IO	SIM_VCC	BIDIR	2	4	1	In, PU
18	SIM_VCC	VBAT1	Power	N/A	N/A	N/A	High-Z, PD
19	GNSS_TXD3	N/A	N/A	N/A	N/A	N/A	N/A
20	GND	N/A	N/A	N/A	N/A	N/A	N/A
21	GNSS_RXD3	N/A	N/A	N/A	N/A	N/A	N/A
22	GND	N/A	N/A	N/A	N/A	N/A	N/A
23	GNSS_BOOT0	N/A	N/A	N/A	N/A	N/A	N/A
24	GND	N/A	N/A	N/A	N/A	N/A	N/A
25	GNSS_RSTN	N/A	N/A	N/A	N/A	N/A	N/A
26	GND	N/A	N/A	N/A	N/A	N/A	N/A
27	GNSS_STDBY_OUT	N/A	N/A	N/A	N/A	N/A	N/A
28	GND	N/A	N/A	N/A	N/A	N/A	N/A
29	GNSS_WAKEUP	N/A	N/A	N/A	N/A	N/A	N/A
30	GND	N/A	N/A	N/A	N/A	N/A	N/A
31	GND	N/A	N/A	N/A	N/A	N/A	N/A
32	GND	N/A	N/A	N/A	N/A	N/A	N/A
33	GND	N/A	N/A	N/A	N/A	N/A	N/A
34	GND	N/A	N/A	N/A	N/A	N/A	N/A
35	GNSS_STDBYN	N/A	N/A	N/A	N/A	N/A	N/A
36	GNSS_GPIO28	N/A	N/A	N/A	N/A	N/A	N/A
37	GNSS_GPIO1_PPSOUT	N/A	N/A	N/A	N/A	N/A	N/A
38	GNSS_GPIO0/BLANKING	N/A	N/A	N/A	N/A	N/A	N/A
39	RFDATA12	N/A	N/A	N/A	N/A	N/A	N/A
40	RFDATA16	N/A	N/A	N/A	N/A	N/A	N/A
41	RFDATA17	N/A	N/A	N/A	N/A	N/A	N/A
42	GND	N/A	N/A	N/A	N/A	N/A	N/A
43	GND	N/A	N/A	N/A	N/A	N/A	N/A

Pad#	Pad Name	IO Power Group	Pad Type	Drive (mA)	Max drive strength that will be used (mA)	Max toggling freq (all modes) (MHz)	State @reset
44	GNSS_ANT1	N/A	N/A	N/A	N/A	N/A	N/A
45	GND	N/A	N/A	N/A	N/A	N/A	N/A
46	GND	N/A	N/A	N/A	N/A	N/A	N/A
47	RESETN	VBAT1	IN_PMU	N/A	N/A	0	In, HiZ
48	JTAG_TDO	1V8	BIDIR	12	12	5	Out
49	JTAG_TRSTN	1V8	IN	N/A	N/A	N/A	in, PD
50	JTAG_TMS	1V8	IN	N/A	N/A	5	In, PU
51	JTAG_TDI	1V8	IN	N/A	N/A	5	In, PU
52	JTAG_TCK	1V8	IN	N/A	N/A	10	In, PD
53	GND	N/A	N/A	N/A	N/A	N/A	N/A
54	LTE_ANT	N/A	N/A	N/A	N/A	N/A	N/A
55	GND	N/A	N/A	N/A	N/A	N/A	N/A
56	RXD2	1V8	BIDIR	2	4	6.25	In, PU
57	ADC	N/A	N/A	N/A	N/A	N/A	N/A
58	TXD2	1V8	BIDIR	2	4	6.25	In, PU
59	SPI_SDI	1V8	BIDIR	2	4	13	In, PU
60	SPI_CSN	1V8	BIDIR	2	4	13	In, PU
61	SPI_CLK	1V8	BIDIR	2	8	13	In, PU
62	GND	N/A	N/A	N/A	N/A	N/A	N/A
63	GND	N/A	N/A	N/A	N/A	N/A	N/A
64	GND	N/A	N/A	N/A	N/A	N/A	N/A
65	GND	N/A	N/A	N/A	N/A	N/A	N/A
66	GND	N/A	N/A	N/A	N/A	N/A	N/A
67	SPI_SDO	1V8	BIDIR	2	4	13	In, PU
68	GND	N/A	N/A	N/A	N/A	N/A	N/A
69	GND	N/A	N/A	N/A	N/A	N/A	N/A
70	GND	N/A	N/A	N/A	N/A	N/A	N/A
71	GND	N/A	N/A	N/A	N/A	N/A	N/A
72	GND	N/A	N/A	N/A	N/A	N/A	N/A
73	GND	N/A	N/A	N/A	N/A	N/A	N/A
74	GND	N/A	N/A	N/A	N/A	N/A	N/A
75	RTS0	VBAT1	BIDIR_WAKE	N/A	N/A	N/A	In, HiZ
76	CTS0	1V8	BIDIR	2	4	6.25	In, PU
77	TXD0	1V8	BIDIR	2	4	6.25	In, PU
78	GPIO14/TXD1	1V8	BIDIR	2	4	6.25	In, PU
79	RXD0	1V8	BIDIR	2	4	6.25	In, PU
80	GPIO15/RXD1	1V8	BIDIR	2	4	6.25	In, PU
81	GPIO17/CTS1	1V8	BIDIR	2	4	6.25	In, PU
82	GPIO38/CLK1	1V8	BIDIR	2	4	6.25	In, PU
83	GPIO16/RTS1	VBAT1	BIDIR_WAKE	N/A	N/A	4	In, HiZ
84	GPIO41/DTR0	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
85	GPIO39/DSR0	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
86	GND	N/A	N/A	N/A	N/A	N/A	N/A
87	GND	N/A	N/A	N/A	N/A	N/A	N/A
88	GPIO23/DCD0	1V8	BIDIR	2	4	1	In, PU
89	GPIO25/RING0	VBAT1	BIDIR_WAKE			0	In, HiZ
90	GPIO40/EMGCY_SHDN	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ

Pad#	Pad Name	IO Power Group	Pad Type	Drive (mA)	Max drive strength that will be used (mA)	Max toggling freq (all modes) (MHz)	State @reset
91	GPIO26/CLK2	1V8	BIDIR	2	4	6.25	In, PU
92	I2C_SDA	1V8	BIDIR	2	8	6.25	In, PU
93	GPIO24	1V8	BIDIR	2	4	1	In, PU
94	I2C_SCL	1V8	BIDIR	2	8	6.25	In, PU
95	GPIO21	1V8	BIDIR	2	4	13	In, PU
96	WAKE1	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
97	VCC1_PA	N/A	N/A	N/A	N/A	N/A	N/A
98	VCC2_PA	N/A	N/A	N/A	N/A	N/A	N/A
99	VCC2_PA	N/A	N/A	N/A	N/A	N/A	N/A
100	GNSS_VCC1	N/A	N/A	N/A	N/A	N/A	N/A
101	GNSS_VCC2	N/A	N/A	N/A	N/A	N/A	N/A
102	GNSS_VCC3	N/A	N/A	N/A	N/A	N/A	N/A
103	GPIO29/32KHZ_CLK_OUT	1V8	BIDIR	2	8	0.032	In, HiZ
104	WAKE0	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
105	GPIO42/SAR_DETECT	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
106	POWER_EN	VBAT1	BIDIR_WAKE	N/A	N/A	0	In, HiZ
107	VBAT1	N/A	N/A	N/A	N/A	N/A	N/A
108	VBAT1	N/A	N/A	N/A	N/A	N/A	N/A
T1-T30	GND	N/A	N/A	N/A	N/A	N/A	N/A

FCC Regulatory Approval

Attention

FCC-ID: 2AU6XRZ014A (single modular approval)

This above identified LTE radio module is not intended to be provided to end-users but is for installation by OEM integrators only.

Installation/Integration

OEM integrators must follow Renesas' installation instructions to provide for and benefit from FCC compliant module integrations and must abide especially by the following:

The maximum antenna gain values (accounting for cable attenuation) to comply with the FCC maximum ERP/EIRP limits and with RF Exposure rules:

- LTE band 2 (1800 MHz): 2.1 dBi
- LTE band 4 (1700 MHz): 2 dBi
- LTE band 5 (850 MHz): 0.2 dBi
- LTE band 12 (700 MHz): -2 dBi
- LTE band 13 (700 MHz): -2.4 dBi
- LTE band 25 (1900+ MHz): 2.1 dBi

The Renesas module integration guidelines must be closely followed.

Compliance of host integrations of the module is limited to hosts adaptation designs which are identical to Renesas' reference design.

Host integrations with adaption designs deviating from Renesas' reference design require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Host integrations with co-located (simultaneously operating) radio transmitters must be evaluated in accordance with FCC multi-transmitter rules and may require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID, dependent on the result of the evaluation; Inquiry at FCC or a TCB is urgently recommended.

Integrations of the module into host products which are intended for portable use, i.e. less than 20cm distance between its radiating structures (antenna) and the body of nearby persons, or which otherwise put additional technical

requirements like Hearing Aid compatibility require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Compliance with Unwanted Emission Limits for Digital Device

If the OEM host integration fully complies with the above described reference design and can completely inherit and rest on compliance of the existing modular approval the OEM remains still responsible to show compliance of the overall end-product with the FCC limits for unwanted conducted and radiated emissions from the digital device (unintentional radio) portion of such end-product (commonly addressed as part 15B compliance or similar).

End-product Labelling

- FCC-ID
  The module's FCC-ID must either be visible from the exterior of the host product (e.g. per window) or per electronic display, or shall be displayed on an additional exterior label per the following or similar string:
  `contains FCC-ID: 2AU6XRYZ014A`
- Digital Device - Unwanted Emissions Notice
  If the end-product falls under part 15 of the FCC rules it shall display the following user notice on its exterior acc. to part 15.19 (the notice may be printed in the manual in case the host is too small):
  `This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:`
  `(1) This device may not cause harmful interference, and`
  `(2) This device must accept any interference received, including interference that may cause undesired operation.`
- Further Labelling Requirements may apply dependent on the FCC rule parts relevant to the host product.
- End-product User Instructions / Notices in the Manual
  At a minimum, end-product users must be provided with the following notices at a prominent location of the product literature furnished with the product:
  `Product Modifications`
  `* Modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.`
  `* RF Exposure Compliance`
  `This equipment complies with FCC radio frequency radiation exposure rules and limits set forth for an uncontrolled environment, when installed and operated with minimum distance of 20cm between its radiating structures (antenna) and the body of nearby persons and when not operated simultaneously with other nearby radio-transmitters.`
- Maximum Antenna Gain
  The user instructions of end-products equipped with standard external antenna connectors for the modular radio transmitter providing the option to connect other antennae than those which may or may not be bundled with the end-product must list the maximum allowed antenna gain values as derived from those given above, accounting for the cable attenuations of the actual installation.
- Digital Device - Unwanted Emissions Notice
  If the end-product is or contains a digital device (unintentional radio portions) and is not exempted by its use case (like vehicular use) the following part 15.105 (b) user notice shall be provided at prominent location of the product literature:
  `This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: o Reorient or relocate the receiving antenna. o Increase the separation between the equipment and receiver. o Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. o Consult the dealer or an experienced radio/TV technician for help`
- Further User Notices
  May be required dependent on the FCC rule parts relevant to the host product.
- Non-allowed User Instructions
  The end-product user guidance may NOT include instructions about how to install or de-install the module.

Industry Canada Statement

This device complies with ISED's licence exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co located with an y other transmitter or antenna

As long as 2 conditions above are met , further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmp lanté av ec un autre émetteur ou antenne.

Tant que les 2 conditions ci dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorizatio n is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: `"Contains IC: 20519-RYZ014A"`.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:

`"Contient des IC: 20519-RYZ014A".`

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Physical Characteristics

ECCN and Part Number

The orderable part number of the RYZ014A module is RYZ014A000FZ00#HD0.

The ECCN of the RYZ014A module is 5A992.c. The HTS number is 8542.39.00.01.

The following comment from licensing officer is reported on the license information:

- This encryption item is described in paragraph B to note 3 (mass market note) of category 5 part 2. It is authorized for export and reexport under section 740.17(B)(3) of the export administration regulations (EAR).

Electrical Operating Conditions

Detailed Information

Table 5 describes the electrical operating conditions for RYZ014A.

Table 5. Electrical Operating Conditions

Parameter	Direction	Minimum	Typical	Maximum
VBAT1	In	3.1 V		5.5 V (operational) 4.5 V (performance)
SIM_VCC (1.8 V or 3.0 V)	Out	1.62 V	1.8 V	1.98 V
		2.7 V	3.0 V	3.3 V
1V8 See notes below.	Out	1.71 V	1.8 V	1.89 V
3V0 See note 2 below.	Out	2.85 V	3.0 V	3.15 V
VCC1_PA	In	2.85 V	3.0 V	3.3 V
VCC2_PA	In	2.85 V	3.0 V	3.3 V

Note: 1. The maximum current consumption allowed from the 1V8 reference pin is 100 mA.
2. Each output reference voltage (1V8, 3V0) can be either running or powered off depending on the internal software configuration. They should not be used to power external IC or parts that require permanent supply.

RYZ014A Power Tree

Figure 2 provides a representation of the power tree of the RYZ014A. All current values are maximum RMS current.

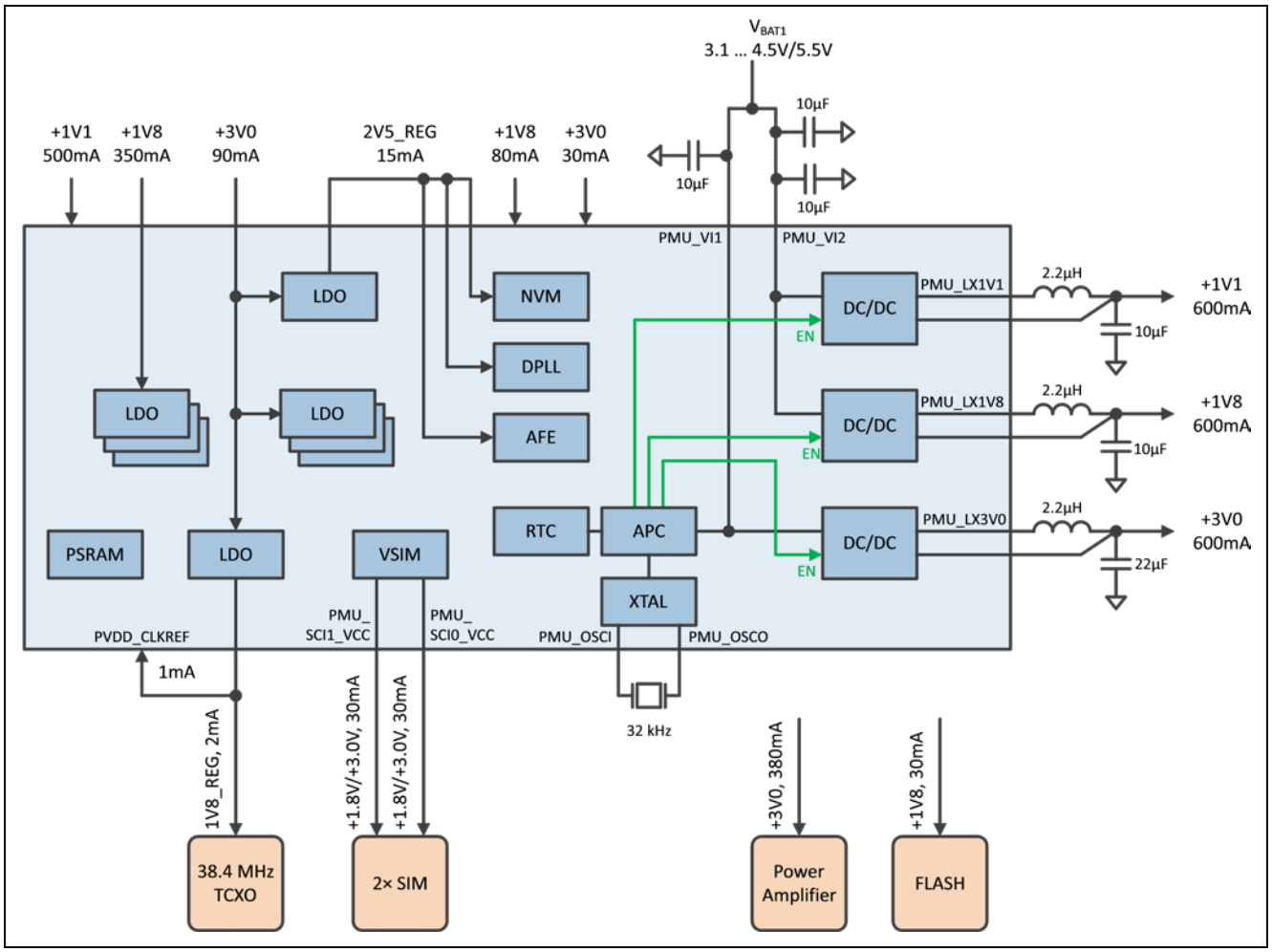

Figure 2. RYZ014A Power Tree

Power Supplies Environment

Figure 3 illustrates the connections between the RF front-end power supplies of the RYZ014A.

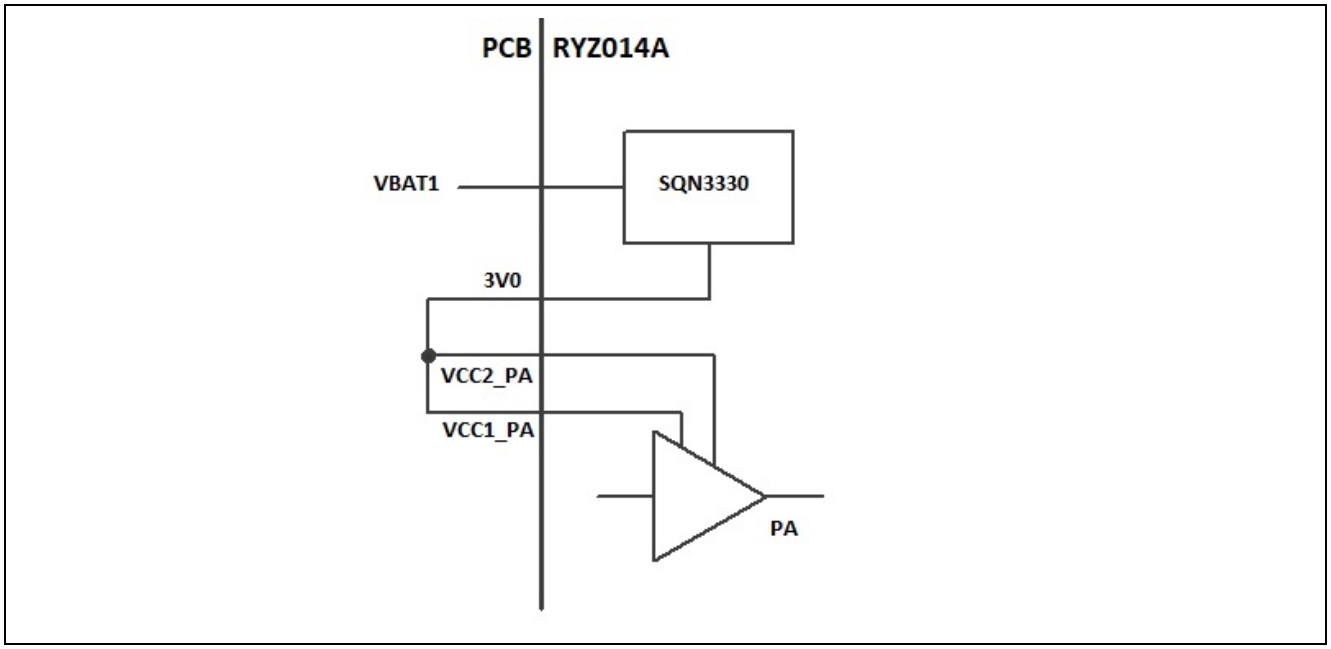

Figure 3. RYZ014A LTE RF Front-End Power Supplies Diagram

Environmental Operating Conditions

Temperature

- RF compliant: -30°C to +85°C (measured on board thermistor)
- Operational, with additional software to limit TxPower: -40°C to +95°C (measured on board thermistor)
- Storage: -40°C to +95°C

Humidity

- Operating: 10% to 85% (non-condensing)
- Storage: 5% to 85% (non-condensing)

Power Supply Dimensioning

Important: - Information provided here is ***measured peak current consumption*** for the RYZ014A Module in various LTE Tx/Rx configurations, with and without the DC/DC losses. It represents the maximum RMS current.

The power consumption depends on LTE band of operation. The figures in Table 6 are provided for LTE Band 13 only. Please contact your Renesas representative for other LTE Bands figures.

Table 6. Measured Peak Current and Peak Power Consumption (LTE Band 13)

Parameter	Measured Peak Power Consumption	Measured Battery Peak Current (for VBAT1=4.2 V)
RRC Connected, 0dBm Tx, with UL and DL traffic	0.9 W	210 mA
RRC Connected, 10dBm Tx, with UL and DL traffic	1.1 W	250 mA
RRC Connected, 23dBm Tx, with UL and DL traffic	2.0 W	485 mA

I/O Characteristics

The voltage and current characteristics of the various IO pads of the RYZ014A versus IO bank supply voltage are illustrated in the tables below.

Caution: Note that the V_{oh} values in the tables below do not apply to GPIOs configured in open drain mode. GPIOs can be individually configured in open drain mode. When in open drain mode they either drive the line to V_{ol}, or leave it floating, to be pulled up by an external pullup resistance. The PCB designer must ensure that the voltage on these pads never exceeds V_{ih} of the IO group to which they belong.

Refer to Table 3 to know the type of IO pad used on every termination.

- The Minimum values for I_{ol} and I_{oh} should not be exceeded to guarantee that the logical level are not spoiled for each pad type.
- The Nominal values for I_{ol} and I_{oh} represent the nominal values for the pad type. They are provided for information only.
- The Maximum values for I_{ol} and I_{oh} represent the maximal values for the pad type. They are provided for information only.
- By default, during boot time, the pad defined as GPIO as default function, with BIDIR or BIDIR_WAKE types, are configured as input, output disabled, with no internal pull-up and no internal pull-down.

Note: Please read *Module Integration Guide* for details on persistent AT Commands availability to change these default behaviors.

Table 7. DC Characteristics for Digital IOs, Voltage 1.8 V - BIDIR and IN Types

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
VIL Input Low Voltage		0		0.54	V
VIH Input High Voltage		1.26		3.6	V
VOL Output Low Voltage		0		0.45	V
VOH Output High Voltage		1.35		1.8	V
V_T Threshold Point		0.79	0.87	0.94	V
VT+ Schmitt Trigger Low to High Threshold Point		1	1.12	1.22	V
VT- Schmitt Trigger High to Low Threshold Point		0.61	0.71	0.8	V
VT PU Threshold Point with Pull-up Resistor Enabled		0.79	0.86	0.93	V
VT PD Threshold Point with Pull-down Resistor Enabled		0.8	0.87	0.95	V
VT+ PU Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled		1	1.12	1.21	V
VT- PU Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled		0.61	0.7	0.8	V
VT+ PD Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled		1.01	1.13	1.23	V
VT- PD Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled		0.62	0.72	0.81	V
II Input Leakage Current @ VI=1.8V or 0V				±10	µA

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
IOZ Tri-state Output Leakage Current @ VO=1.8V or 0V				±10	µA
Input Capacitance			3		pF
RPU Pull-up Resistor		56	89	148	kOhm
RPD Pull-down Resistor		52	90	167	kOhm
IOL Low Level Output Current at V_{OL}(max)	2 mA	1.2	2.2	3.6	mA
	4 mA	2.3	4.3	7.1	mA
	8 mA	4.6	8.6	14.3	mA
IOH High Level Output Current at V_{OH}(max)	2 mA	1.0	2.4	4.6	mA
	4 mA	2.0	4.7	9.2	mA
	8 mA	4.0	9.4	18.4	mA

Table 8. DC Characteristics - IN_PMU Type

Parameter	Min.	Nom.	Max.	Unit
VIL Input Low Voltage	0		0.27	V
VIH Input High Voltage	1.56		3.6	V

Table 9. DC Characteristics - BIDIR_WAKE Type

Parameter	Min.	Nom.	Max.	Unit
VIL Input Low Voltage	0		0.27	V
VIH Input High Voltage.	1.56		3.6	V
VOL Output Low Voltage	0		0.2	V
VOH Output High Voltage	1.63		1.98	V

Auxiliary ADC

ADC specification is described in Table 10.

Table 10. ADC Specification

Performance Specification	Description	Value			Unit
		Min.	Typical	Max.	
ADC voltage range		0.1		1.8	V
ADC tolerance	After calibration. The tolerance considered is the highest value between the percentage and the absolute voltage mentioned.	Highest of -2% or -5 mV		Higher of +2% or +5 mV	% or mV
ADC resolution	Nominal resolution		10		bit
ADC input capacitance	ADC input capacitance. See the note below to prevent current leakage in low-power mode.			2	pF
ADC input resistance	ADC input resistance. See the note below to prevent current leakage in low-power mode.	1			MOhm

Important: If the ADC input is interfacing with an external device which doesn't drive 0V when the RYZ014A is in Sleeping Mode, then an external analog switch (such as FET) must be connected to ADC input pin to prevent any current leakage in PMU sleeping state.

Performance

Table 11 presents the RYZ014A module's performance in the supported LTE Bands.

Table 11. RF Sensitivity and Output Power

RYZ014A Module Version	Typ. Sensitivity level (dBm) Bandwidth 1.4 MHz, 6 RB, MCS-5, BLER <5%	Conducted Power (dBm) Bandwidth 1.4 MHz, 6 RB
RYZ014A000FZ00#HD0	≤ -104	23 +1/-1.7

Component Reliability

Note: Information related to component reliability will be provided in a future edition of this document.

Package Description

Module Weight

The module weight is 2.08 g.

Module Footprint

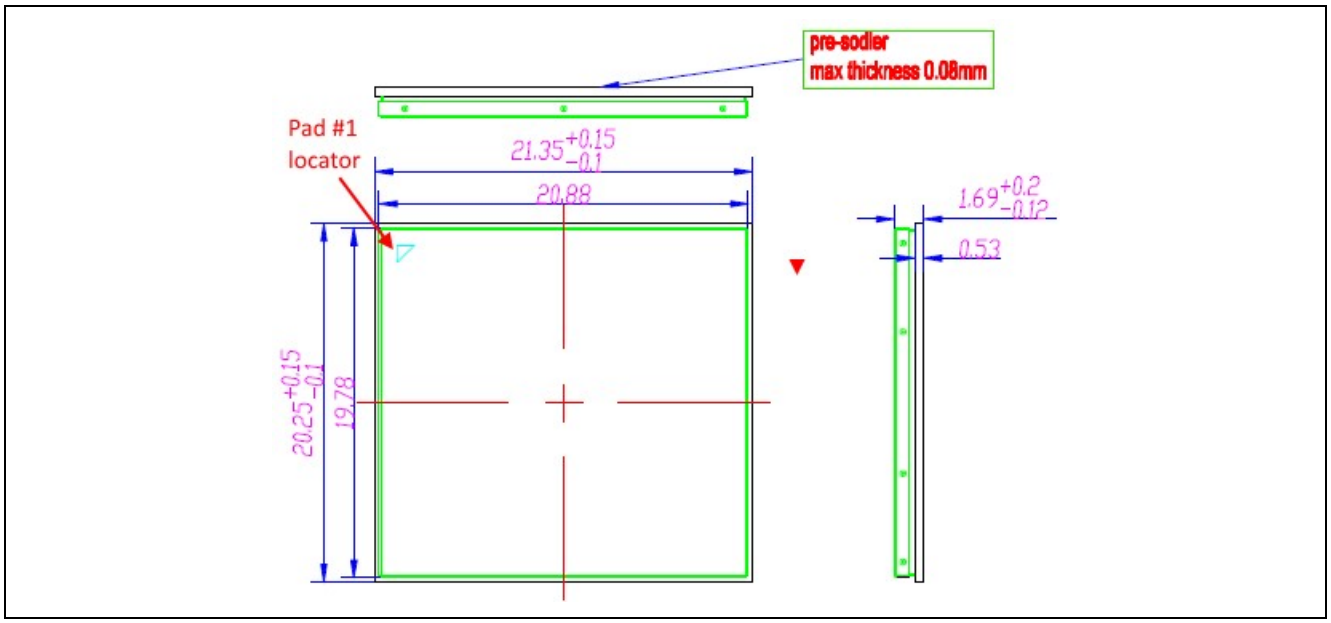

Figure 4. Module Top and Side View and Dimensions

Note: Figure 5 is a view of the pads seen on the module, and Figure 6 represents the footprint of the module on the PCB. Pad #1 is located on the top right of the module in Figure 5 and will be soldered on the top left area of the PCB footprint on Figure 6.

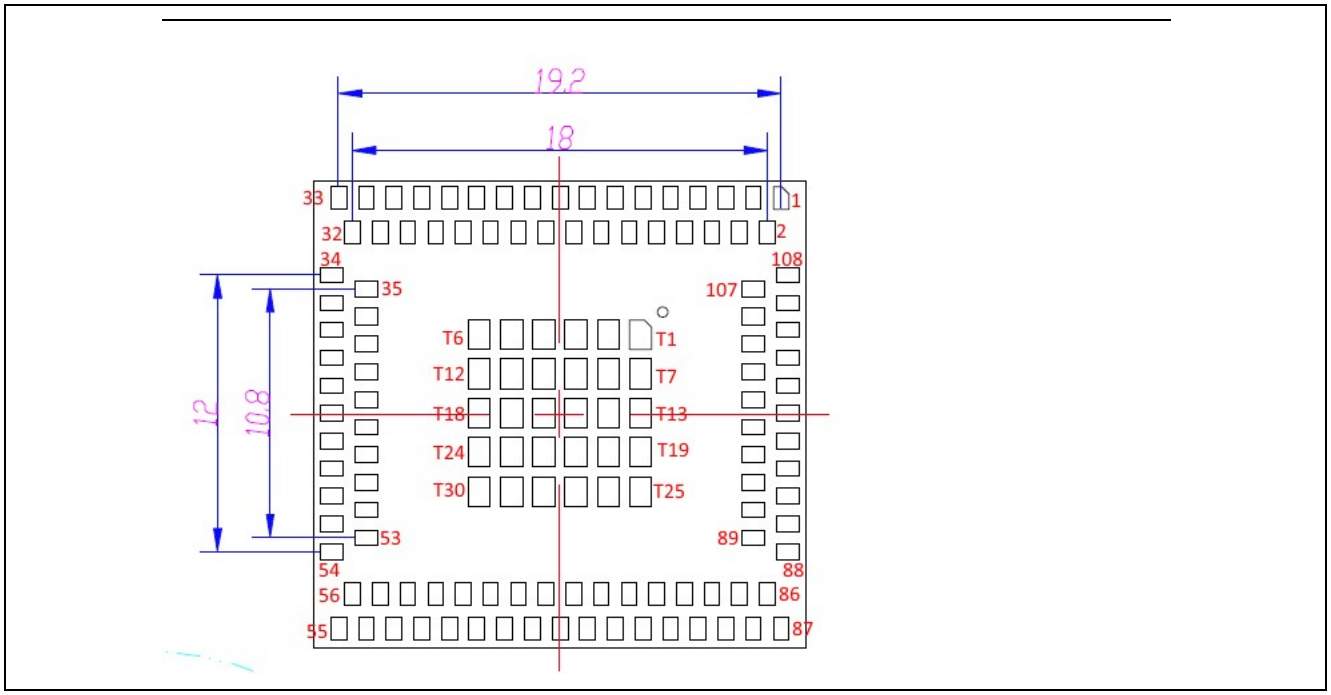

Figure 5. Module Bottom View, Dimensions and Pads Numbering (Module View)

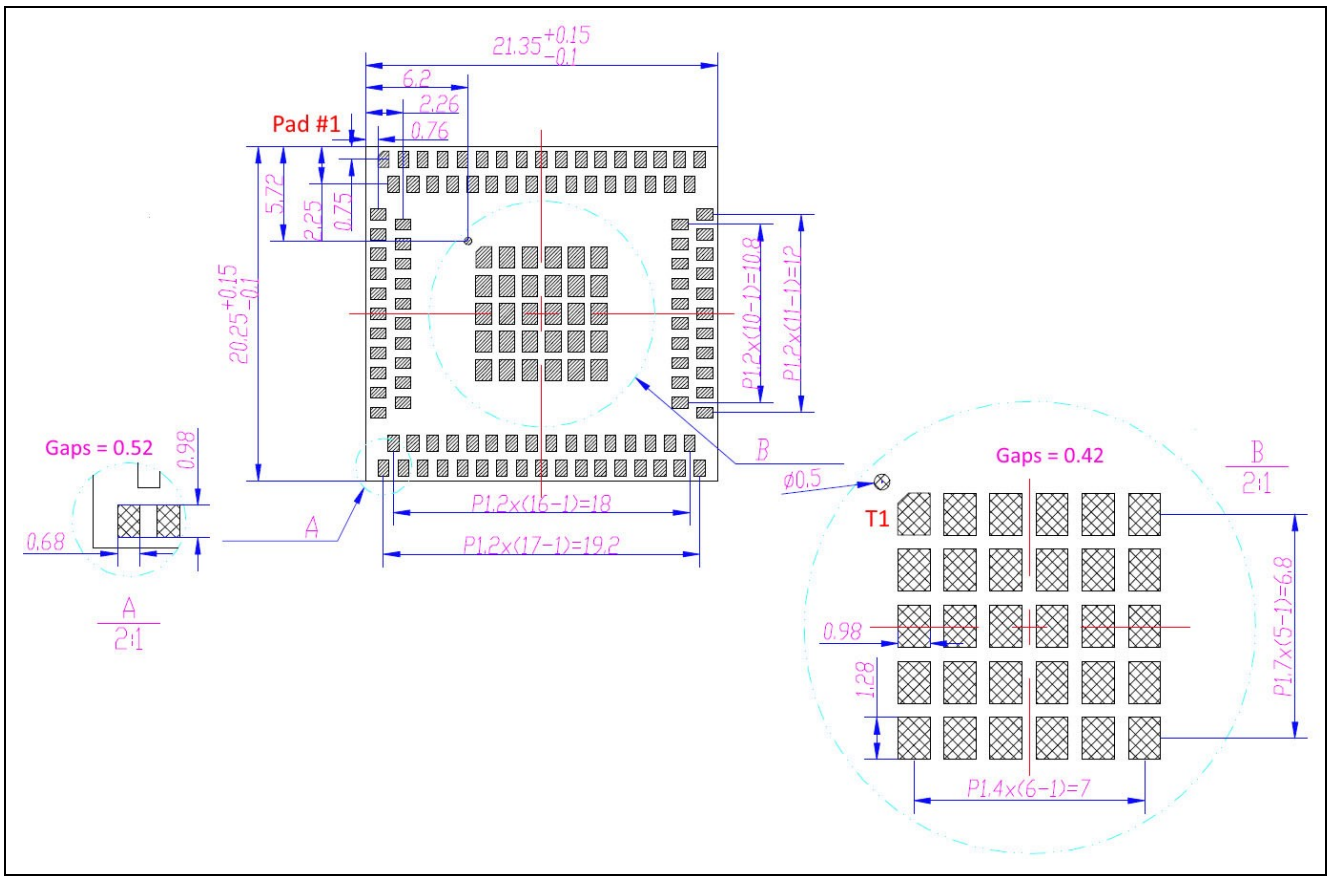

Figure 6. Module Detailed Bottom View and Dimensions (PCB View)

Marking Information

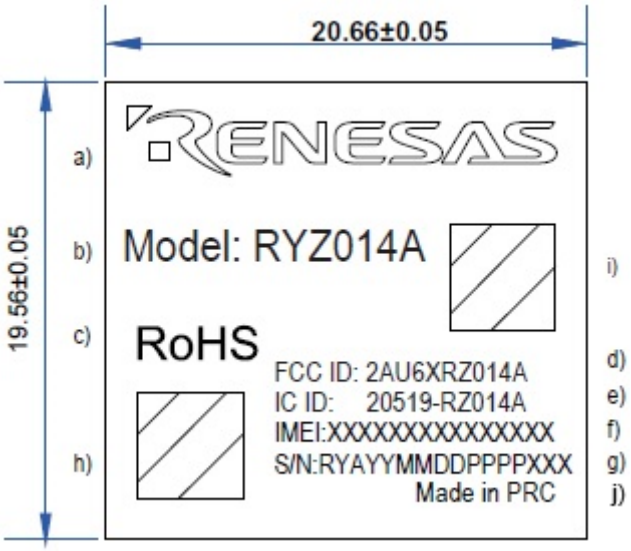

Figure 7. RYZ014A Marking Description

Table 12. Marking Details

Symbol	Description
a	Renesas Logo
b	RYZ014A Product Name
c	RoHS logo
d	FCC ID: 2AU6XRYZ014A
e	IC: 20519-RYZ014A
f	IMEI: XXXXXXXXXXXXXXX (15 digits)
g	S/N: RYAYYMMDDPPPPXXX (16 digits) RYA: is immovable (3 digits) YYMMDD: Manufacturing Date (YY: Year, MM: Month, DD: Date) PPPP: Panel Counter (4 digits 0001-9999); XXX: Piece counter (001-020)
h	IMEI Barcode
i	S/N Barcode
j	Made in PRC

Packing Information

The module is delivered in Tape-and-Reel as described below. All dimensions are in mm.

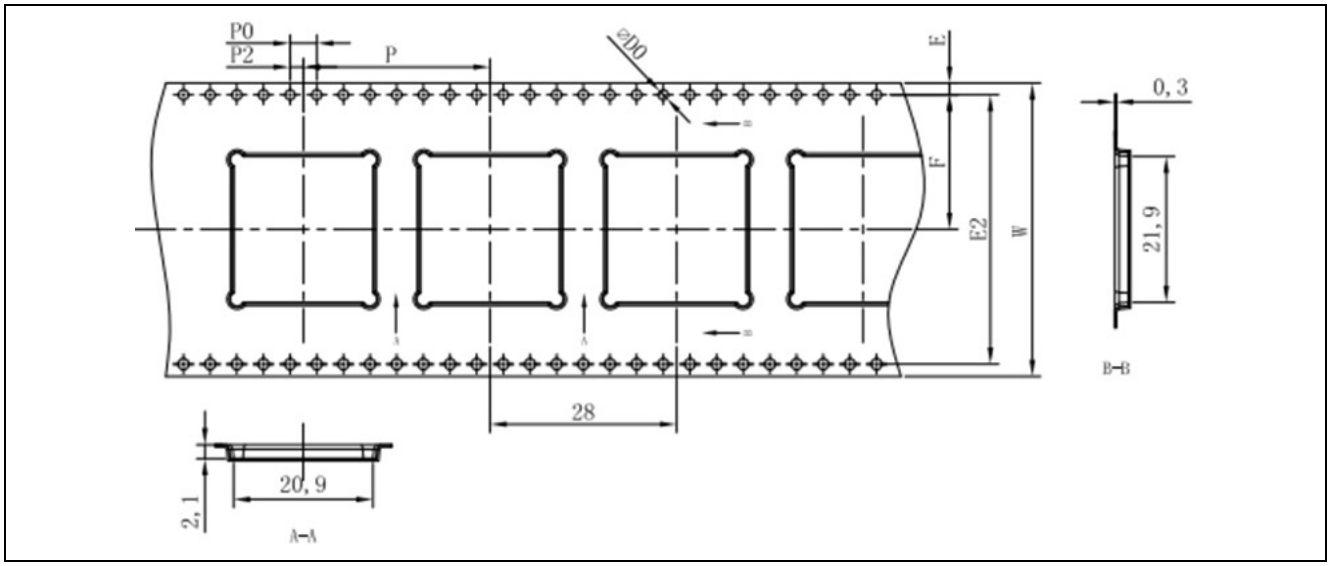

Figure 8. Packing Details

Notes: 1. 10 sprocket hole pitch cumulative tolerance +/-0.20
2. Carrier camber is within 1 mm in 250 mm
3. Material: PS, Black color
4. All dimensions meet ETA-481-C requirements
5. Thickness: 0.30 +/- 0.05 mm
6. Packing length per 15” reel: 28.56 meter
7. Component load per 15” reel : 100 pcs
8. Quantity: 1020 pcs. Empty before: 10 pcs. Empty after: 10 pcs.

Table 13. Packing Size Details

Item	Dimension and Tolerance
W	44 (-0.30 / +0.30)
A0	20.90 (-0.30 / +0.30
B0	21.90 (-0.10 / +0.10)
K0	2.10 (-0.30 / +0.30)
P	28 (-0.30 / +0.30)
E2	40.4 (-0.10 / +0.10)
F	20.2 (-0.15 / +0.15)
E	1.75 (-0.10 / +0.10)
D0	1.50 (-0.00 / +0.10)
P0	4.00 (-0.10 / +0.10)
P2	2.00 (-0.15 / +0.15)
T	0.30 (-0.05 / +0.05)

Storage Conditions

Note: Additional storage conditions impacting the mounting process are provided in the Mounting Considerations section on page 24.

The module is MSL3 compliant.

1. Calculated shelf life in sealed bag : 12 months at < 40°C and < 90% RH
2. Peak package body temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be:
   a) mounted within 168 hours of factory conditions ≤ 30°C/60%RH, or
   b) Stored as per J-STD-033
4. Devices require bake, before mounting, if
   a) Humidity Indicator Card reads >10% for level 2a-5a devices or >60% for level 2 devices when read at 23±5°C
   b) 3a or 3b above are not met
5. If baking is required, refer to IPC/FEDEC J-STD-033 for bake procedure.

Note: Level and body temperature are defined by IPC/JEDEC J-STD-020.

Mounting Considerations

The RYZ014A can support up to 3 reflows with 250°C maximum.

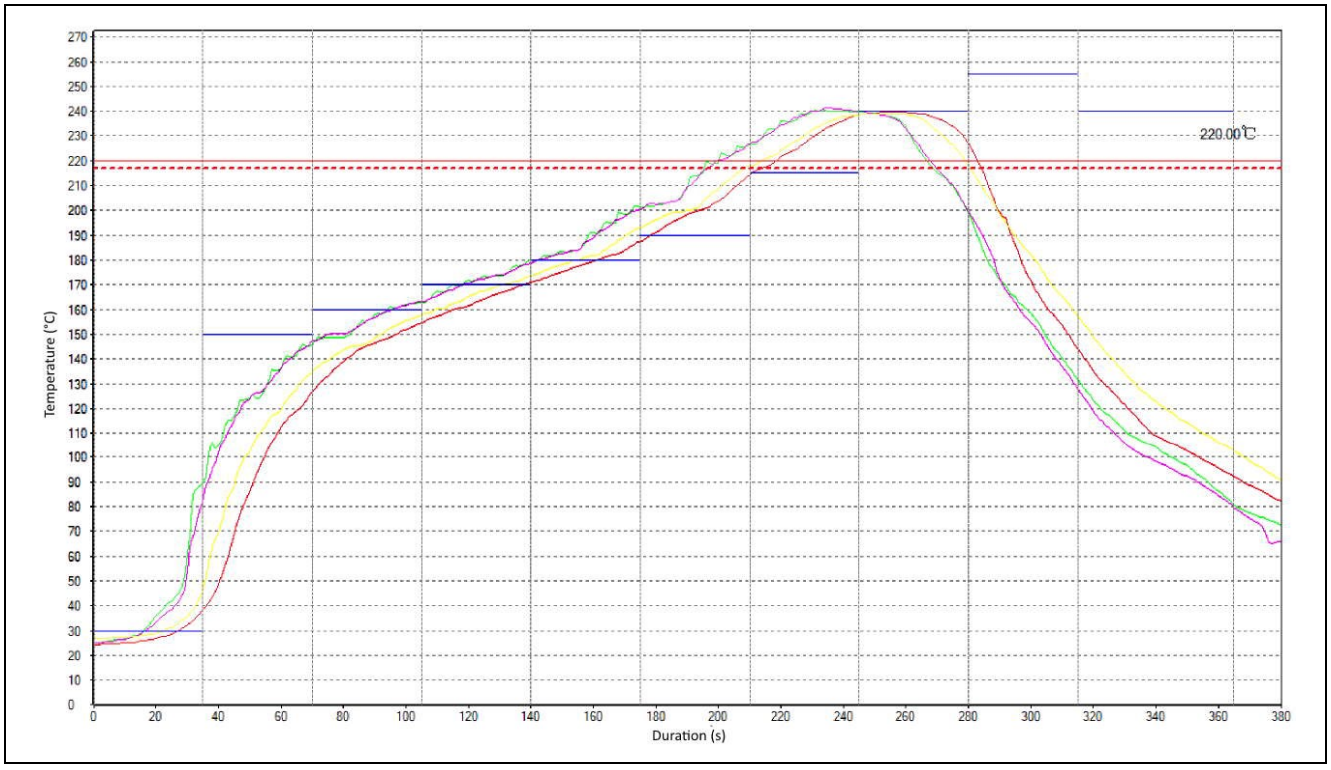

Figure 9. Reflow Profile

Table 14. Reflow Parameters

Parameter	Setting
Peak package body temperature	230°C to 255 °C
Liquidous Time	60 to 120 seconds
Preheat/Soak	60 to 120 seconds
Ramp-up rate	< 5°C/s
Ramp-down rate	-4.99 °C/s

Signals and Pins

RYZ014A Pinout

The signals and all the related details are listed in the MS-Excel companion file delivered together with the present document in a PDF portfolio.

The pads listed in Table 15 are connected to ground.

Table 15. Ground and Thermal Pads

Pad #	Pad Name	Comment
1 20 22 24 26 28 30 31 32 33 34 42 43 45 46 53 55 62 63 64 65 66 68 69 70 71 72 73 74 86 87	GND	All GND pads shall be connected to the same copper.
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23 T24 T25 T26 T27 T28 T29 T30	GND	T1 to T30 pads are used as both GND and thermal drops.

Signals Description

Table 16. Notes on Signals

Signal Name	Direction	Description
32KHZ_CLK_OUT	OUT	32 KHz clock line This output signal is available whatever module states except in power off and deep sleep modes.
ADC	IN	Analog Digital Converter
FFF_FFH	IN	Boot mode selection. Pull-up is required for proper behavior.
GPIO	IN or OUT	General Purpose I/O.
PS_STATUS	OUT	Power Saving status of the module. Pull-down is required for proper behavior. A high level indicates that module is in active mode (UART available). A low level indicates that module is in low power modes (sleep mode or deep sleep mode) to minimize power consumption.
STATUS_LED	OUT	Status LED This output signal reflects the LTE modem status.
WAKE0 WAKE1	IN	Wake signals Wake trigger is based on signal level (polarity is configurable). Minimum required duration of a pulse for detection is 100 µs.
RING0	OUT	UART0 ring line RING0 is active low by default (and configurable) and module drives this signal low to notify to the host an unsolicited result code (URC) cannot be delivered over UART<*id*> because UART is not available (RTS line high level) or busy (AT command under execution or UART in data mode).

UART Interfaces

Figure 10 represents the typical implementation for the hardware flow control for UART0, UART1 and UART2. TXD and RXD signals are mandatory. RTS and CTS are strongly recommended. The other signals are optional.

RYZ014A is designed for use as DCE (Data Communication Equipment).

Based on the conventions for DCE-DTE connections, the DCE device will communicate with the customer application (DTE) using the following signals:

- Port TXD on Application sends data to the module's TXD signal line.
- Port RXD on Application receives data from the module's RXD signal line.

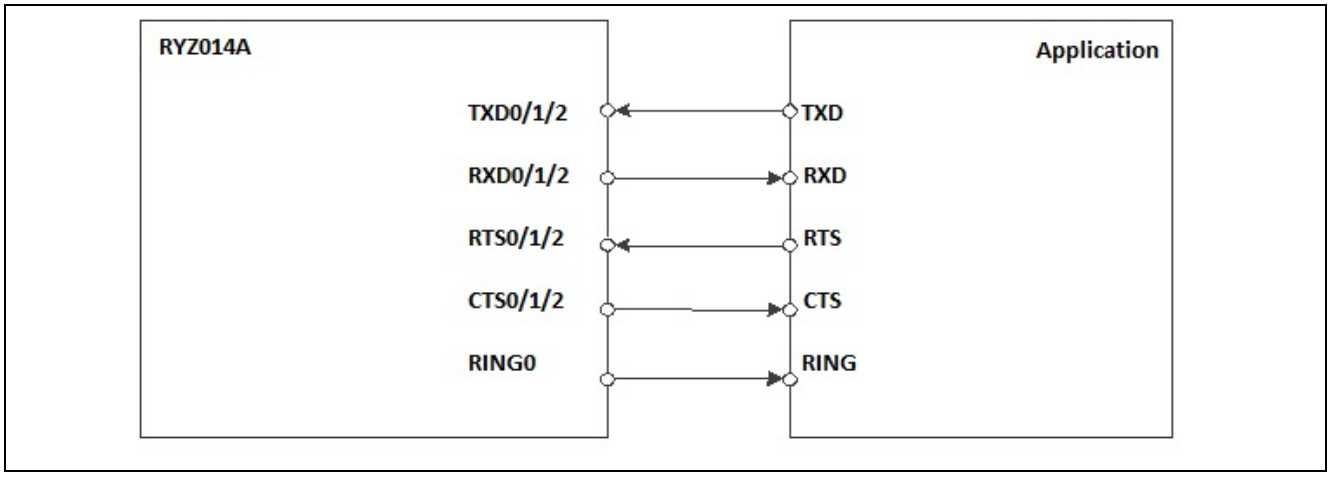

Figure 10. UART0, UART1 and UART2 Signals Convention and Flow Control

The default configuration is:

- UART0
  4 wires (hardware flow control RTS0/CTS0), baud rate 921600 baud, 8 bit data, no parity, 1 stop bit, low power wake-up capability enabled with RTS0.
  UART0 is the main interface for the LTE modem, configured for AT commands.

Important: RYZ014A UART0 is configured with hardware flow control (RTS0, CTS0). During the boot cycle, it is mandatory that the Application Host connected to UART0 implements hardware flow control on its UART, because the RYZ014A will send SYSSTART URC. Not complying with this requirement can prevent the module to boot.

- UART1
  2 wires (no hardware flow control), baud rate 115200 baud, 8 bit data, no parity, 1 stop bit, low power wake-up capability is disabled on UART1. UART1 is console interface for debug.

Note: UART1 hardware is capable to support 4 wires, higher speed up to 921600 baud and low power wake-up capability with RTS1; this capability is enabled with a persistent AT command.

- UART2
  4 wires (hardware flow control RTS2/CTS2), baud rate 921600 baud, 8 bit data, no parity, 1 stop bit, no wake-up capability on UART2 RTS2.
  UART2 is configured as a debug and software upgrade port by default.
  Please read the following notes on UART-related signals.

Table 17. UART Signals Description

Signal Name	UART0	UART1	UART2	Direction	Description
CTS0 CTS1 CTS2	Yes	Yes	Yes	OUT	UART0/1/2 Clear To Send. Pull-up is required for proper behavior.
RTS0 RTS1 RTS2	Yes	Yes	Yes	IN	UART0/1/2 Request To Send RTS0 signal is active low and indicates host is ready to receive data over UART<*id*>. Pad may be configured to wake-up the module at RTS<*id*> falling edge. This wake-up capability is only available for RTS0 and RTS1.
RING0	N/A	N/A	N/A	OUT	See Table 16 on page 25.

Power-up Sequence

The following timing requirement applies to the signals VBAT1, POWER_EN and RESET_N. It must be respected for proper RYZ014A's behavior.

Note: The POWER_EN signal has no function for RYZ014A modules.

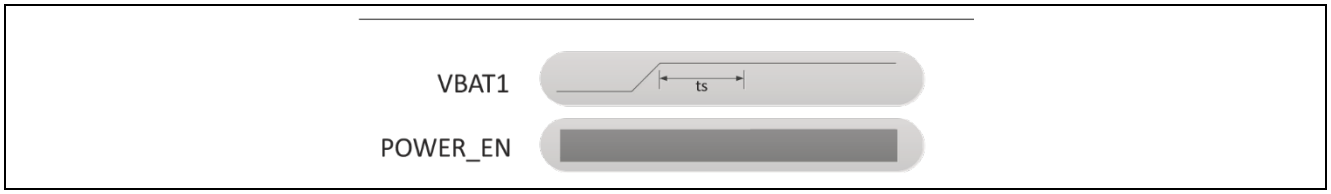

Figure 11. VBAT1 and POWER_EN Signals Timing Requirement for Cold Start

Note: RESETN signal has no impact on the cold start sequence.

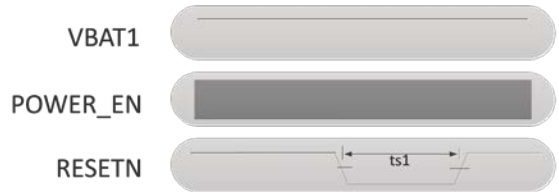

Figure 12. VBAT1, POWER_EN and RESET_N Signals Timing Requirement for Warm Start and Reset Cycle

The timing minimum values are listed in Table 18.

Table 18. VBAT1 and RESET_N Signal Timing Values

Symbol	Description	Minimum Duration
ts1	RESET_N hold time	1 µs
ts	VBAT1 setup time	1 ms

LTE Low Power Mode

General Information

Important: The RYZ014A module is provided with an internal RTC whose supply is VBAT1. As a consequence, VBAT1 should not be removed, in order to keep RTC active.

The RYZ014A will automatically enter in low-power mode. RYZ014A can be woken from low power mode by external sources through:

- SIM_DETECT input signal to cope with SIM card insertion or removal into a SIM card connector with built-in hardware detection.
- The RTS0/1 input signal whenever data traffic is initiated by the host connected to the module UART0/1 with hardware flow control.
- Up to four dedicated input signals WAKE0, WAKE1, WAKE2 and WAKE3. They are not configured by default as wake-up source but a persistent AT command can enable and configure them. As example, these signals can be used to detect an alarm from an external IC such as a sensor. Software can enable and disable the wake-up functionality on these signals.

Important: WAKE inputs are detected on level (configurable by software to 0 or 1) that must last at least 5 periods of the 32 kHz clock, that is 156.25 µs. Their polarity is configurable by software.

Detailed Behavior of IO Pads of BIDIR Type

- Behavior in Sleep Mode or Active Mode

Typical
50 MOhm

Figure 13 shows a simplified diagram of the Digital bi-directional IOs in Sleep Mode or active mode.

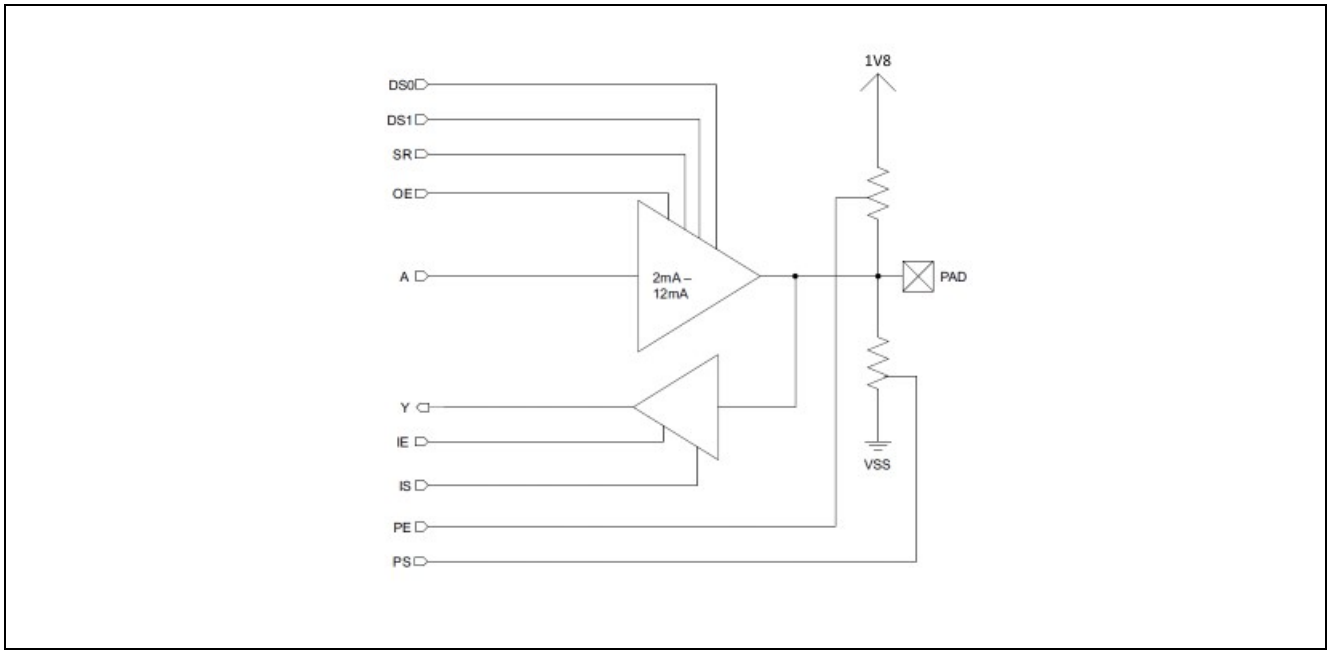

Figure 13. Digital Bi-Directional IOs in Sleep Mode or Active Mode

- Behavior in Deep Sleep Mode
  In Deep Sleep Mode the Digital bi-directional IOs are completely powered Off.
  In Deep Sleep Mode the Digital bi-directional IOs can be seen as high-impedance from the outside.

Detailed Behavior of IO Pads of BIDIR_WAKE Type

- Behavior in Sleep Mode or Active Mode
  PMU bi-directional wake IOs are used as general purposed IO buffers in Sleep Mode or active mode.
  Figure 14 shows a simplified diagram of the PMU bi-directional wake IOs in Sleep Mode or active mode.

Note: The PMU bi-directional wake IOs output buffer requires the 3.0V power supply to be ON.

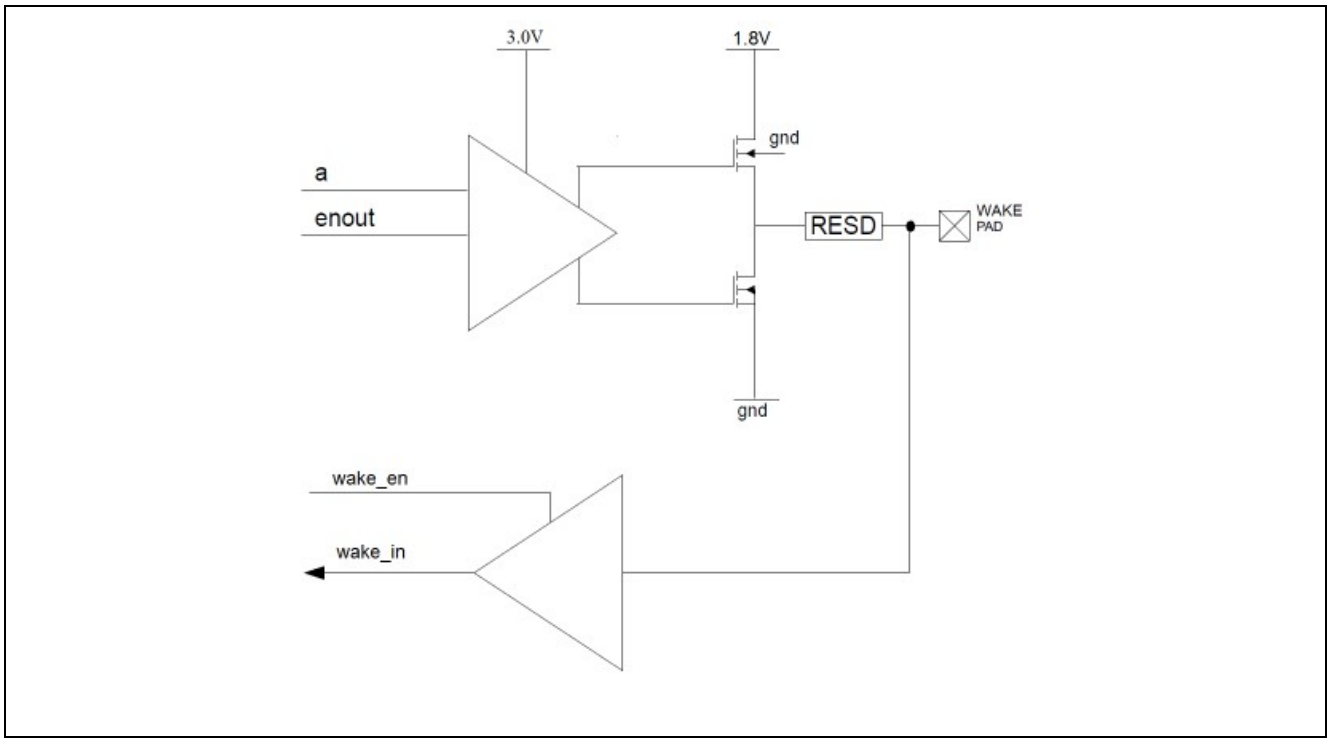

Figure 14. PMU Wake IOs in Sleep Mode or Active Mode

LTE LOW POWER MODE

- Behavior in Deep Sleep Mode.

Note: The PMU bi-directional wake IOs output buffer is disabled in Deep Sleep Mode.

Figure 15 shows a simplified diagram of the PMU bi-directional wake IOs in Deep Sleep Mode.

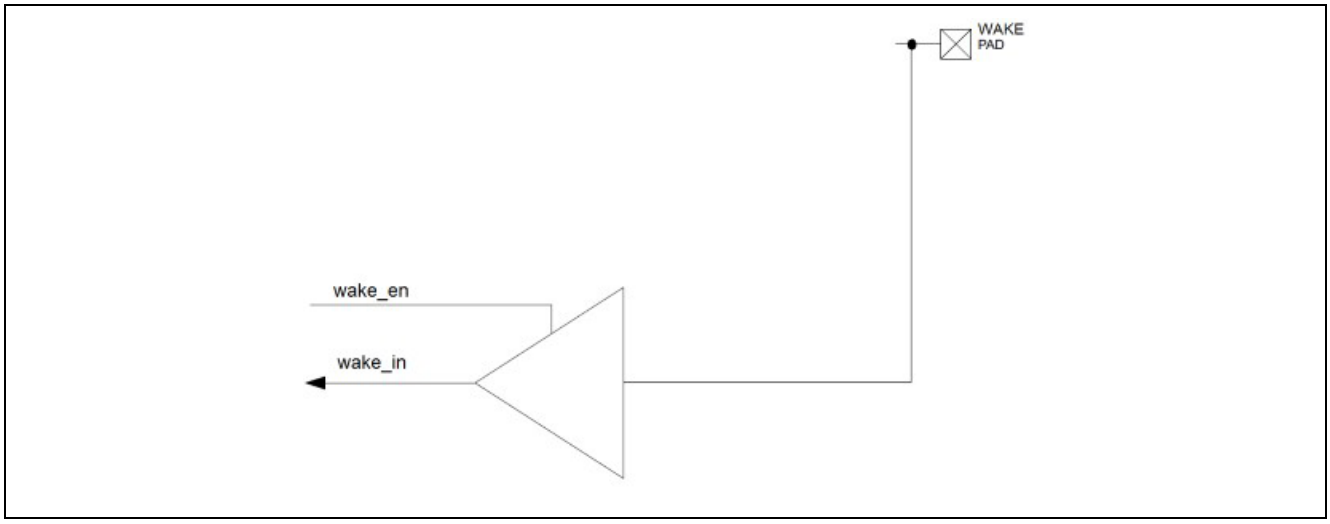

Figure 15. PMU Wake IOs in Deep Sleep Mode

In Deep Sleep Mode, all PMU bi-directional wake IOs are high impedance with ultra-low leakage current. This corresponds to a minimum impedance of 180 MOhm at the maximum input supply voltage of 3.6 V.

If an event is presented on the wake IO pad and this wake IO has been configured to be sensitive on that event, this will take the system back to Active mode.

Table 19 shows the values of the measured leakage current (measurements taken on silicon) for the PMU bi-directional wake IOs.

Table 19. Measured leakage current for the PMU bi-directional wake IOs.

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 20 shows values of the external pull-up/pull-down resistor to be used on the PMU bi-directional wake IOs pads.

Table 20. External pull-up/pull-down resistor to be used on the PMU bi-directional wake IOs pads

Minimum	Typical	Maximum
1 kOhm	10 kOhm	100 kOhm

Table 21 shows details about the PMU bi-directional wake IOs pulses detection mechanism timings.

Table 21. Details about the PMU bi-directional wake IOs pulses detection mechanism timings

Maximum pulse width that is guaranteed to be ignored	Minimum pulse width that is guaranteed to be seen
11.1 ns	100 µs

Acronyms

Acronym	Definition
AFE	Analog Front-End
APC	Automatic Control Power
CE	Coverage Extension
COO	Country of origin
CPU	Central Processing Unit
DC/DC	Direct current converter

Acronym	Definition
DDR	Double Data Rate (SDRAM)
DL	Downlink
DPLL	Digital Phase-Locked Loop
ECCN	Export Control Classification Number
EPS	Evolved Packet System
ESD	Electro-static discharge
ETSI	European Telecommunications Standard Institute
FCC	Federal Communications Commission (USA)
GND	Ground
GPIO	General Purpose Input Output
HBM	Human Body Model (ESD)
I/O	Input/Output
I2C	Inter-integrated circuit (bus)
IETF	Internet Engineering Task Force. See https://www.ietf.org/
IMEI	International Mobile Equipment Identity
IMS	Instant Messaging Service
IP	Internet Protocol
JTAG	Joint Test Action Group. See IEEE 1149.7 specification
LDO	Low Drop-Out regulator
LGA	Large Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution, or 4G. Standard is developed by the 3GPP www.3gpp.org.
MM	Machine Model (ESD)
NAS	Network Access Server
NVM	Non Volatile Memory
OEM	Original Equipment Manufacturer
OMADM	Open Mobile Alliance Device Management
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit
pSRAM	Pseudo-Static Random Access Memory
QTY	Quantity
RAM	Random Access Memory
RAN	Radio Access Network
RB	Resource Block
RF	Radio Frequency
RFIC	RF Integrated Circuit
RoHS	Restriction of Hazardous Substances
RTC	Real-Time Clock
Rx	Reception
S/N	or SN: Serial Number
SAW	Surface Acoustic Wave (filters)
SDM	Socketed Device Model (ESD)
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
TCXO	Temperature-controlled crystal oscillator
Tx	Transmission
UART	Universal asynchronous receiver transmitter.

Acronym	Definition
UE	User Equipment
UICC	Universal integrated circuit card (SIM)
UL	Uplink
XTAL	Crystal

References

1. Core technology specifications:
   - 3GPP E-UTRA 21 series Release 13 (EPS)
   - 3GPP E-UTRA 22 series Release 13 (IMEI)
   - 3GPP E-UTRA 23 series Release 13 (NAS, SMS)
   - 3GPP E-UTRA 24 series Release 13 (NAS)
   - 3GPP E-UTRA 31 series Release 13 (UICC)
   - 3GPP E-UTRA 33 series Release 13 (security)
   - 3GPP E-UTRA 36 series Release 13 (RAN)
   - 3GPP2 C.S0015-A v1.0 (SMS)
   - IETF, RFC 3261, 4861, 4862, 6434For more information, see
   - ftp://ftp.3gpp.org/Specs/archive/
   - http://www.3gpp2.org/public_html/specs/CS0015-0.pdf
   - https://tools.ietf.org/html/

2. Test specifications:
   3GPP E-UTRA 36 series Release 13 (RAN) ftp://ftp.3gpp.org/Specs/archive/

3. Vocabulary reference:
   - 3GPP TR 21.905: "Vocabulary for 3GPP Specifications"
     For more information, see http://www.3gpp.org/ftp/specs/archive/21_series/21.905/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	Initial release.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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