

# nRF52820

## Product Specification

v1.0

# Feature list

## Features:

- **Bluetooth<sup>®</sup> 5.1**, IEEE 802.15.4-2006, 2.4 GHz transceiver
  - -95 dBm sensitivity in 1 Mbps **Bluetooth<sup>®</sup> Low Energy** mode
  - -103 dBm sensitivity in 125 kbps **Bluetooth<sup>®</sup> Low Energy** mode (long range)
  - -20 to +8 dBm TX power, configurable in 4 dB steps
  - On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP Series
  - Supported data rates:
    - **Bluetooth<sup>®</sup> 5.1** – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
    - IEEE 802.15.4-2006 – 250 kbps
    - Proprietary 2.4 GHz – 2 Mbps, 1 Mbps
  - Angle-of-arrival (AoA) and angle-of-departure (AoD) direction finding using **Bluetooth<sup>®</sup>**
  - Single-ended antenna output (on-chip balun)
  - 128-bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
  - 4.9 mA peak current in TX (0 dBm)
  - 4.7 mA peak current in RX
  - RSSI (1 dB resolution)
- **Arm<sup>®</sup> Cortex<sup>®</sup>-M4** 32-bit processor, 64 MHz
  - 144 EEMBC CoreMark<sup>®</sup> score running from flash memory
  - 33  $\mu$ A/MHz running CoreMark from flash memory
  - 33  $\mu$ A/MHz running CoreMark from RAM
  - Serial wire debug (SWD)
- Flexible power management
  - 1.7 V to 5.5 V supply voltage range
  - On-chip DC/DC and LDO regulators with automated low current modes
  - Automated peripheral power management
  - Fast wake-up using 64 MHz internal oscillator
  - 0.3  $\mu$ A at 3 V in System OFF mode, no RAM retention
  - 1.2  $\mu$ A at 3 V in System ON mode, no RAM retention, wake on RTC
- 256 kB flash and 32 kB RAM
- Advanced on-chip interfaces
  - USB 2.0 full speed (12 Mbps) controller
  - Programmable peripheral interconnect (PPI)
  - 18 general purpose I/O pins
  - EasyDMA automated data transfer between memory and peripherals
- Nordic SoftDevice ready with support for concurrent multiprotocol
- 64 level comparator
- Temperature sensor
- 4x 32-bit timer with Counter mode
- Up to 2x SPI master/slave with EasyDMA
- Up to 2x I<sup>2</sup>C compatible two-wire master/slave
- UART (CTS/RTS) with EasyDMA
- Quadrature decoder (QDEC)
- 2x real-time counter (RTC)
- Single crystal operation
- Operating temperature from -40 to 105 °C
- Package variants
  - QFN40 package, 5 x 5 mm

## Applications:

- Advanced computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Internet of things (IoT)
  - Smart home sensors and controllers
  - Industrial IoT sensors and controllers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers

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# 1 Revision history

Date	Version	Description
June 2020	1.0	First release

# 2 About this document

This document is organized into chapters that are based on the modules and peripherals available in the IC.

## 2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

## 2.2 Peripheral chapters

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM<sup>®</sup> Cortex<sup>®</sup> Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

The chapters describing peripherals may include the following information:

- A detailed functional description of the peripheral
- Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in [Recommended operating conditions](#) on page 430.

## 2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

### 2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..!'.  
 ..!

A feature marked **Deprecated** should not be used for new designs.

### 2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.

Table 2: Register field permission schemes

## 2.4 Registers

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

Table 3: Register overview

### 2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID					D	D	D	D					C	C	C					B					A	A							
<b>Reset 0x00050002</b>	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

ID	Acce	Field	Value ID	Value	Description
A	RW	FIELD_A			Example of a read-write field with several enumerated values
			Disabled	0	The example feature is disabled
			NormalMode	1	The example feature is enabled in normal mode
			ExtendedMode	2	The example feature is enabled along with extra functionality
B	RW	FIELD_B			Example of a deprecated read-write field <span style="float: right;">Deprecated</span>
			Disabled	0	The override feature is disabled
C	RW	FIELD_C			Example of a read-write field with a valid range of values
			ValidRange	[2..7]	Example of allowed values for this field
D	RW	FIELD_D			Example of a read-write field with no restriction on the values

# 3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

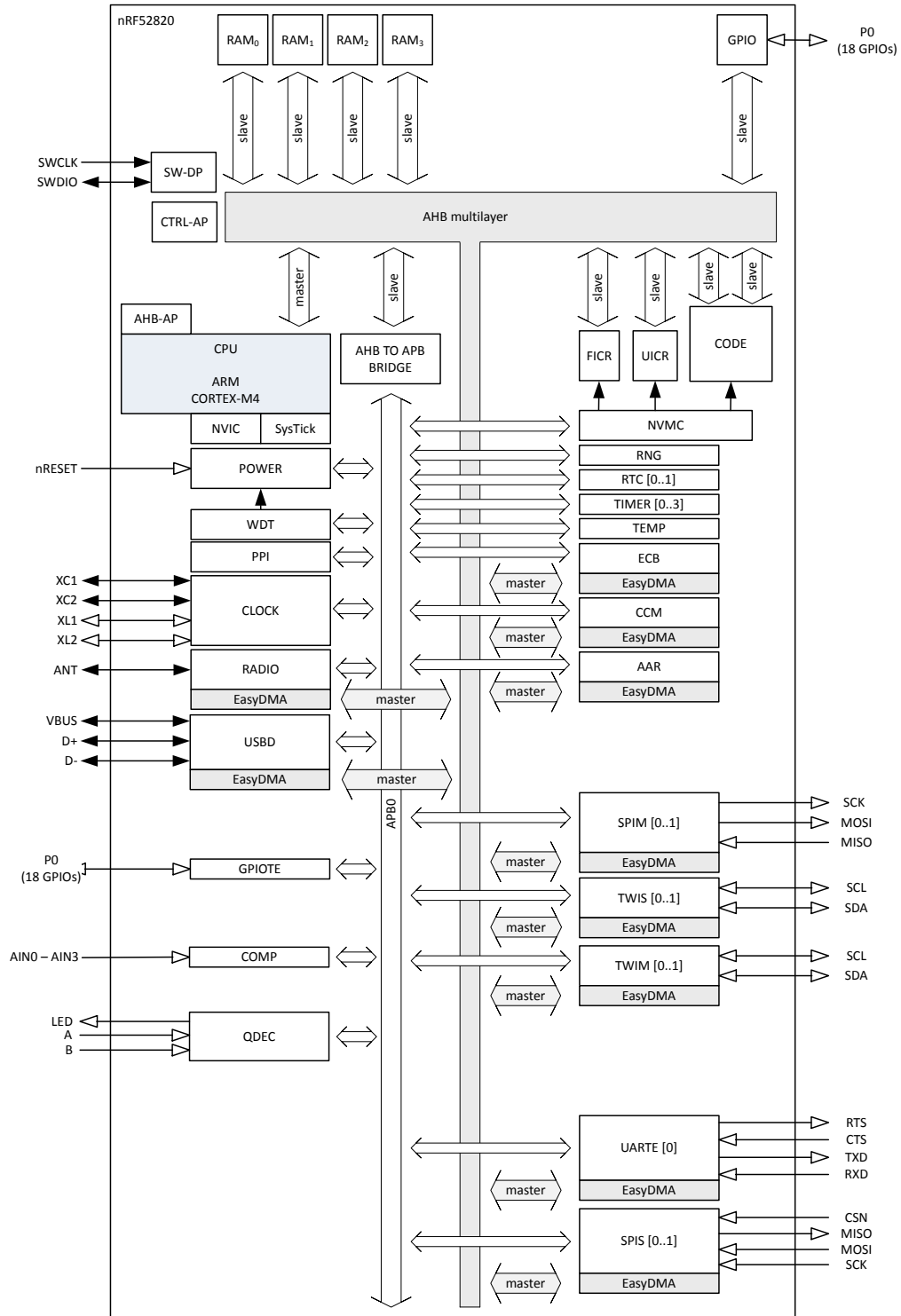


Figure 1: Block diagram

# 4 Core components

## 4.1 CPU

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processor has a 32-bit instruction set (Thumb<sup>®</sup>-2 technology) that implements a superset of 16- and 32-bit instructions to maximize code density and performance.

This processor implements the following features that enable energy-efficient arithmetic and high-performance signal processing.

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions

The ARM<sup>®</sup> Cortex<sup>®</sup> Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM<sup>®</sup> Cortex<sup>®</sup> processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from flash memory will have a wait state penalty on the nRF52 Series. The [Electrical specification](#) on page 15 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark<sup>®</sup> benchmark.

The ARM system timer (SysTick) is present on nRF52820. The SysTick's clock will only tick when the CPU is running or when the system is in debug interface mode.

### 4.1.1 CPU and support module configuration

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processor has a number of CPU options and support modules implemented on the IC.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vector interrupt controller	48 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup interrupt controller	NO
Endianness	Memory system endianness	Little endian
Bit-banding	Bit banded memory	NO
DWT	Data watchpoint and trace	NO
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating-point unit	NO
DAP	Debug access port	YES
ETM	Embedded trace macrocell	NO
ITM	Instrumentation trace macrocell	NO
TPIU	Trace port interface unit	NO
ETB	Embedded trace buffer	NO
FPB	Flash patch and breakpoint unit	YES
HTM	AMBA <sup>™</sup> AHB trace macrocell	NO



See [AHB multilayer](#) on page 39 and [EasyDMA](#) on page 37 for more information about the AHB multilayer interconnect and EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

### 4.2.1 RAM - Random access memory

The RAM interface is divided into four RAM AHB slaves.

RAM AHB slaves 0 to 3 are connected to two 4 kB RAM sections each, as shown in [Memory layout](#) on page 15.

Each RAM section has separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the [POWER — Power supply](#) on page 49).

### 4.2.2 Flash - Non-volatile memory

The CPU can read from flash memory an unlimited number of times, but is restricted in how it writes to flash and the number of writes and erases it can perform.

Writing to flash memory is managed by the non-volatile memory controller (NVMC), see [NVMC — Non-volatile memory controller](#) on page 19.

Flash memory is divided into 64 pages of 4 kB each that can be accessed by the CPU via the ICODE and DCODE buses as shown in [Memory layout](#) on page 15.

### 4.2.3 Memory map

The complete memory map for the nRF52820 is shown in the following figure. As described in [Memory](#) on page 15, Code RAM and Data RAM are the same physical RAM.



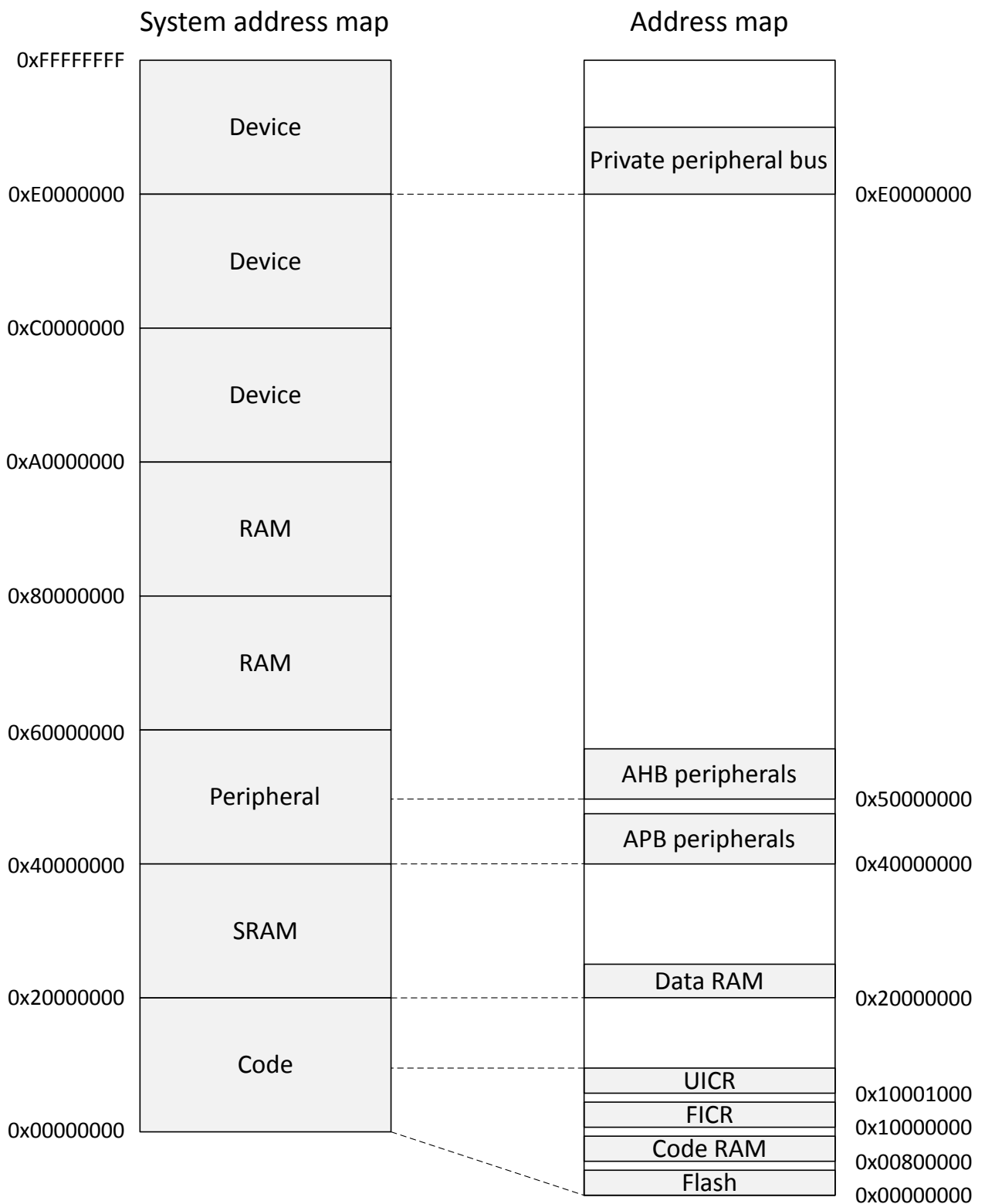


Figure 3: Memory map

## 4.2.4 Instantiation

ID	Base address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
0	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0	0x50000000	GPIO	P0	General purpose input and output, port 0.	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UART	UART0	Universal asynchronous receiver/transmitter	Deprecated
2	0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA, unit 0	
3	0x40003000	SPI	SPIO	SPI master 0	Deprecated
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
6	0x40006000	GPIOE	GPIOE	GPIO tasks and events	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES electronic code book (ECB) mode block encryption	
15	0x4000F000	AAR	AAR	Accelerated address resolver	
15	0x4000F000	CCM	CCM	AES counter with CBC-MAC (CCM) mode block encryption	
16	0x40010000	WDT	WDT	Watchdog timer	
17	0x40011000	RTC	RTC1	Real-time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	COMP	COMP	General purpose comparator	
20	0x40014000	EGU	EGU0	Event generator unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	EGU	EGU1	Event generator unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	EGU	EGU2	Event generator unit 2	
22	0x40016000	SWI	SWI2	Software interrupt 2	
23	0x40017000	EGU	EGU3	Event generator unit 3	
23	0x40017000	SWI	SWI3	Software interrupt 3	
24	0x40018000	EGU	EGU4	Event generator unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	EGU	EGU5	Event generator unit 5	
25	0x40019000	SWI	SWI5	Software interrupt 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
30	0x4001E000	ACL	ACL	Access control lists	
30	0x4001E000	NVMC	NVMC	Non-volatile memory controller	
31	0x4001F000	PPI	PPI	Programmable peripheral interconnect	

ID	Base address	Peripheral	Instance	Description
39	0x40027000	USB	USB	Universal serial bus device
N/A	0x10000000	FICR	FICR	Factory information configuration
N/A	0x10001000	UICR	UICR	User information configuration

Table 4: Instantiation table

## 4.3 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing of the internal flash memory and the UICR (user information configuration registers).

The [CONFIG](#) on page 21 is used to enable the NVMC for writing (CONFIG.WEN = Wen) and erasing (CONFIG.WEN = Een).

The CPU must be halted before initiating a NVMC operation from the debug system.

### 4.3.1 Writing to flash

When write is enabled, full 32-bit words can be written to word-aligned addresses in flash memory.

As illustrated in [Memory](#) on page 15, the flash is divided into multiple pages. The same 32-bit word in flash memory can only be written  $n_{WRITE}$  number of times before a page erase must be performed.

The NVMC is only able to write 0 to bits in flash memory that are erased (set to 1). It cannot rewrite a bit back to 1. Only full 32-bit words can be written to flash memory using the NVMC interface. To write less than 32 bits, write the data as a full 32-bit word and set all the bits that should remain unchanged in the word to 1. The restriction on the number of writes ( $n_{WRITE}$ ) still applies in this case.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

The time it takes to write a word to flash is specified by  $t_{WRITE}$ . The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

NVM writing time can be reduced by using READYNEXT. If this status bit is set to 1, code can perform the next data write to the flash. This write will be buffered and will be taken into account as soon as the ongoing write operation is completed.

### 4.3.2 Erasing a page in flash

When erase is enabled, the flash memory can be erased page by page using the [ERASEPAGE](#) on page 22.

After erasing a flash page, all bits in the page are set to 1. The time it takes to erase a page is specified by  $t_{ERASEPAGE}$ . The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the flash.

See [Partial erase of a page in flash](#) on page 20 for information on dividing the page erase time into shorter chunks.

### 4.3.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written  $n_{WRITE}$  number of times before an erase must be performed using [ERASEUICR](#) on page 23 or [ERASEALL](#) on page 22. The time it takes to write a word to UICR is specified by  $t_{WRITE}$ . The CPU is halted if the CPU executes code from the flash while the NVMC is writing to the UICR.

### 4.3.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the [ERASEUICR](#) on page 23.

After erasing UICR, all bits in UICR are set to 1. The time it takes to erase UICR is specified by  $t_{ERASEPAGE}$ . The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

### 4.3.5 Erase all

When erase is enabled, flash and UICR can be erased completely in one operation by using the [ERASEALL](#) on page 22. This operation will not erase the factory information configuration registers (FICR).

The time it takes to perform an [ERASEALL](#) command is specified by  $t_{ERASEALL}$ . The CPU is halted if the CPU executes code from the flash while the NVMC performs the erase operation.

### 4.3.6 Access port protection behavior

When access port protection is enabled, parts of the NVMC functionality will be blocked in order to prevent intentional or unintentional erase of UICR.

	CTRL-AP	ERASEALL	NVMC ERASEPAGE	NVMC ERASEPAGE PARTIAL	NVMC ERASEALL	NVMC ERASEUICR
<b>APPROTECT</b>						
Disabled	Allowed	Allowed	Allowed	Allowed	Allowed	Allowed
Enabled	Allowed	Allowed	Allowed	Allowed	Allowed	Blocked

Table 5: NVMC Protection

### 4.3.7 NVMC power failure protection

NVMC power failure protection is possible through use of power-fail comparator that is monitoring power supply.

If the power-fail comparator is enabled, and the power supply voltage is below  $V_{POF}$  threshold, the power-fail comparator will prevent the NVMC from performing erase or write operations in non-volatile memory (NVM).

If a power failure warning is present at the start of an NVM erase operation, the NVMC operation will be ignored.

If a power failure warning is present at the start of an NVM write operation, the CPU will hardfault.

### 4.3.8 Partial erase of a page in flash

Partial erase is a feature in the NVMC to split a page erase time into shorter chunks to prevent longer CPU stalls in time-critical applications. Partial erase is only applicable to the code area in flash memory and does not work with UICR.

When erase is enabled, the partial erase of a flash page can be started by writing to [ERASEPAGEPARTIAL](#) on page 23. The duration of a partial erase can be configured in [ERASEPAGEPARTIALCFG](#) on page 24. A flash page is erased when its erase time reaches  $t_{ERASEPAGE}$ . Use [ERASEPAGEPARTIAL](#) N number of times so that  $N * ERASEPAGEPARTIALCFG \geq t_{ERASEPAGE}$ , where  $N * ERASEPAGEPARTIALCFG$  gives the cumulative (total) erase time. Every time the cumulative erase time reaches  $t_{ERASEPAGE}$ , it counts as one erase cycle.

After the erase is complete, all bits in the page are set to 1. The CPU is halted if the CPU executes code from the flash while the NVMC performs the partial erase operation.

The bits in the page are undefined if the flash page erase is incomplete, i.e. if a partial erase has started but the total erase time is less than  $t_{ERASEPAGE}$ .



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	WEN		Program memory access mode. It is strongly recommended to only activate erase and write modes when they are actively used.																												
		Ren	0	Read only access																												
		Wen	1	Write enabled																												
		Een	2	Erase enabled																												

#### 4.3.9.4 ERASEPAGE

Address offset: 0x508

Register for erasing a page in code area

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A																														A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	W	ERASEPAGE		Register for starting erase of a page in code area																												
				The value is the address to the page to be erased. (Addresses of first word in page). The erase must be enabled using CONFIG.WEN before the page can be erased. Attempts to erase pages that are outside the code area may result in undesirable behavior, e.g. the wrong page may be erased.																												

#### 4.3.9.5 ERASEPCR1 ( Deprecated )

Address offset: 0x508

Register for erasing a page in code area, equivalent to ERASEPAGE

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A																														A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	W	ERASEPCR1		Register for erasing a page in code area, equivalent to ERASEPAGE																												

#### 4.3.9.6 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	W	ERASEPAGEPARTIAL		<p>Register for starting partial erase of a page in code area</p> <p>The value is the address to the page to be partially erased (address of the first word in page). The erase must be enabled using CONFIG.WEN before every erase page partial and disabled using CONFIG.WEN after every erase page partial. Attempts to erase pages that are outside the code area may result in undesirable behavior, e.g. the wrong page may be erased.</p>																												

#### 4.3.9.10 ERASEPAGEPARTIALCFG

Address offset: 0x51C

Register for partial erase configuration

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																										A	A	A	A	A	A		
Reset 0x0000000A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
ID	Acce Field	Value ID	Value	Description																													
A	RW	DURATION		<p>Duration of the partial erase in milliseconds</p> <p>The user must ensure that the total erase time is long enough for a complete erase of the flash page.</p>																													

### 4.3.10 Electrical specification

#### 4.3.10.1 Flash programming

Symbol	Description	Min.	Typ.	Max.	Units
$n_{\text{WRITE}}$	Number of times a 32-bit word can be written before erase			2	
$n_{\text{ENDURANCE}}$	Erase cycles per page	10000			
$t_{\text{WRITE}}$	Time to write one 32-bit word			42.5 <sup>1</sup>	μs
$t_{\text{ERASEPAGE}}$	Time to erase one page			87.5 <sup>1</sup>	ms
$t_{\text{ERASEALL}}$	Time to erase all flash			173 <sup>1</sup>	ms
$t_{\text{ERASEPAGEPARTIAL,acc}}$	Accuracy of the partial page erase duration. Total execution time for one partial page erase is defined as $\text{ERASEPAGEPARTIALCFG} * t_{\text{ERASEPAGEPARTIAL,acc}}$			1.09 <sup>1</sup>	

## 4.4 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

<sup>1</sup> Applies when HFXO is used. Timing varies according to HFINT accuracy when HFINT is used.



## 4.4.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory information configuration	

Table 8: Instances

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption root, word 0	
ER[1]	0x084	Encryption root, word 1	
ER[2]	0x088	Encryption root, word 2	
ER[3]	0x08C	Encryption root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Build code (hardware version and production configuration)	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
INFO.UNUSED8[0]	0x114		Reserved
INFO.UNUSED8[1]	0x118		Reserved
INFO.UNUSED8[2]	0x11C		Reserved
PRODTEST[0]	0x350	Production test signature 0	
PRODTEST[1]	0x354	Production test signature 1	
PRODTEST[2]	0x358	Production test signature 2	
TEMP.A0	0x404	Slope definition A0	
TEMP.A1	0x408	Slope definition A1	
TEMP.A2	0x40C	Slope definition A2	
TEMP.A3	0x410	Slope definition A3	
TEMP.A4	0x414	Slope definition A4	
TEMP.A5	0x418	Slope definition A5	
TEMP.B0	0x41C	Y-intercept B0	
TEMP.B1	0x420	Y-intercept B1	
TEMP.B2	0x424	Y-intercept B2	
TEMP.B3	0x428	Y-intercept B3	
TEMP.B4	0x42C	Y-intercept B4	
TEMP.B5	0x430	Y-intercept B5	
TEMP.T0	0x434	Segment end T0	
TEMP.T1	0x438	Segment end T1	
TEMP.T2	0x43C	Segment end T2	
TEMP.T3	0x440	Segment end T3	
TEMP.T4	0x444	Segment end T4	

Table 9: Register overview

### 4.4.1.1 CODEPAGESIZE

Address offset: 0x010

Code memory page size

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce	Field	Value ID	Value	Description																											
A	R	CODEPAGESIZE			Code memory page size																											

### 4.4.1.2 CODESIZE

Address offset: 0x014

Code memory size

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
ID	Acce	Field	Value ID	Value	Description																											
A	R	CODESIZE			Code memory size in number of pages																											
					Total code space is: CODEPAGESIZE * CODESIZE																											

### 4.4.1.3 DEVICEID[n] (n=0..1)

Address offset: 0x060 + (n × 0x4)

Device identifier

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
ID	Acce	Field	Value ID	Value	Description																											
A	R	DEVICEID			64 bit unique device identifier																											
					DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.																											

### 4.4.1.4 ER[n] (n=0..3)

Address offset: 0x080 + (n × 0x4)

Encryption root, word n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
ID	Acce	Field	Value ID	Value	Description																											
A	R	ER			Encryption root, word n																											

### 4.4.1.5 IR[n] (n=0..3)

Address offset: 0x090 + (n × 0x4)

## Identity Root, word n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	R	IR		Identity Root, word n																												

## 4.4.1.6 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	R	DEVICEADDRTYPE		Device address type																												
		Public	0	Public address																												
		Random	1	Random address																												

## 4.4.1.7 DEVICEADDR[n] (n=0..1)

Address offset: 0x0A4 + (n × 0x4)

Device address n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	R	DEVICEADDR		48 bit device address																												
				DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.																												

## 4.4.1.8 INFO.PART

Address offset: 0x100

Part code

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
Reset 0x00052820	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	R	PART		Part code																													
		N52820	0x52820	nRF52820																													
		N52833	0x52833	nRF52833																													
		N52840	0x52840	nRF52840																													
		Unspecified	0xFFFFFFFF	Unspecified																													

### 4.4.1.9 INFO.VARIANT

Address offset: 0x104

Build code (hardware version and production configuration)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce	Field	Value ID	Value	Description																											
A	R	VARIANT			Build code (hardware version and production configuration). Encoded as ASCII.																											
			AAAA	0x41414141	AAAA																											
			Unspecified	0xFFFFFFFF	Unspecified																											

### 4.4.1.10 INFO.PACKAGE

Address offset: 0x108

Package option

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce	Field	Value ID	Value	Description																											
A	R	PACKAGE			Package option																											
			QD	0x2007	QDxx - 40-pin QFN																											
			Unspecified	0xFFFFFFFF	Unspecified																											

### 4.4.1.11 INFO.RAM

Address offset: 0x10C

RAM variant

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce	Field	Value ID	Value	Description																											
A	R	RAM			RAM variant																											
			K16	0x10	16 kByte RAM																											
			K32	0x20	32 kByte RAM																											
			K64	0x40	64 kByte RAM																											
			K128	0x80	128 kByte RAM																											
			K256	0x100	256 kByte RAM																											
			Unspecified	0xFFFFFFFF	Unspecified																											

### 4.4.1.12 INFO.FLASH

Address offset: 0x110

Flash variant

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R FLASH			Flash variant																												
		K128	0x80	128 kByte FLASH																												
		K256	0x100	256 kByte FLASH																												
		K512	0x200	512 kByte FLASH																												
		K1024	0x400	1 MByte FLASH																												
		K2048	0x800	2 MByte FLASH																												
		Unspecified	0xFFFFFFFF	Unspecified																												

#### 4.4.1.13 PRODTST[n] (n=0..2)

Address offset: 0x350 + (n × 0x4)

Production test signature n

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R PRODTST			Production test signature n																												
		Done	0xBB42319F	Production tests done																												
		NotDone	0xFFFFFFFF	Production tests not done																												

#### 4.4.1.14 TEMP.A0

Address offset: 0x404

Slope definition A0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R A			A (slope definition) register.																												

#### 4.4.1.15 TEMP.A1

Address offset: 0x408

Slope definition A1

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R A			A (slope definition) register.																												

#### 4.4.1.16 TEMP.A2

Address offset: 0x40C

Slope definition A2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																						
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																				
ID	Acce	Field	Value ID	Value	Description																																																	
A	R	A			A (slope definition) register.																																																	

#### 4.4.1.17 TEMP.A3

Address offset: 0x410

Slope definition A3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																			
ID	Acce	Field	Value ID	Value	Description																																																
A	R	A			A (slope definition) register.																																																

#### 4.4.1.18 TEMP.A4

Address offset: 0x414

Slope definition A4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																			
ID	Acce	Field	Value ID	Value	Description																																																
A	R	A			A (slope definition) register.																																																

#### 4.4.1.19 TEMP.A5

Address offset: 0x418

Slope definition A5

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																			
ID	Acce	Field	Value ID	Value	Description																																																
A	R	A			A (slope definition) register.																																																

#### 4.4.1.20 TEMP.B0

Address offset: 0x41C

Y-intercept B0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																					
ID	Acce	Field	Value ID	Value	Description																																																
A	R	B				B (y-intercept)																																															

#### 4.4.1.21 TEMP.B1

Address offset: 0x420

Y-intercept B1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																				
ID	Acce	Field	Value ID	Value	Description																																															
A	R	B				B (y-intercept)																																														

#### 4.4.1.22 TEMP.B2

Address offset: 0x424

Y-intercept B2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																				
ID	Acce	Field	Value ID	Value	Description																																															
A	R	B				B (y-intercept)																																														

#### 4.4.1.23 TEMP.B3

Address offset: 0x428

Y-intercept B3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																				
ID	Acce	Field	Value ID	Value	Description																																															
A	R	B				B (y-intercept)																																														

#### 4.4.1.24 TEMP.B4

Address offset: 0x42C

Y-intercept B4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																				
ID	Acce	Field	Value ID	Value	Description																																															
A	R	B				B (y-intercept)																																														

#### 4.4.1.25 TEMP.B5

Address offset: 0x430

Y-intercept B5

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0xFFFFFFFF</b>																								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ID	Acce Field	Value ID	Value	Description																																																	
A	R	B		B (y-intercept)																																																	

#### 4.4.1.26 TEMP.T0

Address offset: 0x434

Segment end T0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0xFFFFFFFF</b>																								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ID	Acce Field	Value ID	Value	Description																																																	
A	R	T		T (segment end) register																																																	

#### 4.4.1.27 TEMP.T1

Address offset: 0x438

Segment end T1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0xFFFFFFFF</b>																								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ID	Acce Field	Value ID	Value	Description																																																	
A	R	T		T (segment end) register																																																	

#### 4.4.1.28 TEMP.T2

Address offset: 0x43C

Segment end T2

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0xFFFFFFFF</b>																								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ID	Acce Field	Value ID	Value	Description																																																	
A	R	T		T (segment end) register																																																	

#### 4.4.1.29 TEMP.T3

Address offset: 0x440

Segment end T3



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R	T	T (segment end) register																													

#### 4.4.1.30 TEMPT4

Address offset: 0x444

Segment end T4

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0xFFFFFFFF	1 1																															
ID	Acce Field	Value ID	Value	Description																												
A	R	T	T (segment end) register																													

## 4.5 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user-specific settings.

For information on writing UICR registers, see the [NVMC — Non-volatile memory controller](#) on page 19 and [Memory](#) on page 15 chapters.

### 4.5.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x10001000	UICR	UICR	User information configuration	

Table 10: Instances

Register	Offset	Description
UNUSED0	0x000	Reserved
UNUSED1	0x004	Reserved
UNUSED2	0x008	Reserved
UNUSED3	0x010	Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design
NRFFW[1]	0x018	Reserved for Nordic firmware design
NRFFW[2]	0x01C	Reserved for Nordic firmware design
NRFFW[3]	0x020	Reserved for Nordic firmware design
NRFFW[4]	0x024	Reserved for Nordic firmware design
NRFFW[5]	0x028	Reserved for Nordic firmware design
NRFFW[6]	0x02C	Reserved for Nordic firmware design
NRFFW[7]	0x030	Reserved for Nordic firmware design
NRFFW[8]	0x034	Reserved for Nordic firmware design
NRFFW[9]	0x038	Reserved for Nordic firmware design
NRFFW[10]	0x03C	Reserved for Nordic firmware design
NRFFW[11]	0x040	Reserved for Nordic firmware design
NRFFW[12]	0x044	Reserved for Nordic firmware design
NRFFHW[0]	0x050	Reserved for Nordic hardware design

Register	Offset	Description
NRFHW[1]	0x054	Reserved for Nordic hardware design
NRFHW[2]	0x058	Reserved for Nordic hardware design
NRFHW[3]	0x05C	Reserved for Nordic hardware design
NRFHW[4]	0x060	Reserved for Nordic hardware design
NRFHW[5]	0x064	Reserved for Nordic hardware design
NRFHW[6]	0x068	Reserved for Nordic hardware design
NRFHW[7]	0x06C	Reserved for Nordic hardware design
NRFHW[8]	0x070	Reserved for Nordic hardware design
NRFHW[9]	0x074	Reserved for Nordic hardware design
NRFHW[10]	0x078	Reserved for Nordic hardware design
NRFHW[11]	0x07C	Reserved for Nordic hardware design
CUSTOMER[0]	0x080	Reserved for customer
CUSTOMER[1]	0x084	Reserved for customer
CUSTOMER[2]	0x088	Reserved for customer
CUSTOMER[3]	0x08C	Reserved for customer
CUSTOMER[4]	0x090	Reserved for customer
CUSTOMER[5]	0x094	Reserved for customer
CUSTOMER[6]	0x098	Reserved for customer
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access port protection
DEBUGCTRL	0x210	Processor debug control
REGOUT0	0x304	Output voltage from REG0 regulator stage. The maximum output voltage from this stage is given as VDDH - VREGDROP.

Table 11: Register overview

### 4.5.1.1 NRFFW[n] (n=0..12)

Address offset:  $0x014 + (n \times 0x4)$

Reserved for Nordic firmware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	RW NRFFW			Reserved for Nordic firmware design																												

### 4.5.1.2 NRFHW[n] (n=0..11)

Address offset:  $0x050 + (n \times 0x4)$

Reserved for Nordic hardware design

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	RW NRFHW			Reserved for Nordic hardware design																												

### 4.5.1.3 CUSTOMER[n] (n=0..31)

Address offset:  $0x080 + (n \times 0x4)$

Reserved for customer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	RW CUSTOMER			Reserved for customer																												

### 4.5.1.4 PSELRESET[n] (n=0..1)

Address offset:  $0x200 + (n \times 0x4)$

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If values are not the same, there will be no nRESET function exposed on a GPIO. As a result, the device will always start independently of the levels present on any of the GPIOs.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	C																															
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																												
A	RW PIN		18	GPIO pin number onto which nRESET is exposed																												
C	RW CONNECT			Connection																												
		Disconnected	1	Disconnect																												
		Connected	0	Connect																												

### 4.5.1.5 APPROTECT

Address offset: 0x208

Access port protection

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																										
ID																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																																										
ID	Acce	Field	Value ID	Value	Description																																																						
A	RW	PALL			Enable or disable access port protection.																																																						
			Disabled	0xFF	Disable																																																						
			Enabled	0x00	Enable																																																						

See [Debug](#) on page 40 for more information.

### 4.5.1.6 DEBUGCTRL

Address offset: 0x210

Processor debug control

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																										
ID																															B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																																										
ID	Acce	Field	Value ID	Value	Description																																																						
B	RW	CPUPBEN			Configure CPU flash patch and breakpoint (FPB) unit behavior																																																						
			Enabled	0xFF	Enable CPU FPB unit (default behavior)																																																						
			Disabled	0x00	Disable CPU FPB unit. Writes into the FPB registers will be ignored.																																																						

### 4.5.1.7 REGOUT0

Address offset: 0x304

Output voltage from REG0 regulator stage. The maximum output voltage from this stage is given as VDDH - VREGODROP.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																															A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																
ID	Acce	Field	Value ID	Value	Description																												
A	RW	VOUT			Output voltage from REG0 regulator stage.																												
			1V8	0	1.8 V																												
			2V1	1	2.1 V																												
			2V4	2	2.4 V																												
			2V7	3	2.7 V																												
			3V0	4	3.0 V																												
			3V3	5	3.3 V																												
			DEFAULT	7	Default voltage: 1.8 V																												

## 4.6 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in [EasyDMA example](#) on page 37.

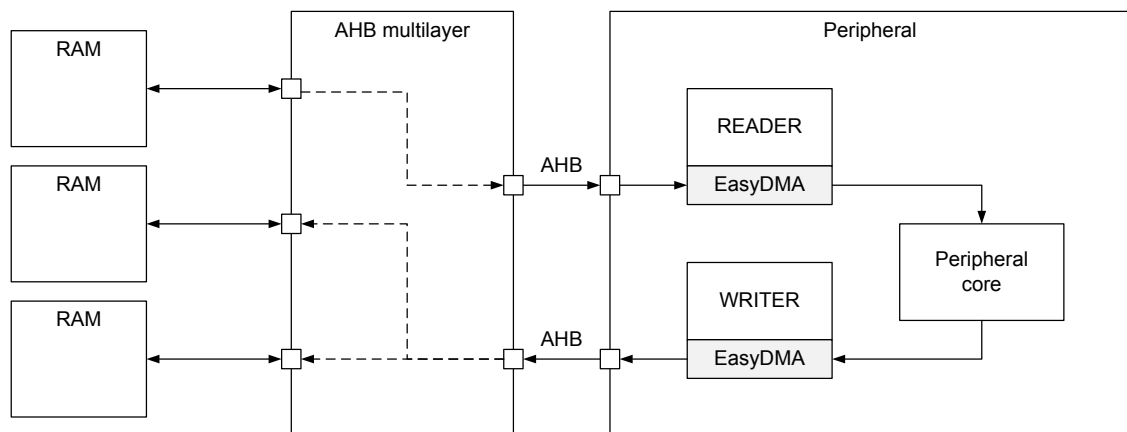


Figure 4: EasyDMA example

An EasyDMA channel is implemented in the following way, but some variations may occur:

```

READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;

```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will perform the following tasks:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000
- Process the data
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005

The memory layout of these buffers is illustrated in [EasyDMA memory layout](#) on page 38.

0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 5: EasyDMA memory layout

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

**Note:** The PTR register of a READER or WRITER must point to a valid memory region before use. The reset value of a PTR register is not guaranteed to point to valid memory. See [Memory](#) on page 15 for more information about the different memory regions and EasyDMA connectivity.

### 4.6.1 EasyDMA error handling

Some errors may occur during DMA handling.

If READER.PTR or WRITER.PTR is not pointing to a valid memory region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

If several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. An EasyDMA channel is an AHB master. Depending on the peripheral, the peripheral may either stall and wait for access to be granted, or lose data.

### 4.6.2 EasyDMA array list

EasyDMA is able to operate in Array List mode.

The Array List mode is implemented in channels where the LIST register is available.

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA Array List can be implemented by using the data structure `ArrayList_type` as illustrated in the code example below using a `READER` EasyDMA channel as an example:

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
    uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3] __at__ 0x20000000;

MYPERIPHERAL->READER.MAXCNT = BUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &ReaderList;
MYPERIPHERAL->READER.LIST = MYPERIPHERAL_READER_LIST_ArrayList;
```

The data structure only includes a buffer with size equal to the size of `READER.MAXCNT` register. EasyDMA uses the `READER.MAXCNT` register to determine when the buffer is full.

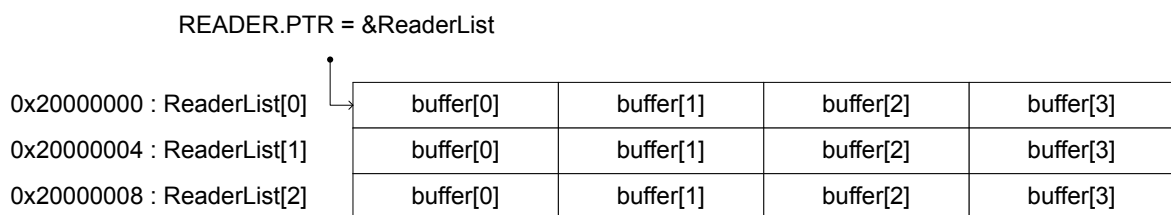


Figure 6: EasyDMA array list

## 4.7 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to all the slave devices using an interconnection matrix. The bus masters are assigned priorities, which are used to resolve access when two (or more) bus masters request access to the same slave device. When that occurs, the following rules apply:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted the access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- Bus masters that have the same priority are mutually exclusive, thus cannot be used concurrently.

Some peripherals, such as `RADIO`, do not have a safe stalling mechanism (no internal data buffering, or opportunity to pause incoming data). Being a low priority bus master might cause loss of data for such peripherals upon bus contention. To avoid AHB bus contention when using multiple bus masters, follow these guidelines:

- Avoid situations where more than one bus master is accessing the same slave.
- If more than one bus master is accessing the same slave, make sure that the bus bandwidth is not exhausted.

Below is a list of bus masters in the system and their priorities.

Bus master name	Description
CPU	
CTRL-AP	
USB	
SPIM1/SPIS1/TWIM1/TWIS1	Same priority and mutually exclusive
RADIO	
CCM/ECB/AAR	Same priority and mutually exclusive
UARTE0	
SPIM0/SPIS0/TWIM0/TWIS0	Same priority and mutually exclusive

Table 12: AHB bus masters (listed from highest to lowest priority)

Defined bus masters are the CPU and peripherals with implemented EasyDMA. The available slaves are RAM AHB slaves. How the bus masters and slaves are connected using the interconnection matrix is illustrated in [Memory](#) on page 15.

## 4.8 Debug

Debug system offers a flexible and powerful mechanism for non-intrusive debugging.

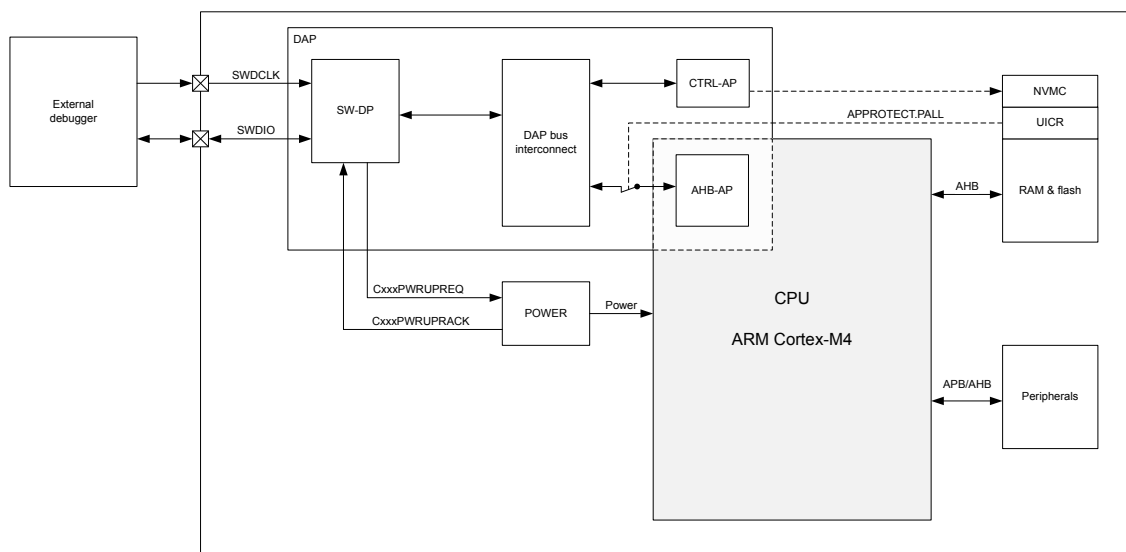


Figure 7: Debug overview

The main features of the debug system are the following:

- Two-pin serial wire debug (SWD) interface
- Flash patch and breakpoint (FPB) unit that supports:
  - Two literal comparators
  - Six instruction comparators

### 4.8.1 DAP - Debug access port

An external debugger can access the device via the DAP.



The debug access port (DAP) implements a standard ARM® CoreSight™ serial wire debug port (SW-DP), which implements the serial wire debug protocol (SWD). SWD is a two-pin serial interface, see SWDCLK and SWDIO in [Debug overview](#) on page 40.

In addition to the default access port in CPU (AHB-AP), the DAP includes a custom control access port (CTRL-AP). The CTRL-AP is described in more detail in [CTRL-AP - Control access port](#) on page 41.

**Note:**

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

## 4.8.2 CTRL-AP - Control access port

The control access port (CTRL-AP) is a custom access port that enables control of the device when other access ports in the DAP are disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register [APPROTECT](#) on page 36 for more information on enabling access port protection.

Control access port has the following features:

- Soft reset, see [Reset](#) on page 57 for more information
- Disabling of access port protection, which is the reason why CTRL-AP allows control of the device even when all other access ports in the DAP are disabled by the access port protection

Access port protection is disabled by issuing an ERASEALL command via CTRL-AP. This command will erase the flash, UICR, and RAM.

### 4.8.2.1 Registers

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP identification register, IDR

Table 13: Register overview

#### 4.8.2.1.1 RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	RESET		Soft reset triggered through CTRL-AP. See Reset behavior in POWER chapter for more details.																												
		NoReset	0	Reset is not active																												
		Reset	1	Reset is active. Device is held in reset.																												

#### 4.8.2.1.2 ERASEALL

Address offset: 0x004

Erase all

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																	A
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	W	ERASEALL		Erase all flash and RAM																													
		NoOperation	0	No operation																													
		Erase	1	Erase all flash and RAM																													

#### 4.8.2.1.3 ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																	A
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	R	ERASEALLSTATUS		Status register for the ERASEALL operation																													
		Ready	0	ERASEALL is ready																													
		Busy	1	ERASEALL is busy (on-going)																													

#### 4.8.2.1.4 APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																	A
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	R	APPROTECTSTATUS		Status register for access port protection																													
		Enabled	0	Access port protection enabled																													
		Disabled	1	Access port protection not enabled																													

#### 4.8.2.1.5 IDR

Address offset: 0x0FC

CTRL-AP identification register, IDR

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	E	E	E	E	D	D	D	D	C	C	C	C	C	C	C	B	B	B	B							A	A	A	A	A	A	A	A
Reset 0x02880000	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																												
A	R	APID			AP identification																												
B	R	CLASS			Access port (AP) class																												
			NotDefined	0x0	No defined class																												
			MEMAP	0x8	Memory access port																												
C	R	JEP106ID			JEDEC JEP106 identity code																												
D	R	JEP106CONT			JEDEC JEP106 continuation code																												
E	R	REVISION			Revision																												

## 4.8.2.2 Electrical specification

### 4.8.2.2.1 Control access port

Symbol	Description	Min.	Typ.	Max.	Units
$R_{pull}$	Internal SWDIO and SWDCLK pull up/down resistance		13		k $\Omega$
$f_{SWDCLK}$	SWDCLK frequency	0.125		8	MHz

## 4.8.3 Debug interface mode

Before an external debugger can access either CPU's access port (AHB-AP) or the control access port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in [RESETREAS](#) on page 62 will be set. The device is in the debug interface mode as long as the debugger is requesting power via CxxxPWRUPREQ. Once the debugger stops requesting power via CxxxPWRUPREQ, the device is back in normal mode. Some peripherals behave differently in Debug Interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption is higher in debug interface mode than in normal mode.

For details on how to use the debug capabilities, read the debug documentation of your IDE.

## 4.8.4 Real-time debug

The nRF52820 supports real-time debugging.

Real-time debugging allows interrupts to execute to completion in real time when breakpoints are set in thread mode or lower priority interrupts. This enables developers to set breakpoints and single-step through the code without the risk of real-time event-driven threads running at higher priority failing. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

# 5 Power and clock management

## 5.1 Power management unit (PMU)

Power and clock management in nRF52820 is designed to automatically ensure maximum power efficiency.

The core of the power and clock management system is the power management unit (PMU) illustrated in the following figure.

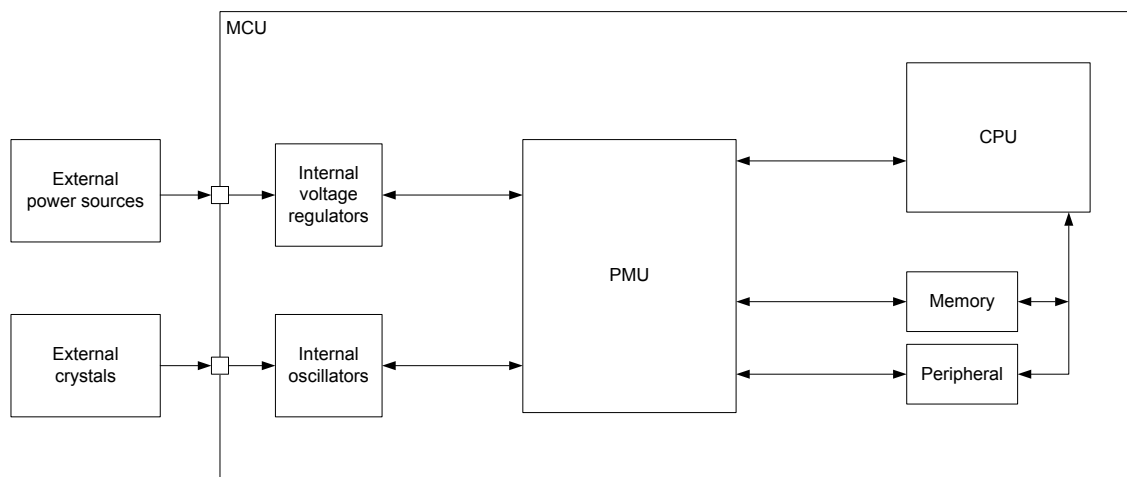


Figure 8: Power management unit

The PMU automatically detects which power and clock resources are required by the different system components at any given time. The PMU will then automatically start/stop and choose operation modes in supply regulators and clock sources, to achieve the lowest power consumption possible.

## 5.2 Current consumption

Because the system is continually being tuned by the [Power management unit \(PMU\)](#) on page 44, estimating an application's current consumption can be challenging when measurements cannot be directly performed on the hardware. To facilitate the estimation process, a set of current consumption scenarios are provided to show the typical current drawn from the VDD supply.

Each scenario specifies a set of operations and conditions applying to the given scenario. The following table shows a set of common conditions used in all scenarios, unless otherwise stated in the description of a given scenario. All scenarios are listed in [Electrical specification](#) on page 45.

Condition	Value
Supply	3 V on VDD/VDDH (Normal voltage mode)
Temperature	25°C
CPU	WFI (wait for interrupt)/WFE (wait for event) sleep
Peripherals	All idle
Clock	Not running
Regulator	LDO
RAM	In System ON, full 32 kB powered. In System OFF, full 32 kB retention.
Compiler	GCC v7.3.1 20180622 (release) [ARM/embedded-7-branch revision 261907] (GNU Tools for Arm Embedded Processors 7-2018-q3-update). <ul style="list-style-type: none"> <li>• Compiler flags: <code>-O0 -falign-functions=16 -fno-strict-aliasing -mthumb -mcpu=cortex-m4 -mfloat-abi=hard -mfpu=fpv4-sp-d16</code>.</li> </ul>
Compiler for CPU Running and Compounded	ARMCC v6.13. <ul style="list-style-type: none"> <li>• Compiler flags: <code>-xc -std=gnu99 --target=arm-arm-none-eabi -mcpu=cortex-m4 -mfpu=none -mfloat-abi=soft -c -fno-rtti -funsigned-char -gdwarf-3 -fropi -Ofast -ffunction-sections -Omax</code></li> <li>• Linker flags: <code>--cpu=Cortex-M4 --fpu=SoftVFP --strict -Omax</code></li> </ul>
32 MHz crystal <sup>2</sup>	SMD 2520, 32 MHz, 10 pF +/- 10 ppm

Table 14: Current consumption scenarios, common conditions

## 5.2.1 Electrical specification

### 5.2.1.1 Sleep

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>ON_RAMOFF_EVENT</sub>	System ON, no RAM retention, wake on any event		0.4		μA
I <sub>ON_RAMON_EVENT</sub>	System ON, full 32 kB RAM retention, wake on any event		0.6		μA
I <sub>ON_RAMON_POF</sub>	System ON, full 32 kB RAM retention, wake on any event, power-fail comparator enabled		0.8		μA
I <sub>ON_RAMON_GPIOTE</sub>	System ON, full 32 kB RAM retention, wake on GPIOTE input (event mode)		2.5		μA
I <sub>ON_RAMON_GPIOTEPORT</sub>	System ON, full 32 kB RAM retention, wake on GPIOTE PORT event		0.6		μA
I <sub>ON_RAMOFF_RTC</sub>	System ON, no RAM retention, wake on RTC (running from LFRC clock)		1.2		μA
I <sub>ON_RAMON_RTC</sub>	System ON, full 32 kB RAM retention, wake on RTC (running from LFRC clock)		1.4		μA
I <sub>OFF_RAMOFF_RESET</sub>	System OFF, no RAM retention, wake on reset		0.3		μA
I <sub>OFF_RAMON_RESET</sub>	System OFF, full 32 kB RAM retention, wake on reset		0.5		μA

<sup>2</sup> Applies only when HFXO is running

Symbol	Description	Min.	Typ.	Max.	Units
$I_{ON\_RAMOFF\_EVENT\_5V}$	System ON, no RAM retention, wake on any event, 5 V supply on VDDH, REGO output = 3.3 V		0.9		$\mu A$
$I_{OFF\_RAMOFF\_RESET\_5V}$	System OFF, no RAM retention, wake on reset, 5 V supply on VDDH, REGO output = 3.3 V		0.7		$\mu A$

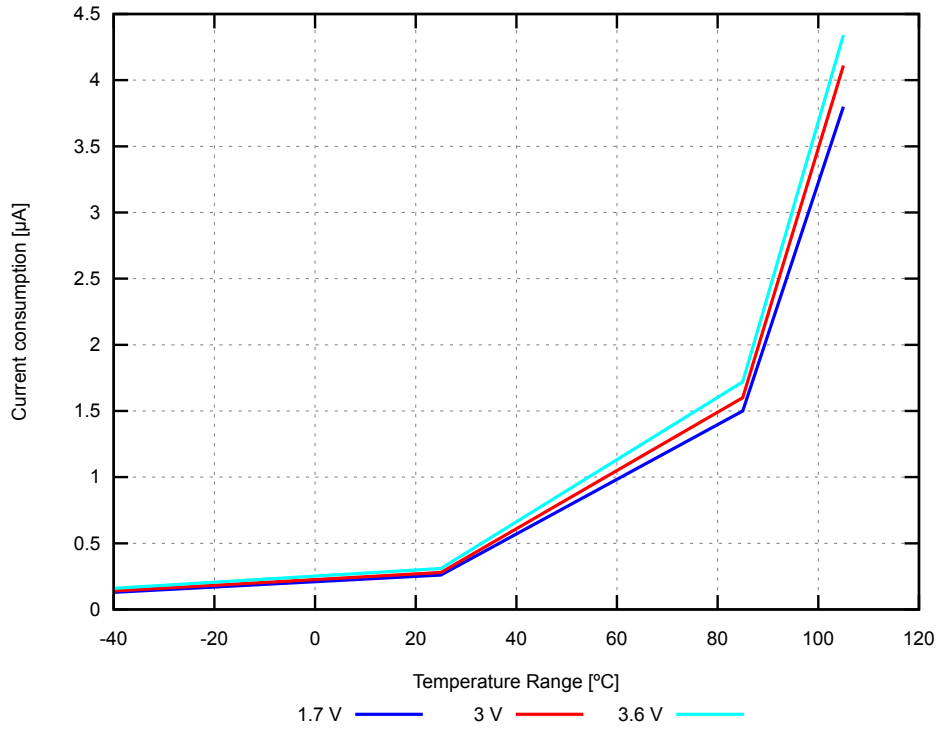


Figure 9: System OFF, no RAM retention, wake on reset (typical values)

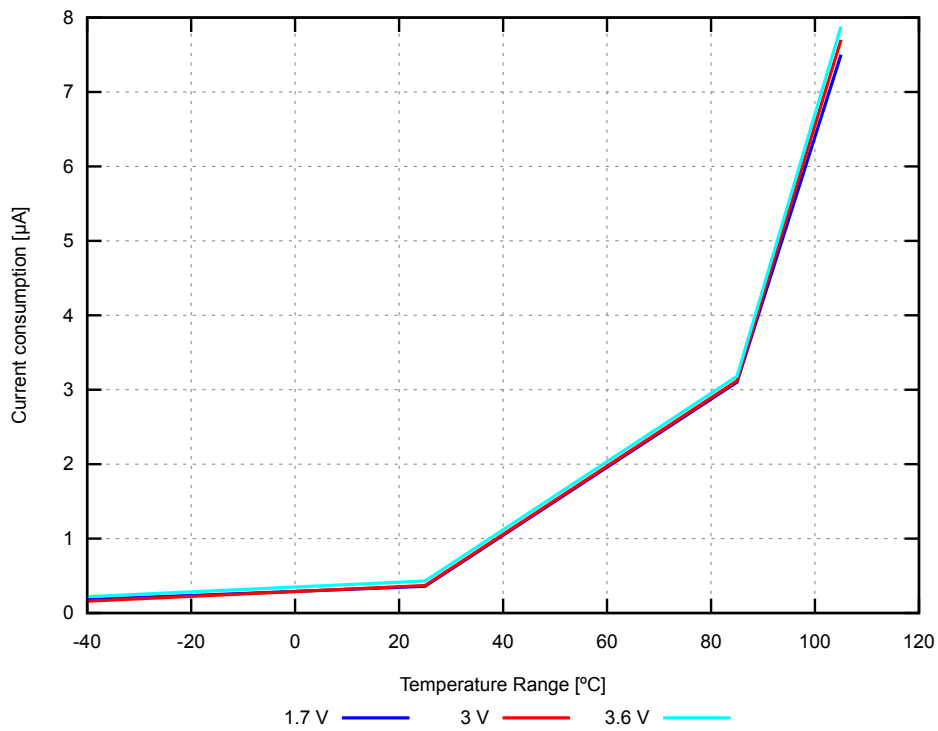


Figure 10: System ON, no RAM retention, wake on any event (typical values)

### 5.2.1.2 COMP active

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>COMP,LP</sub>	COMP enabled, low power mode		21.4		μA
I <sub>COMP,NORM</sub>	COMP enabled, normal mode		25.3		μA
I <sub>COMP,HS</sub>	COMP enabled, high-speed mode		33.0		μA

### 5.2.1.3 CPU running

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>CPU0</sub>	CPU running CoreMark @64 MHz from flash, Clock = HFXO, Regulator = DC/DC		2.1		mA
I <sub>CPU1</sub>	CPU running CoreMark @64 MHz from flash, Clock = HFXO		3.9		mA
I <sub>CPU2</sub>	CPU running CoreMark @64 MHz from RAM, Clock = HFXO, Regulator = DC/DC		2.1		mA
I <sub>CPU3</sub>	CPU running CoreMark @64 MHz from RAM, Clock = HFXO		3.8		mA
I <sub>CPU4</sub>	CPU running CoreMark @64 MHz from flash, Clock = HFINT, Regulator = DC/DC		1.9		mA

### 5.2.1.4 Radio transmitting/receiving

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>RADIO_TX0</sub>	Radio transmitting @ 8 dBm output power, 1 Mbps Bluetooth <sup>®</sup> Low Energy (BLE) mode, Clock = HFXO, Regulator = DC/DC		15.0		mA
I <sub>RADIO_TX1</sub>	Radio transmitting @ 0 dBm output power, 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC		5.9		mA
I <sub>RADIO_TX2</sub>	Radio transmitting @ -40 dBm output power, 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC		3.4		mA
I <sub>RADIO_TX3</sub>	Radio transmitting @ 0 dBm output power, 1 Mbps BLE mode, Clock = HFXO		10.9		mA
I <sub>RADIO_TX4</sub>	Radio transmitting @ -40 dBm output power, 1 Mbps BLE mode, Clock = HFXO		5.2		mA
I <sub>RADIO_TX5</sub>	Radio transmitting @ 0 dBm output power, 250 kbit/s IEE 802.15.4-2006 mode, Clock = HFXO, Regulator = DC/DC		5.9		mA
I <sub>RADIO_RX0</sub>	Radio receiving @ 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC		5.8		mA
I <sub>RADIO_RX1</sub>	Radio receiving @ 1 Mbps BLE mode, Clock = HFXO		10.5		mA
I <sub>RADIO_RX2</sub>	Radio receiving @ 250 kbit/s IEE 802.15.4-2006 mode, Clock = HFXO, Regulator = DC/DC		6.0		mA

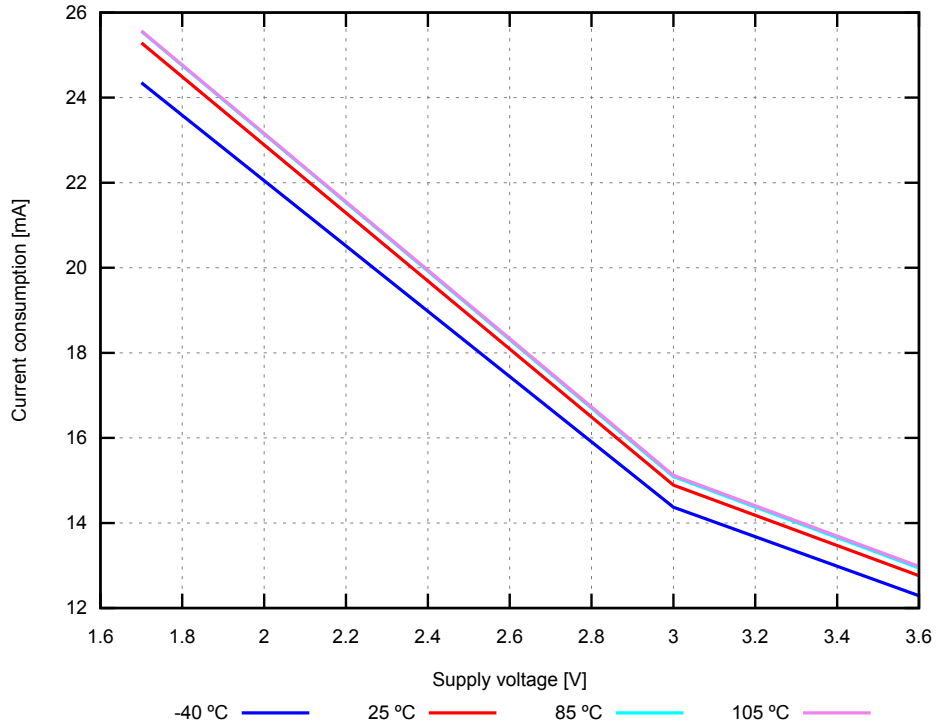


Figure 11: Radio transmitting @ 8 dBm output power, 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC (typical values)

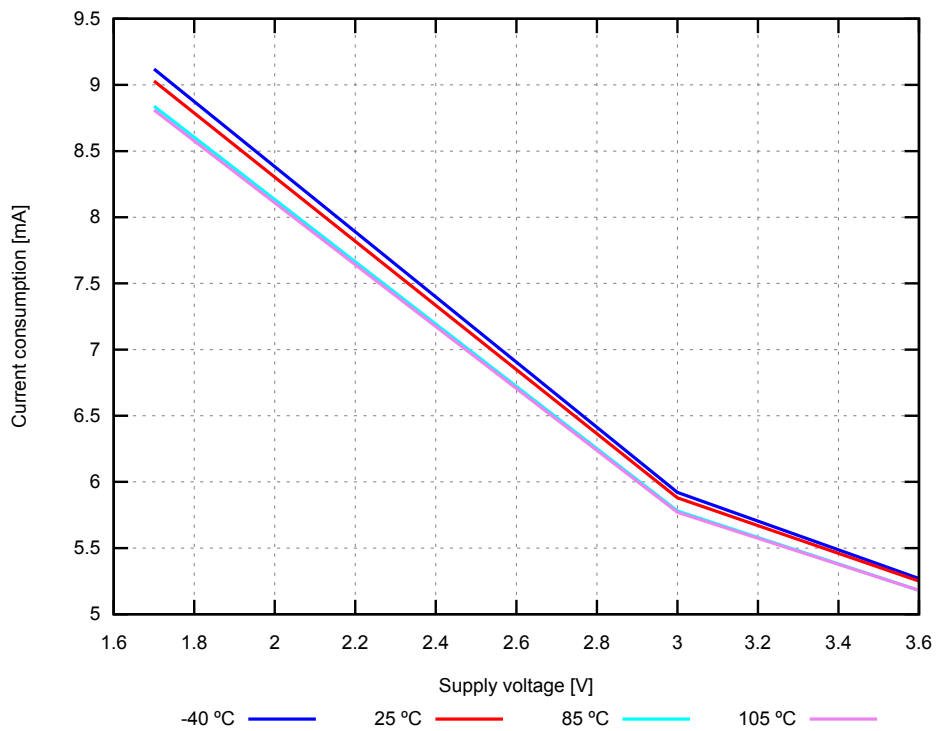


Figure 12: Radio transmitting @ 0 dBm output power, 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC (typical values)



### 5.2.1.5 RNG active

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>RNG0</sub>	RNG running		471		μA

### 5.2.1.6 TEMP active

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>TEMP0</sub>	TEMP started		0.62		mA

### 5.2.1.7 TIMER running

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>TIMER0</sub>	One TIMER instance running @ 1 MHz, Clock = HFINT		326		μA
I <sub>TIMER1</sub>	Two TIMER instances running @ 1 MHz, Clock = HFINT		327		μA
I <sub>TIMER2</sub>	One TIMER instance running @ 1 MHz, Clock = HFXO		511		μA
I <sub>TIMER3</sub>	One TIMER instance running @ 16 MHz, Clock = HFINT		426		μA
I <sub>TIMER4</sub>	One TIMER instance running @ 16 MHz, Clock = HFXO		612		μA

### 5.2.1.8 WDT active

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>WDT,STARTED</sub>	WDT started		1.4		μA

### 5.2.1.9 Compounded

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>S0</sub>	CPU running CoreMark from flash, Radio transmitting @ 0 dBm output power, 1 Mbps <i>Bluetooth</i> <sup>®</sup> Low Energy (BLE) mode, Clock = HFXO, Regulator = DC/DC		7.3		mA
I <sub>S1</sub>	CPU running CoreMark from flash, Radio receiving @ 1 Mbps BLE mode, Clock = HFXO, Regulator = DC/DC		7.2		mA
I <sub>S2</sub>	CPU running CoreMark from flash, Radio transmitting @ 0 dBm output power, 1 Mbps BLE mode, Clock = HFXO		14.1		mA
I <sub>S3</sub>	CPU running CoreMark from flash, Radio receiving @ 1 Mbps BLE mode, Clock = HFXO		13.7		mA

## 5.3 POWER — Power supply

The power supply consists of a number of LDO and DC/DC regulators that are utilized to maximize the system's power efficiency.

This device has the following power supply features:

- On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- Supervisor hardware to manage power-on reset, brownout, and power failure
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency

- Separate USB supply

### 5.3.1 Main supply

The main supply voltage is connected to the VDD/VDDH pins. The system will enter one of two supply voltage modes, Normal or High Voltage mode, depending on how the supply voltage is connected to these pins.

The system enters Normal Voltage mode when the supply voltage is connected to both the VDD and VDDH pins (pin VDD shorted to pin VDDH). For the supply voltage range to connect to both VDD and VDDH pins, see parameter  $V_{DD}$ .

The system enters High Voltage mode when the supply voltage is only connected to the VDDH pin and the VDD pin is not connected to any voltage supply. For the supply voltage range to connect to the VDDH pin, see parameter  $V_{DDH}$ .

The register `MAINREGSTATUS` on page 66 can be used to read the current supply voltage mode.

#### 5.3.1.1 Main voltage regulators

The system contains two main supply regulator stages, REG0 and REG1.

REG1 regulator stage has the regulator type options of Low-dropout regulator (LDO) and Buck regulator (DC/DC). REG0 regulator stage has only the option of Low-dropout regulator (LDO).

In Normal Voltage mode, only the REG1 regulator stage is used, and the REG0 stage is automatically disabled. In High Voltage mode, both regulator stages (REG0 and REG1) are used. The output voltage of REG0 can be configured in register `REGOUT0` on page 36. This output voltage is connected to VDD and is the input voltage to REG1.

**Note:** In High Voltage mode, the configured output voltage for REG0 (`REGOUT0` on page 36) must not be greater than REG0 input voltage minus the voltage drop in REG0 ( $V_{DDH} - V_{REG0,DROP}$ ).

By default, the LDO regulators are enabled and the DC/DC regulator of REG1 stage is disabled. Register `DCDCEN` on page 66 is used to enable the DC/DC regulator for REG1 stage.

When the REG1 DC/DC converter is enabled, the LDO for the REG1 stage will be disabled. External LC filters must be connected for the DC/DC regulator if it is being used. The advantage of using the DC/DC regulator is that the overall power consumption is normally reduced as the efficiency of such a regulator is higher than that of a LDO. The efficiency gained by using the DC/DC regulator is best seen when the regulator voltage drop (difference between input and output voltage) is high. The efficiency of internal regulators vary with the supply voltage and the current drawn from the regulators.

**Note:** Do not enable the DC/DC regulator without an external LC filter being connected as this will inhibit device operation, including debug access, until an LC filter is connected.

#### 5.3.1.2 GPIO levels

The GPIO high reference voltage is equal to the level on the VDD pin.

In Normal Voltage mode, the GPIO high level equals the voltage supplied to the VDD pin. In High Voltage mode, it equals the level specified in register `REGOUT0` on page 36.

#### 5.3.1.3 Regulator configuration examples

The voltage regulators can be configured in several ways, depending on the selected supply voltage mode (Normal/High) and the regulator type option for REG1 (LDO or DC/DC).

Four configuration examples are illustrated in the following figures.

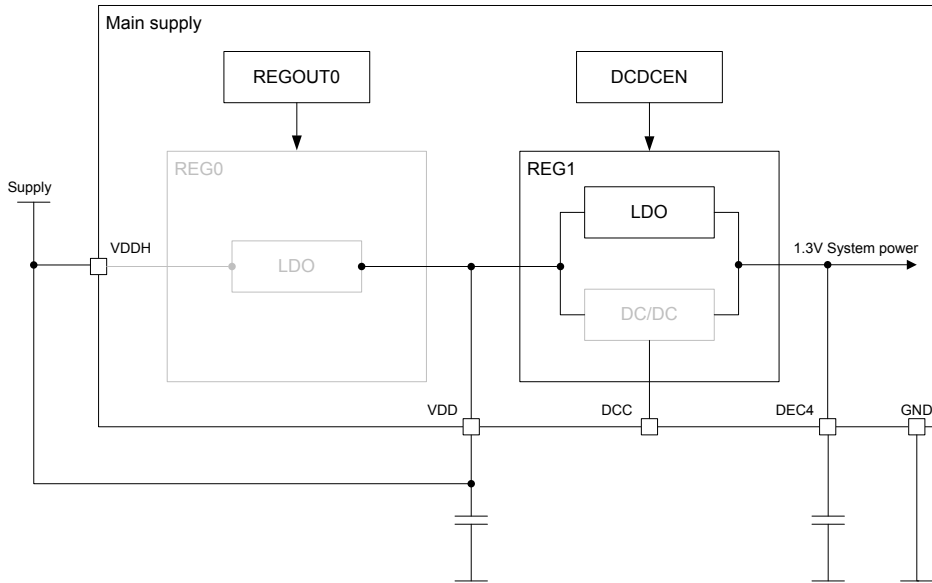


Figure 13: Normal Voltage mode, REG1 LDO

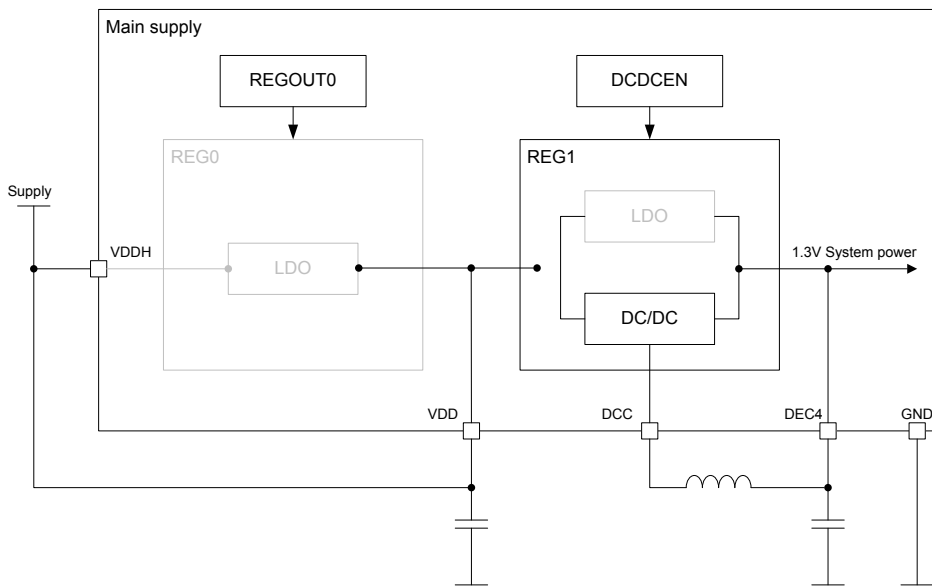


Figure 14: Normal Voltage mode, REG1 DC/DC

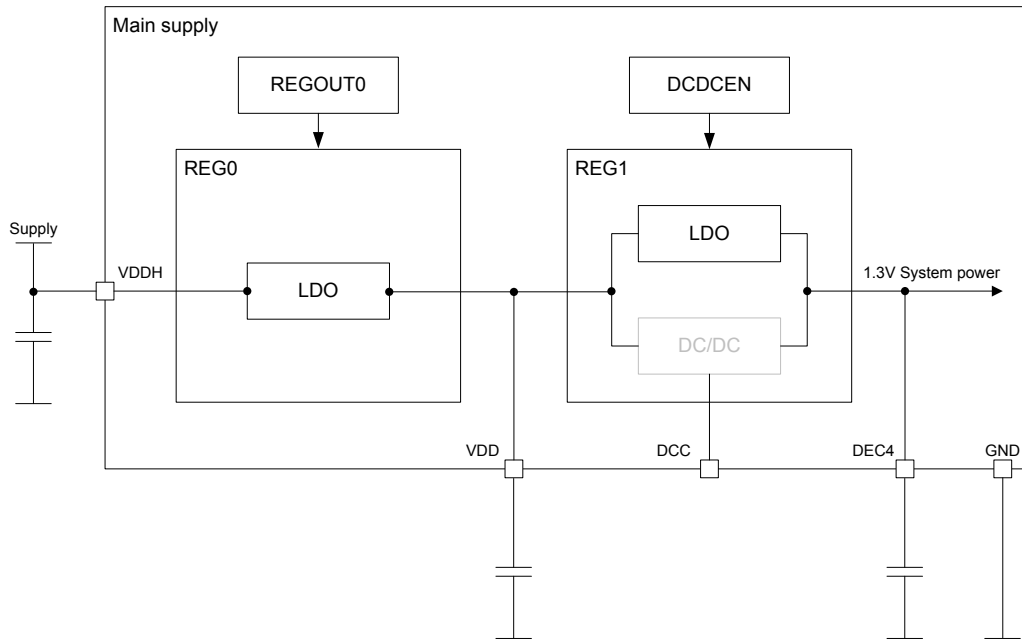


Figure 15: High Voltage mode, REG1 LDO

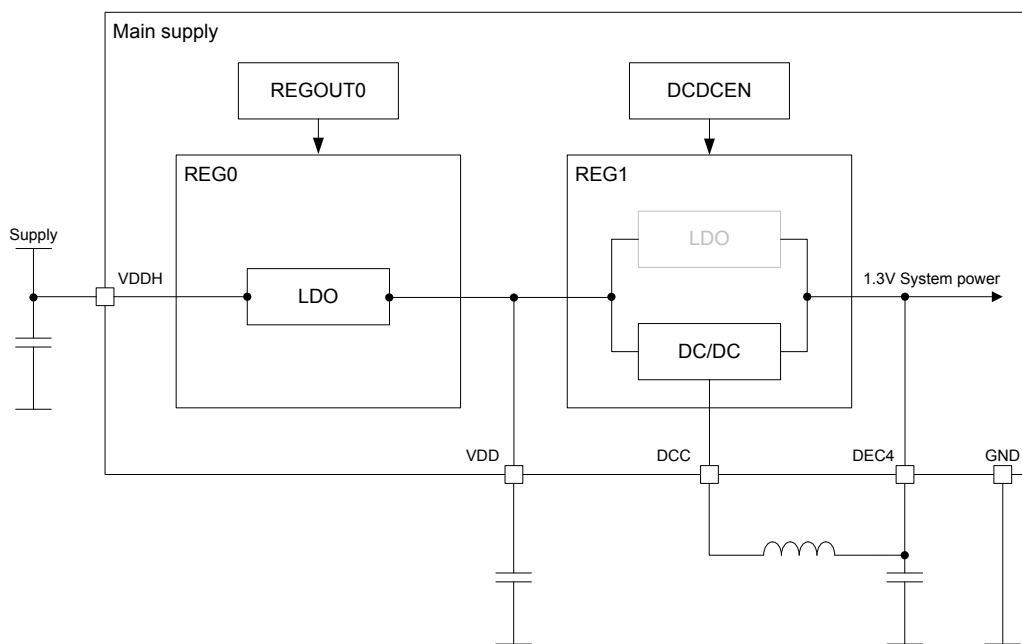


Figure 16: High Voltage mode, REG1 DC/DC

### 5.3.1.4 Power supply supervisor

The power supply supervisor enables monitoring of the connected power supply.

The power supply supervisor provides the following functionality:

- Power-on reset - signals the circuit when a supply is connected
- An optional power-fail comparator (POF) - signals the application when the supply voltages drop below a configured threshold
- A fixed brownout reset detector - holds the system in reset when the voltage is too low for safe operation

The power supply supervisor is illustrated in the following figure.

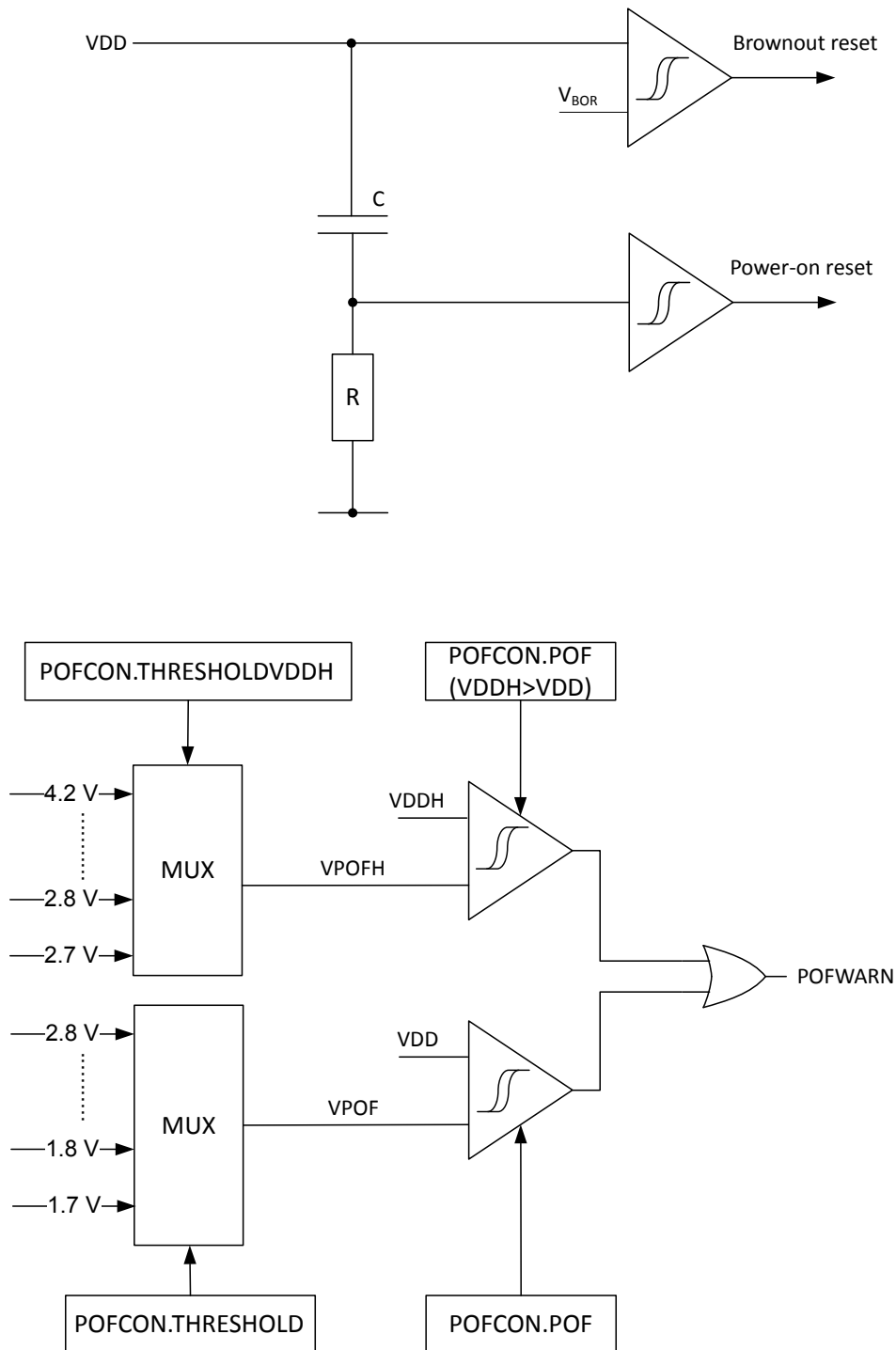


Figure 17: Power supply supervisor

### 5.3.1.5 Power-fail comparator

Using the power-fail comparator (POF) is optional. When enabled, it can provide an early warning to the CPU of an impending power supply failure.

To enable and configure the power-fail comparator, see the register [POFCON](#) on page 64.

When the supply voltage falls below the defined threshold, the power-fail comparator generates an event (POFWARN) that can be used by an application to prepare for power failure. This event is also generated when the supply voltage is already below the threshold at the time the power-fail comparator is enabled, or if the threshold is re-configured to a level above the supply voltage.

If the power failure warning is enabled, and the supply voltage is below the threshold, the power-fail comparator will prevent the **NVMC** from performing write operations to the flash.

The comparator features a hysteresis of  $V_{HYST}$ , as illustrated in the following figure.

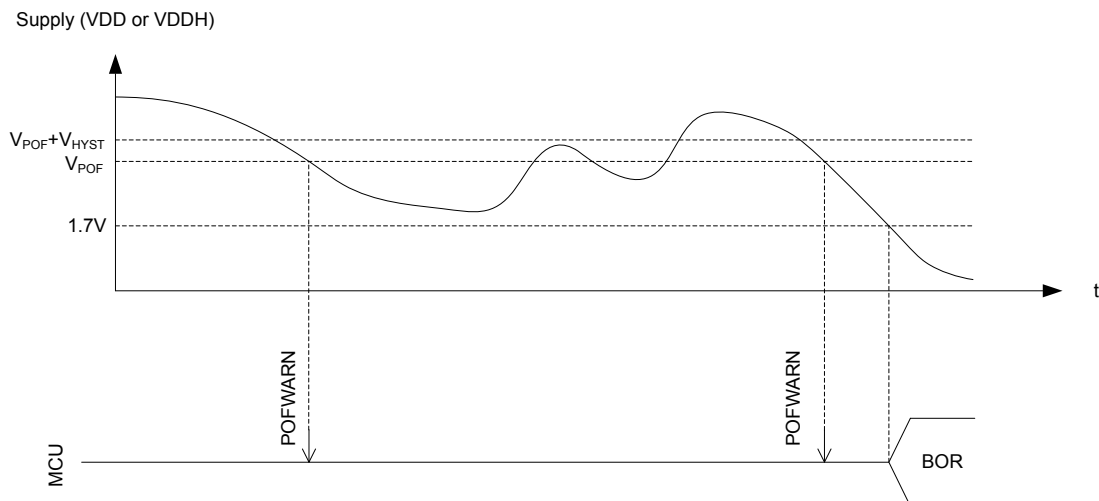


Figure 18: Power-fail comparator (BOR = brownout reset)

To save power, the power-fail comparator is not active in System OFF or System ON when HFCLK is not running.

### 5.3.2 USB supply

When using the USB peripheral, a 5 V USB supply needs to be provided to the VBUS pin.

The USB peripheral has a dedicated internal voltage regulator for converting the VBUS supply to 3.3 V used by the USB signalling interface (D+ and D- lines, and pull-up on D+). The remainder of the USB peripheral (USBDM) is supplied through the main supply like other on-chip features. As a consequence, VBUS and either VDDH or VDD supplies are required for USB peripheral operation.

When VBUS rises into its valid range, the software is notified through a USBDETECTED event. A USBREMOVED event is sent when VBUS goes below its valid range. Use these events to implement the USBDM start-up sequence described in the [USBDM](#) chapter.

When VBUS rises into its valid range while the device is in System OFF, the device resets and transitions to System ON mode. The [RESETREAS](#) register will have the VBUS bit set to indicate the source of the wake-up.

See [VBUS detection specifications](#) on page 69 for the levels at which the events are sent ( $V_{BUS,DETECT}$  and  $V_{BUS,REMOVE}$ ) or at which the system is woken up from System OFF ( $V_{BUS,DETECT}$ ).

When the USBDM peripheral is enabled through the [ENABLE](#) register, and VBUS is detected, the regulator is turned on. A USBPWRRDY event is sent when the regulator's worst case settling time has elapsed, indicating to the software that it can enable the USB pull-up to signal a USB connection to the host.

The software can read the state of the VBUS detection and regulator output readiness at any time through the [USBREGSTATUS](#) register.

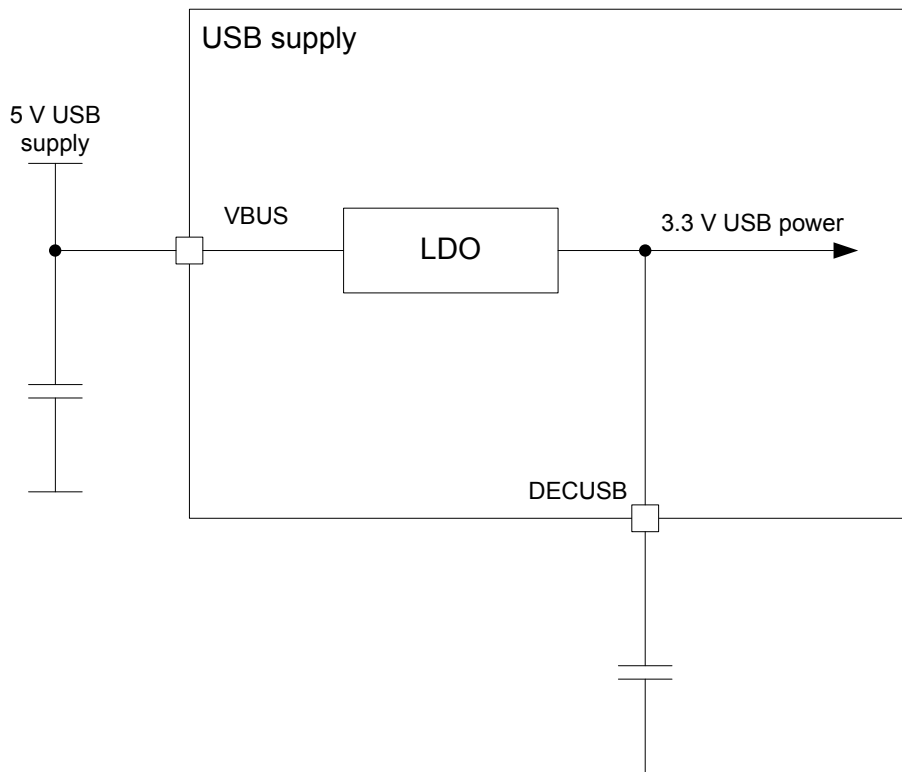


Figure 19: USB voltage regulator

To ensure stability, the input and output of the USB regulator need to be decoupled with a suitable decoupling capacitor. See [Reference circuitry](#) on page 418 for the recommended values.

### 5.3.3 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the register [SYSTEMOFF](#) on page 64. When in System OFF mode, the device can be woken up through one of the following signals:

- The DETECT signal, optionally generated by the GPIO peripheral.
- The ANADETECT signal, optionally generated by the LPCOMP module.
- Detecting a [valid USB voltage](#) on the VBUS pin ( $V_{BUS,DETECT}$ ).
- A reset.

The system is reset when it wakes up from System OFF mode.

One or more RAM sections can be retained in System OFF mode, depending on the settings in the `RAM[n].POWER` registers. `RAM[n].POWER` are retained registers. These registers are usually overwritten by the start-up code provided with the nRF application examples.

Before entering System OFF mode, all on-going EasyDMA transactions need to have completed. See peripheral specific chapters for more information about how to acquire the status of EasyDMA transactions.

#### 5.3.3.1 Emulated System OFF mode

If the device is in Debug Interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

Required resources needed for debugging include the following key components:

- [Debug](#) on page 40

- [CLOCK](#) — [Clock control](#) on page 69
- [POWER](#) — [Power supply](#) on page 49
- [NVMC](#) — [Non-volatile memory controller](#) on page 19
- [CPU](#) on page 14
- Flash memory
- RAM

See [Debug](#) on page 40 for more information.

Because the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.

### 5.3.4 System ON mode

System ON is the default state after power-on reset. In System ON mode, all functional blocks such as the CPU or peripherals can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register [RESETREAS](#) on page 62 provides information about the source causing the wakeup or reset.

The system can switch the appropriate internal power sources on and off, depending on the amount of power needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral fluctuates when specific tasks are triggered or events are generated.

#### 5.3.4.1 Sub-power modes

In System ON mode, when the CPU and all peripherals are in IDLE mode, the system can reside in one of the two sub-power modes.

The sub-power modes are:

- Constant Latency
- Low-power

In Constant Latency mode, the CPU wakeup latency and the PPI task response are constant and kept at a minimum. This is secured by forcing a set of basic resources to be turned on while in sleep. The cost of constant and predictable latency is increased power consumption. Constant Latency mode is selected by triggering the CONSTLAT task.

In Low-power mode, the automatic power management system described in [System ON mode](#) on page 56 ensures that the most efficient supply option is chosen to save power. The cost of having the lowest possible power consumption is a varying CPU wakeup latency and PPI task response. Low-power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it is by default in the sub-power mode Low-power.

### 5.3.5 RAM power control

The RAM power control registers are used for configuring the following:

- The RAM sections to be retained during System OFF
- The RAM sections to be retained and accessible during System ON

In System OFF, retention of a RAM section is configured in the RETENTION field of the corresponding register [RAM\[n\].POWER \(n=0..3\)](#) on page 66.

In System ON, retention and accessibility of a RAM section is configured in the RETENTION and POWER fields of the corresponding register [RAM\[n\].POWER \(n=0..3\)](#) on page 66.

The following table summarizes the behavior of these registers.



Configuration			RAM section status	
System on/off	RAM[n].POWER.POWER	RAM[n].POWER.RETENTION	Accessible	Retained
Off	x	Off	No	No
Off	x	On	No	Yes
On	Off	Off	No	No
On	Off <sup>3</sup>	On	No	Yes
On	On	x	Yes	Yes

Table 15: RAM section configuration

The advantage of not retaining RAM contents is that the overall current consumption is reduced.

See [Memory](#) on page 15 for more information on RAM sections.

## 5.3.6 Reset

Several sources may trigger a reset.

After a reset has occurred, register [RESETREAS](#) can be read to determine which source triggered the reset.

### 5.3.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

### 5.3.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via both registers [PSELRESET\[n\]](#) ( $n=0..1$ ) on page 35.

### 5.3.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The debug access port (DAP) is not reset following a wake up from System OFF mode if the device is in Debug Interface mode. See chapter [Debug](#) on page 40 for more information.

### 5.3.6.4 Soft reset

A soft reset is generated when the [SYSRESETREQ](#) bit of the application interrupt and reset control register (AIRCR) in the ARM<sup>®</sup> core is set.

See [ARM documentation](#) for more details.

A soft reset can also be generated via the register [RESET](#) on page 41 in the CTRL-AP.

### 5.3.6.5 Watchdog reset

A Watchdog reset is generated when the watchdog times out.

See chapter [WDT — Watchdog timer](#) on page 410 for more information.

### 5.3.6.6 Brownout reset

The brownout reset generator puts the system in a reset state if VDD drops below the brownout reset (BOR) threshold.

See section [Power fail comparator](#) on page 68 for more information.

<sup>3</sup> Not useful. RAM section power off gives negligible reduction in current consumption when retention is on.

### 5.3.6.7 Retained registers

A retained register is one that will retain its value in System OFF mode and through a reset, depending on the reset source. See the individual peripheral chapters for information on which of their registers are retained.

### 5.3.6.8 Reset behavior

The various reset sources and their targets are summarized in the table below.

Reset source	Reset target								
	CPU	Peripherals	GPIO	Debug <sup>4</sup>	SWJ-DP	RAM	WDT	Retained registers	RESETRAS
CPU lockup <sup>5</sup>	x	x	x						
Soft reset	x	x	x						
Wakeup from System OFF mode reset	x	x		x <sup>6</sup>		x <sup>7</sup>	x		
Watchdog reset <sup>8</sup>	x	x	x	x		x	x	x	
Pin reset	x	x	x	x		x	x	x	
Brownout reset	x	x	x	x	x	x	x	x	x
Power-on reset	x	x	x	x	x	x	x	x	x

**Note:** The RAM is never reset, but depending on a reset source the content of RAM may be corrupted.

## 5.3.7 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40000000	POWER	POWER	Power control	

Table 16: Instances

Register	Offset	Description
TASKS_CONSTLAT	0x78	Enable Constant Latency mode
TASKS_LOWPWR	0x7C	Enable Low-power mode (variable latency)
EVENTS_POFWARN	0x108	Power failure warning
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep
EVENTS_USBDTECTED	0x11C	Voltage supply detected on VBUS
EVENTS_USBREMOVED	0x120	Voltage supply removed from VBUS
EVENTS_USBPWRDY	0x124	USB 3.3 V supply ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

<sup>4</sup> All debug components excluding SWJ-DP. See [Debug](#) on page 40 for more information about the different debug components.

<sup>5</sup> Reset from CPU lockup is disabled if the device is in Debug Interface mode. CPU lockup is not possible in System OFF.

<sup>6</sup> The debug components will not be reset if the device is in Debug Interface mode.

<sup>7</sup> RAM is not reset on wakeup from System OFF mode. RAM, or certain parts of RAM, may not be retained after the device has entered System OFF mode, depending on the settings in the RAM registers.

<sup>8</sup> Watchdog reset is not available in System OFF.

Register	Offset	Description
RESETREAS	0x400	Reset reason
RAMSTATUS	0x428	RAM status register
USBREGSTATUS	0x438	USB supply status
SYSTEMOFF	0x500	System OFF register
POFCON	0x510	Power-fail comparator configuration
GPREGRET	0x51C	General purpose retention register
GPREGRET2	0x520	General purpose retention register
DCCEN	0x578	Enable DC/DC converter for REG1 stage
MAINREGSTATUS	0x640	Main supply status
RAM[0].POWER	0x900	RAM0 power control register
RAM[0].POWERSET	0x904	RAM0 power control set register
RAM[0].POWERCLR	0x908	RAM0 power control clear register
RAM[1].POWER	0x910	RAM1 power control register
RAM[1].POWERSET	0x914	RAM1 power control set register
RAM[1].POWERCLR	0x918	RAM1 power control clear register
RAM[2].POWER	0x920	RAM2 power control register
RAM[2].POWERSET	0x924	RAM2 power control set register
RAM[2].POWERCLR	0x928	RAM2 power control clear register
RAM[3].POWER	0x930	RAM3 power control register
RAM[3].POWERSET	0x934	RAM3 power control set register
RAM[3].POWERCLR	0x938	RAM3 power control clear register

Table 17: Register overview

### 5.3.7.1 TASKS\_CONSTLAT

Address offset: 0x78

Enable Constant Latency mode

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_CONSTLAT		Enable Constant Latency mode																											
		Trigger	1	Trigger task																											

### 5.3.7.2 TASKS\_LOWPWR

Address offset: 0x7C

Enable Low-power mode (variable latency)

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_LOWPWR		Enable Low-power mode (variable latency)																											
		Trigger	1	Trigger task																											

### 5.3.7.3 EVENTS\_POFWARN

Address offset: 0x108

Power failure warning

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_POFWARN		Power failure warning																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.4 EVENTS\_SLEEPENTER

Address offset: 0x114

CPU entered WFI/WFE sleep

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_SLEEPENTER		CPU entered WFI/WFE sleep																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.5 EVENTS\_SLEEPEXIT

Address offset: 0x118

CPU exited WFI/WFE sleep

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_SLEEPEXIT		CPU exited WFI/WFE sleep																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.6 EVENTS\_USBDTECTED

Address offset: 0x11C

Voltage supply detected on VBUS

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_USBDTECTED		Voltage supply detected on VBUS																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.7 EVENTS\_USBREMOVED

Address offset: 0x120

Voltage supply removed from VBUS

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_USBREMOVED			Voltage supply removed from VBUS																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.8 EVENTS\_USBPWRRDY

Address offset: 0x124

USB 3.3 V supply ready

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_USBPWRRDY			USB 3.3 V supply ready																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.3.7.9 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
ID																									F	E	D	C	B													A
Reset 0x00000000	0 0																																									
ID	Acce Field	Value ID	Value	Description																																						
A	RW POFWARN			Write '1' to enable interrupt for event <a href="#">POFWARN</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
B	RW SLEEPENTER			Write '1' to enable interrupt for event <a href="#">SLEEPENTER</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
C	RW SLEEPEXIT			Write '1' to enable interrupt for event <a href="#">SLEEPEXIT</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
D	RW USBDETECTED			Write '1' to enable interrupt for event <a href="#">USBDETECTED</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
E	RW USBREMOVED			Write '1' to enable interrupt for event <a href="#">USBREMOVED</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
F	RW USBPWRRDY			Write '1' to enable interrupt for event <a href="#">USBPWRRDY</a>																																						
		Set	1	Enable																																						
		Disabled	0	Read: Disabled																																						

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
ID																								F	E	D	C	B											A
Reset 0x00000000	0 0																																						
ID	Acce Field	Value ID	Value	Description																																			
		Enabled	1	Read: Enabled																																			

### 5.3.7.10 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
ID																								F	E	D	C	B											A
Reset 0x00000000	0 0																																						
ID	Acce Field	Value ID	Value	Description																																			
A	RW POFWARN			Write '1' to disable interrupt for event <a href="#">POFWARN</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
B	RW SLEEPENTER			Write '1' to disable interrupt for event <a href="#">SLEEPENTER</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
C	RW SLEEPEXIT			Write '1' to disable interrupt for event <a href="#">SLEEPEXIT</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
D	RW USBDETECTED			Write '1' to disable interrupt for event <a href="#">USBDETECTED</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
E	RW USBREMOVED			Write '1' to disable interrupt for event <a href="#">USBREMOVED</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
F	RW USBPWRRDY			Write '1' to disable interrupt for event <a href="#">USBPWRRDY</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			

### 5.3.7.11 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																					
ID																													I	G	E	D				C	B	A
Reset	0x00000000																																					
ID	Acce	Field	Value ID	Value	Description																																	
A	RW	RESETPIN			Reset from pin-reset detected																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
B	RW	DOG			Reset from watchdog detected																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
C	RW	SREQ			Reset from soft reset detected																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
D	RW	LOCKUP			Reset from CPU lock-up detected																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
E	RW	OFF			Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
G	RW	DIF			Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	
I	RW	VBUS			Reset due to wake up from System OFF mode by VBUS rising into valid range																																	
			NotDetected	0	Not detected																																	
			Detected	1	Detected																																	

### 5.3.7.12 RAMSTATUS ( Deprecated )

Address offset: 0x428

RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																													B	A	
Reset	0x00000000																														
ID	Acce	Field	Value ID	Value	Description																										
A-B	R	RAMBLOCK[i] (i=0..1)			RAM block i is on or off/powering up																										
			Off	0	Off																										
			On	1	On																										

### 5.3.7.13 USBREGSTATUS

Address offset: 0x438

USB supply status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce	Field	Value ID	Value	Description																											
A	R	VBUSDETECT			VBUS input detection status (USBDETECTED and USBREMOVED events are derived from this information)																											
			NoVbus	0	VBUS voltage below valid threshold																											
			VbusPresent	1	VBUS voltage above valid threshold																											
B	R	OUTPUTRDY			USB supply output settling time elapsed																											
			NotReady	0	USBREG output settling time not elapsed																											
			Ready	1	USBREG output settling time elapsed (same information as USBPWRDY event)																											

### 5.3.7.14 SYSTEMOFF

Address offset: 0x500

System OFF register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															A
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce	Field	Value ID	Value	Description																										
A	W	SYSTEMOFF			Enable System OFF mode																										
			Enter	1	Enable System OFF mode																										

### 5.3.7.15 POFCON

Address offset: 0x510

Power-fail comparator configuration

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																						
ID																									D	D	D	D							B	B	B	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																						
ID	Acce	Field	Value ID	Value	Description																																		
A	RW	POF			Enable or disable power failure warning																																		
			Disabled	0	Disable																																		
			Enabled	1	Enable																																		
B	RW	THRESHOLD			Power-fail comparator threshold setting. This setting applies both for normal voltage mode (supply connected to both VDD and VDDH) and high voltage mode (supply connected to VDDH only). Values 0-3 set threshold below 1.7 V and should not be used as brown out detection will be activated before power failure warning on such low voltages.																																		
			V17	4	Set threshold to 1.7 V																																		
			V18	5	Set threshold to 1.8 V																																		
			V19	6	Set threshold to 1.9 V																																		
			V20	7	Set threshold to 2.0 V																																		
			V21	8	Set threshold to 2.1 V																																		
			V22	9	Set threshold to 2.2 V																																		
			V23	10	Set threshold to 2.3 V																																		
			V24	11	Set threshold to 2.4 V																																		
			V25	12	Set threshold to 2.5 V																																		
			V26	13	Set threshold to 2.6 V																																		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																								
ID																													D	D	D	D					B	B	B	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																								
ID	Acce Field	Value ID	Value	Description																																					
		V27	14	Set threshold to 2.7 V																																					
		V28	15	Set threshold to 2.8 V																																					
D	RW	THRESHOLDVDDH		Power-fail comparator threshold setting for high voltage mode (supply connected to VDDH only). This setting does not apply for normal voltage mode (supply connected to both VDD and VDDH).																																					
		V27	0	Set threshold to 2.7 V																																					
		V28	1	Set threshold to 2.8 V																																					
		V29	2	Set threshold to 2.9 V																																					
		V30	3	Set threshold to 3.0 V																																					
		V31	4	Set threshold to 3.1 V																																					
		V32	5	Set threshold to 3.2 V																																					
		V33	6	Set threshold to 3.3 V																																					
		V34	7	Set threshold to 3.4 V																																					
		V35	8	Set threshold to 3.5 V																																					
		V36	9	Set threshold to 3.6 V																																					
		V37	10	Set threshold to 3.7 V																																					
		V38	11	Set threshold to 3.8 V																																					
		V39	12	Set threshold to 3.9 V																																					
		V40	13	Set threshold to 4.0 V																																					
		V41	14	Set threshold to 4.1 V																																					
		V42	15	Set threshold to 4.2 V																																					

### 5.3.7.16 GPREGRET

Address offset: 0x51C

General purpose retention register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																													A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW	GPREGRET		General purpose retention register																																
				This register is a retained register																																

### 5.3.7.17 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																													A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW	GPREGRET		General purpose retention register																																
				This register is a retained register																																

### 5.3.7.18 DCDCEN

Address offset: 0x578

Enable DC/DC converter for REG1 stage

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	DCDCEN			Enable DC/DC converter for REG1 stage.																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										

### 5.3.7.19 MAINREGSTATUS

Address offset: 0x640

Main supply status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	R	MAINREGSTATUS			Main supply status																										
			Normal	0	Normal voltage mode. Voltage supplied on VDD.																										
			High	1	High voltage mode. Voltage supplied on VDDH.																										

### 5.3.7.20 RAM[n].POWER (n=0..3)

Address offset: 0x900 + (n × 0x10)

RAMn power control register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	D C																B A														
Reset 0x0000FFFF	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A-B	RW	S[i]POWER (i=0..1)			Keep RAM section Si on or off in System ON mode.																										
			Off	0	Off																										
			On	1	On																										
C-D	RW	S[i]RETENTION (i=0..1)			Keep retention on RAM section Si when RAM section is off																										
			Off	0	Off																										
			On	1	On																										

### 5.3.7.21 RAM[n].POWERSET (n=0..3)

Address offset: 0x904 + (n × 0x10)

RAMn power control set register

When read, this register will return the value of the POWER register.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	D C																												B A		
Reset 0x0000FFFF	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																														
ID	Acce Field	Value ID	Value	Description																											
A-B	W S[i]POWER (i=0..1)	On	1	Keep RAM section Si of RAMn on or off in System ON mode On																											
C-D	W S[i]RETENTION (i=0..1)	On	1	Keep retention on RAM section Si when RAM section is switched off On																											

### 5.3.7.22 RAM[n].POWERCLR (n=0..3)

Address offset: 0x908 + (n × 0x10)

RAMn power control clear register

When read, this register will return the value of the POWER register.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	D C																												B A		
Reset 0x0000FFFF	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																														
ID	Acce Field	Value ID	Value	Description																											
A-B	W S[i]POWER (i=0..1)	Off	1	Keep RAM section Si of RAMn on or off in System ON mode Off																											
C-D	W S[i]RETENTION (i=0..1)	Off	1	Keep retention on RAM section Si when RAM section is switched off Off																											

## 5.3.8 Electrical specification

### 5.3.8.1 Regulator operating conditions

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>DD,POR</sub>	VDD supply voltage needed during power-on reset	1.75			V
V <sub>DD</sub>	Normal voltage mode operating voltage	1.7	3.0	3.6	V
V <sub>DDH</sub>	High voltage mode operating voltage	2.5	3.7	5.5	V
C <sub>VDD</sub>	Effective decoupling capacitance on the VDD pin	2.7	4.7	5.5	μF
C <sub>DEC4</sub>	Effective decoupling capacitance on the DEC4 pin	0.7	1	1.3	μF

### 5.3.8.2 Regulator specifications, REG0 stage

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>REGOUT</sub>	REG0 output voltage	1.8		3.3	V
V <sub>REGOUT,ERR</sub>	REG0 output voltage error (deviation from setting in <a href="#">REGOUT0</a> on page 36)	-10		5	%
V <sub>REGOUT,ERR,EXT</sub>	REG0 output voltage error (deviation from setting in <a href="#">REGOUT0</a> on page 36), extended temperature range	-10		7	%
V <sub>VDDH-VDD</sub>	Required difference between input voltage (VDDH) and output voltage (VDD, configured in <a href="#">REGOUT0</a> on page 36), VDDH > VDD	0.3			V

### 5.3.8.3 Device startup times

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>POR</sub>	Time in power-on reset after supply reaches minimum operating voltage, depending on supply rise time				
t <sub>POR,10μs</sub>	VDD rise time 10 μs <sup>9</sup>		1	10	ms
t <sub>POR,10ms</sub>	VDD rise time 10 ms <sup>9</sup>		9		ms
t <sub>POR,60ms</sub>	VDD rise time 60 ms <sup>9</sup>		23	110	ms
t <sub>RISE,REG0OUT</sub>	REG0 output (VDD) rise time after VDDH reaches minimum VDDH supply voltage <sup>9</sup>				
t <sub>RISE,REG0OUT,10μs</sub>	VDDH rise time 10 μs <sup>9</sup>		0.22	1.55	ms
t <sub>RISE,REG0OUT,10ms</sub>	VDDH rise time 10 ms <sup>9</sup>		5		ms
t <sub>RISE,REG0OUT,100ms</sub>	VDDH rise time 100 ms <sup>9</sup>	30	50	80	ms
t <sub>PINR</sub>	Reset time when using pin reset, depending on pin capacitance				
t <sub>PINR,500nF</sub>	500 nF capacitance at reset pin			32.5	ms
t <sub>PINR,10μF</sub>	10 μF capacitance at reset pin			650	ms
t <sub>R2ON</sub>	Time from power-on reset to System ON				
t <sub>R2ON,NOTCONF</sub>	If reset pin not configured	t <sub>POR</sub>			ms
t <sub>R2ON,CONF</sub>	If reset pin configured	t <sub>POR</sub> + t <sub>PINR</sub>			ms
t <sub>OFF2ON</sub>	Time from OFF to CPU execute		16.5		μs
t <sub>IDLE2CPU</sub>	Time from IDLE to CPU execute		3.0		μs
t <sub>EVTSET,CL1</sub>	Time from HW event to PPI event in Constant Latency System ON mode		0.0625		μs
t <sub>EVTSET,CL0</sub>	Time from HW event to PPI event in Low Power System ON mode		0.0625		μs

### 5.3.8.4 Power fail comparator

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>POF,NV</sub>	Nominal power level warning thresholds (falling supply voltage) in Normal voltage mode (supply on VDD). Levels are configurable between Min. and Max. in 100 mV increments	1.7		2.8	V
V <sub>POF,HV</sub>	Nominal power level warning thresholds (falling supply voltage) in High voltage mode (supply on VDDH). Levels are configurable in 100 mV increments	2.7		4.2	V
V <sub>POFTOL</sub>	Threshold voltage tolerance (applies in both Normal voltage mode and High voltage mode)	-5		5	%
V <sub>POFHYST</sub>	Threshold voltage hysteresis (applies in both Normal voltage mode and High voltage mode)	40	50	60	mV
V <sub>BOR,OFF</sub>	Brownout reset voltage range System OFF mode. Brownout only applies to the voltage on VDD	1.2		1.62	V
V <sub>BOR,ON</sub>	Brownout reset voltage range System ON mode. Brownout only applies to the voltage on VDD	1.57	1.6	1.63	V

<sup>9</sup> See Recommended operating conditions on page 430 for more information.

### 5.3.8.5 USB operating conditions

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>BUS</sub>	Supply voltage on VBUS pin	4.35	5	5.5	V
V <sub>DPDM</sub>	Voltage on D+ and D- lines	V <sub>SS</sub> - 0.3		V <sub>USB33</sub> + 0.3	V

### 5.3.8.6 USB regulator specifications

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>USB,QUIES</sub>	USB regulator quiescent current drawn from VBUS (USB <sub>D</sub> enabled)		170		μA
t <sub>USBPWRRDY</sub>	Time from USB enabled to USBPWRRDY event triggered, V <sub>BUS</sub> supply provided		1		ms
V <sub>USB33</sub>	On voltage at the USB regulator output (DECUSB pin)	3.0	3.3	3.6	V
R <sub>SOURCE,VBUS</sub>	Maximum source resistance on VBUS, including cable			2	Ω
C <sub>DECUSB</sub>	Decoupling capacitor on the DECUSB pin	2.35	4.7	5.5	μF

### 5.3.8.7 VBUS detection specifications

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>BUS,DETECT</sub>	Voltage at which rising VBUS gets reported by USBDETECTED	3.4	4.0	4.3	V
V <sub>BUS,REMOVE</sub>	Voltage at which decreasing VBUS gets reported by USBREMOVED	3.0	3.6	3.9	V

## 5.4 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-500 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of crystal oscillator activity for low latency start up
- Automatic internal oscillator and clock control, and distribution for ultra-low power

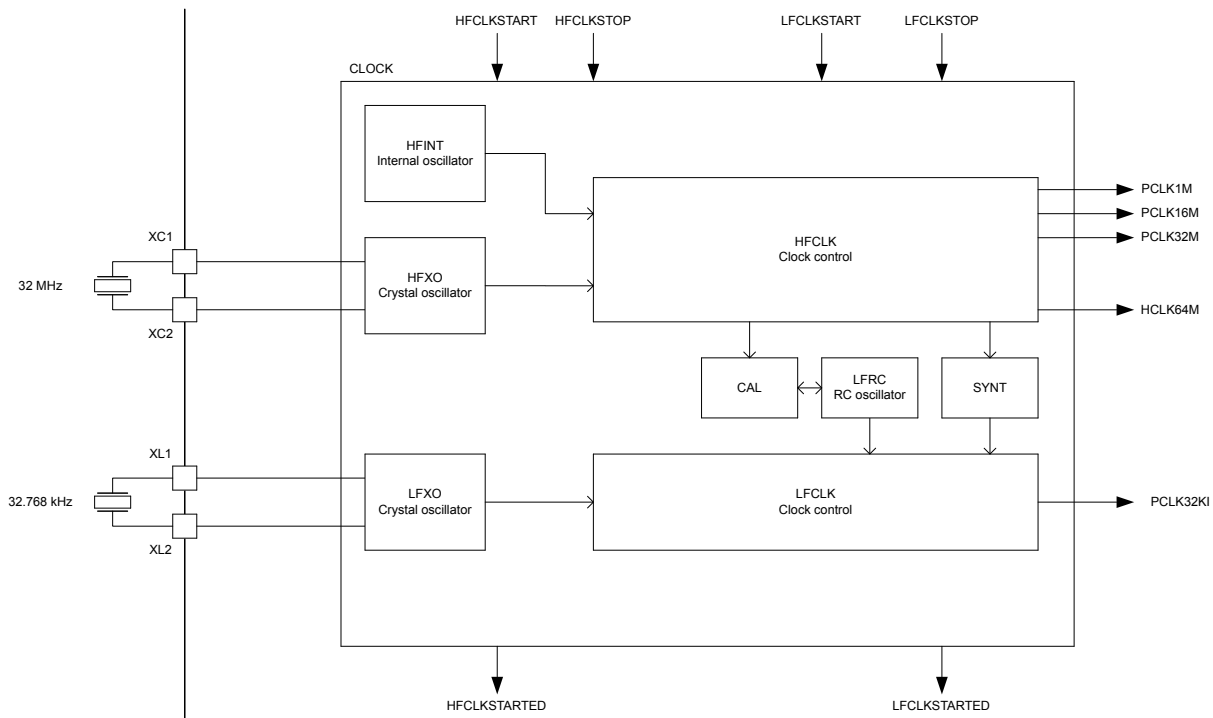


Figure 20: Clock control

### 5.4.1 HFCLK controller

The HFCLK controller provides several clock signals in the system.

These are as follows:

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller uses the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see [Clock control](#) on page 70.

The HFCLK controller will automatically provide the clock(s) requested by the system. If the system does not request any clocks from the HFCLK controller, the controller will enter a power saving mode.

The HFINT source will be used when HFCLK is requested and HFXO has not been started.

The HFXO is started by triggering the HFCLKSTART task and stopped by triggering the HFCLKSTOP task. When the HFCLKSTART task is triggered, the HFCLKSTARTED event is generated once the HFXO startup time has elapsed. The HFXO startup time is given as the sum of the following:

- HFXO power-up time, as specified in [64 MHz crystal oscillator \(HFXO\)](#) on page 82.
- HFXO debounce time, as specified in register [HFNODEBOUNCE](#) on page 81.

The HFXO must be running to use the RADIO or the calibration mechanism associated with the 32.768 kHz RC oscillator.

### 5.4.1.1 64 MHz crystal oscillator (HF XO)

The 64 MHz crystal oscillator (HF XO) is controlled by a 32 MHz external crystal.

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

[Circuit diagram of the 64 MHz crystal oscillator](#) on page 71 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

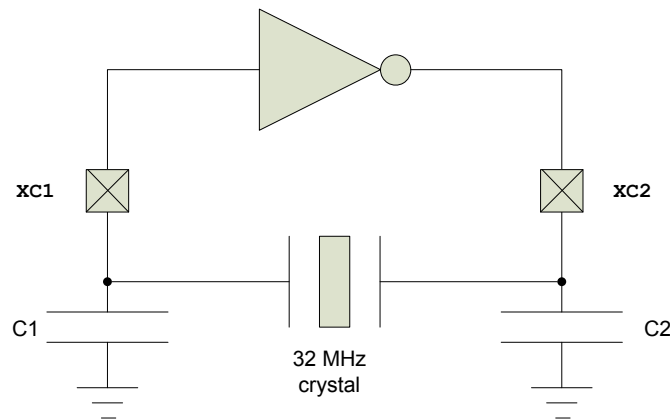


Figure 21: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see [Reference circuitry](#) on page 418.  $C_{pcb1}$  and  $C_{pcb2}$  are stray capacitances on the PCB.  $C_{pin}$  is the pin input capacitance on the XC1 and XC2 pins. See [table 64 MHz crystal oscillator \(HF XO\)](#) on page 82. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in [table 64 MHz crystal oscillator \(HF XO\)](#) on page 82. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.

### 5.4.2 LFCLK controller

The system supports several low frequency clock sources.

As illustrated in [Clock control](#) on page 70, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LF XO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK controller and all of the LFCLK clock sources are always switched off when in System OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in register [LFCLKSRC](#) on page 81 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The register [LFXODEBOUNCE](#) on page 81 is used to configure the LFXO debounce time. The register must be modified if operating in the Extended Operating Conditions temperature range, see [Recommended operating conditions](#) on page 430. The LFXO start up time will be increased as a result.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

Register [LFCLKSRC](#) on page 81 controls the clock source, and its allowed swing. The truth table for various situations is as follows:

SRC	EXTERNAL	BYPASS	Comment
0	0	0	Normal operation, LFRC is source
0	0	1	DO NOT USE
0	1	X	DO NOT USE
1	0	0	Normal XTAL operation
1	1	0	Apply external low swing signal to XL1, ground XL2
1	1	1	Apply external full swing signal to XL1, leave XL2 grounded or unconnected
1	0	1	DO NOT USE
2	0	0	Normal operation, LFSYNT is source
2	0	1	DO NOT USE
2	1	X	DO NOT USE

Table 18: LFCLKSRC configuration depending on clock source

It is not allowed to write to register [LFCLKSRC](#) on page 81 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register [LFCLKSTAT](#) on page 80 indicates LFCLK running state.

The synthesized 32.768 kHz clock depends on the HFCLK to run. If high accuracy is required for the LFCLK running off the synthesized 32.768 kHz clock, the HFCLK must running from the HFXO source.

#### 5.4.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC oscillator does not require additional external components.

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration.

#### 5.4.2.2 Calibrating the 32.768 kHz RC oscillator

After the LFRC oscillator is started and running, it can be calibrated by triggering the CAL task.

The LFRC oscillator will then temporarily request the HFCLK to be used as a reference for the calibration. A DONE event will be generated when calibration has finished. The HFCLK crystal oscillator has to be started (by triggering the HFCLKSTART task) in order for the calibration mechanism to work.

It is not allowed to stop the LFRC during an ongoing calibration.

#### 5.4.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in [CTIV \(Retained\)](#) on page



82 and generate a CTTO event when it reaches 0. The calibration timer will automatically stop when it reaches 0.

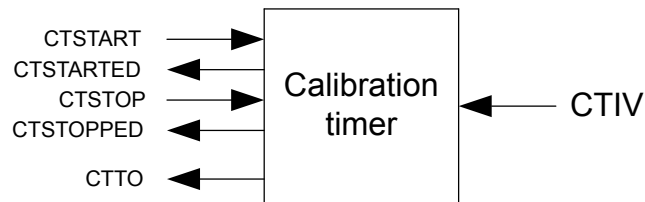


Figure 22: Calibration timer

After a CTSTART task has been triggered, the calibration timer will ignore further tasks until it has returned the CTSTARTED event. Likewise, after a CTSTOP task has been triggered, the calibration timer will ignore further tasks until it has returned a CTSTOPPED event. Triggering CTSTART while the calibration timer is running will immediately return a CTSTARTED event. Triggering CTSTOP when the calibration timer is stopped will immediately return a CTSTOPPED event.

#### 5.4.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 500 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the XL1 pin. The XL2 pin shall then be grounded.
- Rail-to-rail clock signal applied to the XL1 pin. The XL2 pin shall then be grounded or left unconnected.

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. [Circuit diagram of the 32.768 kHz crystal oscillator](#) on page 73 shows the LFXO circuitry.

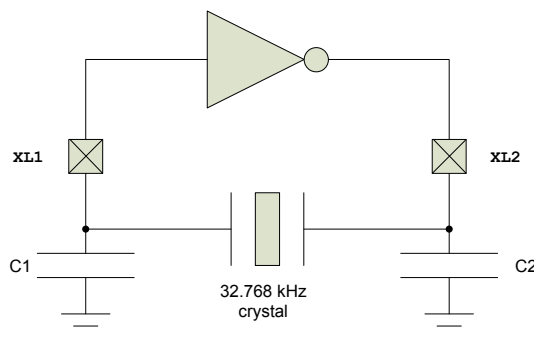


Figure 23: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground.  $C_{pcb1}$  and  $C_{pcb2}$  are stray capacitances on the PCB.  $C_{pin}$  is the pin input capacitance on the XC1 and XC2 pins (see [Low frequency crystal oscillator \(LFXO\)](#) on page 83). The load capacitors C1 and C2 should have the same value.

For more information, see [Reference circuitry](#) on page 418.

### 5.4.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

## 5.4.3 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40000000	CLOCK	CLOCK	Clock control	

Table 19: Instances

Register	Offset	Description	
TASKS_HFCLKSTART	0x000	Start HFXO crystal oscillator	
TASKS_HFCLKSTOP	0x004	Stop HFXO crystal oscillator	
TASKS_LFCLKSTART	0x008	Start LFCLK	
TASKS_LFCLKSTOP	0x00C	Stop LFCLK	
TASKS_CAL	0x010	Start calibration of LFRC	
TASKS_CTSTART	0x014	Start calibration timer	
TASKS_CTSTOP	0x018	Stop calibration timer	
EVENTS_HFCLKSTARTED	0x100	HFXO crystal oscillator started	
EVENTS_LFCLKSTARTED	0x104	LFCLK started	
EVENTS_DONE	0x10C	Calibration of LFRC completed	
EVENTS_CTTO	0x110	Calibration timer timeout	
EVENTS_CTSTARTED	0x128	Calibration timer has been started and is ready to process new tasks	
EVENTS_CTSTOPPED	0x12C	Calibration timer has been stopped and is ready to process new tasks	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered	
HFCLKSTAT	0x40C	HFCLK status	
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered	
LFCLKSTAT	0x418	LFCLK status	
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered	
LFCLKSRC	0x518	Clock source for the LFCLK	
HFXODEBOUNCE	0x528	HFXO debounce time. The HFXO is started by triggering the TASKS_HFCLKSTART task.	
LFXODEBOUNCE	0x52C	LFXO debounce time. The LFXO is started by triggering the TASKS_LFCLKSTART task when the LFCLKSRC register is configured for Xtal.	
CTIV	0x538	Calibration timer interval	Retained

Table 20: Register overview

### 5.4.3.1 TASKS\_HFCLKSTART

Address offset: 0x000

Start HFXO crystal oscillator

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																												
A	W	TASKS_HFCLKSTART	Trigger	1	Start HFXO crystal oscillator Trigger task																												

### 5.4.3.2 TASKS\_HFCLKSTOP

Address offset: 0x004

Stop HFXO crystal oscillator

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_HFCLKSTOP	Trigger	1	Stop HFXO crystal oscillator Trigger task																											

### 5.4.3.3 TASKS\_LFCLKSTART

Address offset: 0x008

Start LFCLK

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_LFCLKSTART	Trigger	1	Start LFCLK Trigger task																											

### 5.4.3.4 TASKS\_LFCLKSTOP

Address offset: 0x00C

Stop LFCLK

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_LFCLKSTOP	Trigger	1	Stop LFCLK Trigger task																											

### 5.4.3.5 TASKS\_CAL

Address offset: 0x010

Start calibration of LFRC

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CAL	Trigger	1	Start calibration of LFRC Trigger task																												

### 5.4.3.6 TASKS\_CTSTART

Address offset: 0x014

Start calibration timer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CTSTART	Trigger	1	Start calibration timer Trigger task																												

### 5.4.3.7 TASKS\_CTSTOP

Address offset: 0x018

Stop calibration timer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CTSTOP	Trigger	1	Stop calibration timer Trigger task																												

### 5.4.3.8 EVENTS\_HFCLKSTARTED

Address offset: 0x100

HF XO crystal oscillator started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_HFCLKSTARTED	NotGenerated	0	HF XO crystal oscillator started Event not generated																												
		Generated	1	Event generated																												

### 5.4.3.9 EVENTS\_LFCLKSTARTED

Address offset: 0x104

LFCLK started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	RW	EVENTS_LFCLKSTARTED		LFCLK started																													
		NotGenerated	0	Event not generated																													
		Generated	1	Event generated																													

### 5.4.3.10 EVENTS\_DONE

Address offset: 0x10C

Calibration of LFRC completed

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_DONE		Calibration of LFRC completed																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.4.3.11 EVENTS\_CTTO

Address offset: 0x110

Calibration timer timeout

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_CTTO		Calibration timer timeout																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.4.3.12 EVENTS\_CTSTARTED

Address offset: 0x128

Calibration timer has been started and is ready to process new tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_CTSTARTED		Calibration timer has been started and is ready to process new tasks																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 5.4.3.13 EVENTS\_CTSTOPPED

Address offset: 0x12C

Calibration timer has been stopped and is ready to process new tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																												
A	RW	EVENTS_CTSTOPPED			Calibration timer has been stopped and is ready to process new tasks																												
			NotGenerated	0	Event not generated																												
			Generated	1	Event generated																												

### 5.4.3.14 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					F	E							D	C	B	A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	HFCLKSTARTED			Write '1' to enable interrupt for event <a href="#">HFCLKSTARTED</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
B	RW	LFCLKSTARTED			Write '1' to enable interrupt for event <a href="#">LFCLKSTARTED</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
C	RW	DONE			Write '1' to enable interrupt for event <a href="#">DONE</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
D	RW	CTTO			Write '1' to enable interrupt for event <a href="#">CTTO</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
E	RW	CTSTARTED			Write '1' to enable interrupt for event <a href="#">CTSTARTED</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
F	RW	CTSTOPPED			Write '1' to enable interrupt for event <a href="#">CTSTOPPED</a>																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											

### 5.4.3.15 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					F	E							D	C	B	A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	HFCLKSTARTED			Write '1' to disable interrupt for event <a href="#">HFCLKSTARTED</a>																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																						
ID																															F	E				D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																						
ID	Acce Field	Value ID	Value	Description																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
<b>B</b>	<b>RW LFCLKSTARTED</b>			Write '1' to disable interrupt for event <b>LFCLKSTARTED</b>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
<b>C</b>	<b>RW DONE</b>			Write '1' to disable interrupt for event <b>DONE</b>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
<b>D</b>	<b>RW CTTO</b>			Write '1' to disable interrupt for event <b>CTTO</b>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
<b>E</b>	<b>RW CTSTARTED</b>			Write '1' to disable interrupt for event <b>CTSTARTED</b>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
<b>F</b>	<b>RW CTSTOPPED</b>			Write '1' to disable interrupt for event <b>CTSTOPPED</b>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			

### 5.4.3.16 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															A
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
<b>A</b>	<b>R STATUS</b>			HFCLKSTART task triggered or not																											
		NotTriggered	0	Task not triggered																											
		Triggered	1	Task triggered																											

### 5.4.3.17 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID		B																														A	
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	R	SRC		Source of HFCLK																													
			RC	0	64 MHz internal oscillator (HFINT)																												
			Xtal	1	64 MHz crystal oscillator (HF XO)																												
B	R	STATE		HFCLK state																													
			NotRunning	0	HFCLK not running																												
			Running	1	HFCLK running																												

### 5.4.3.18 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID		B																														A	
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	R	STATUS		LFCLKSTART task triggered or not																													
			NotTriggered	0	Task not triggered																												
			Triggered	1	Task triggered																												

### 5.4.3.19 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID		B																														A A	
Reset 0x00000000		0 0																															
ID	Acce Field	Value ID	Value	Description																													
A	R	SRC		Source of LFCLK																													
			RC	0	32.768 kHz RC oscillator (LFRC)																												
			Xtal	1	32.768 kHz crystal oscillator (LF XO)																												
			Synth	2	32.768 kHz synthesized from HFCLK (LFSYNT)																												
B	R	STATE		LFCLK state																													
			NotRunning	0	LFCLK not running																												
			Running	1	LFCLK running																												

### 5.4.3.20 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered





LFXO debounce time. The LFXO is started by triggering the TASKS\_LFCLKSTART task when the LFCLKSRC register is configured for Xtal.

The EVENTS\_LFCLKSTARTED event is generated after the LFXO debounce time has elapsed. It is not allowed to change the value of this register while the LFXO is starting.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	LFXODEBOUNCE		LFXO debounce time.																											
		Normal	0	8192 32.768 kHz periods, or 0.25 s. Recommended for normal Operating Temperature conditions.																											
		Extended	1	16384 32.768 kHz periods, or 0.5 s. Recommended for Extended Operating Temperature conditions.																											

### 5.4.3.24 CTIV ( Retained )

Address offset: 0x538

This register is a retained register

Calibration timer interval

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A A A A A A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	CTIV		Calibration timer interval in multiple of 0.25 seconds. Range: 0.25 seconds to 31.75 seconds.																											

## 5.4.4 Electrical specification

### 5.4.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_HFINT}}$	Nominal output frequency		64		MHz
$f_{\text{TOL\_HFINT}}$	Frequency tolerance		$\pm 1.5$	$\pm 8$	%
$f_{\text{TOL\_HFINT,EXT}}$	Frequency tolerance, extended temperature range			$\pm 9$	%

### 5.4.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_HFXO}}$	Nominal output frequency		64		MHz
$f_{\text{XTAL\_HFXO}}$	External crystal frequency		32		MHz
$f_{\text{TOL\_HFXO}}$	Frequency tolerance requirement for 2.4 GHz proprietary radio applications			$\pm 60$	ppm
$f_{\text{TOL\_HFXO\_BLE}}$	Frequency tolerance requirement, Bluetooth low energy applications, packet length $\leq 200$ bytes			$\pm 40$	ppm
$f_{\text{TOL\_HFXO\_BLE\_LP}}$	Frequency tolerance requirement, Bluetooth low energy applications, packet length $> 200$ bytes			$\pm 30$	ppm
$C_{\text{L\_HFXO}}$	Load capacitance			12	pF

Symbol	Description	Min.	Typ.	Max.	Units
C <sub>0_HFXO</sub>	Shunt capacitance			7	pF
R <sub>S_HFXO_7PF</sub>	Equivalent series resistance 3 pF < C <sub>0</sub> ≤ 7 pF			60	Ω
R <sub>S_HFXO_3PF</sub>	Equivalent series resistance C <sub>0</sub> ≤ 3 pF			100	Ω
P <sub>D_HFXO</sub>	Drive level			100	μW
C <sub>PIN_HFXO</sub>	Input capacitance XC1 and XC2		3		pF
I <sub>STBY_X32M</sub>	Core standby current for various crystals				
I <sub>STBY_X32M_X0</sub>	Typical parameters for a given 2.5mm x 2.0mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 1 pF, LM_HFXO = 7 mH, RS_HFXO = 20 Ω		65		μA
I <sub>STBY_X32M_X1</sub>	Typical parameters for a given 1.6mm x 1.2mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 0.4 pF, LM_HFXO = 20 mH, RS_HFXO = 40 Ω		110		μA
I <sub>START_X32M</sub>	Average startup current for various crystals, first 1 ms				
I <sub>START_X32M_X0</sub>	Typical parameters for a given 2.5mm x 2.0mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 1 pF, LM_HFXO = 7 mH, RS_HFXO = 20 Ω		360		μA
I <sub>START_X32M_X1</sub>	Typical parameters for a given 1.6mm x 1.2mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 0.4 pF, LM_HFXO = 20 mH, RS_HFXO = 40 Ω		785		μA
t <sub>POWERUP_X32M</sub>	Power-up time for various crystals				
t <sub>POWERUP_X32M_X0</sub>	Typical parameters for a given 2.5mm x 2.0mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 1 pF, LM_HFXO = 7 mH, RS_HFXO = 20 Ω		60		μs
t <sub>POWERUP_X32M_X1</sub>	Typical parameters for a given 1.6mm x 1.2mm crystal:  CL_HFXO = 8 pF, C <sub>0_HFXO</sub> = 0.4 pF, LM_HFXO = 20 mH, RS_HFXO = 40 Ω		200		μs

### 5.4.4.3 Low frequency crystal oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f <sub>NOM_LFXO</sub>	Crystal frequency		32.768		kHz
f <sub>TOL_LFXO_BLE</sub>	Frequency tolerance requirement for BLE stack			±500	ppm
f <sub>TOL_LFXO_ANT</sub>	Frequency tolerance requirement for ANT stack			±50	ppm
C <sub>L_LFXO</sub>	Load capacitance			12.5	pF
C <sub>0_LFXO</sub>	Shunt capacitance			2	pF
R <sub>S_LFXO</sub>	Equivalent series resistance			100	kΩ
P <sub>D_LFXO</sub>	Drive level			0.5	μW
C <sub>pin</sub>	Input capacitance on XL1 and XL2 pads		4		pF
I <sub>LFXO</sub>	Run current for 32.768 kHz crystal oscillator		0.23		μA
t <sub>START_LFXO</sub>	Startup time for 32.768 kHz crystal oscillator		0.25		s
t <sub>START_LFXO_EXT</sub>	Startup time for 32.768 kHz crystal oscillator when CLOCK.LFXODEBOUNCE configured for Extended debounce time		0.5		s

### 5.4.4.4 Low frequency RC oscillator (LFRC)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_LFRC}}$	Nominal frequency		32.768		kHz
$f_{\text{TOL\_LFRC}}$	Frequency tolerance, uncalibrated			±5	%
$f_{\text{TOL\_CAL\_LFRC}}$	Frequency tolerance after calibration <sup>10</sup>			±500	ppm
$I_{\text{LFRC}}$	Run current		0.7		μA
$t_{\text{START\_LFRC}}$	Startup time		1000		μs

#### 5.4.4.5 Synthesized low frequency clock (LFSYNT)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_LFSYNT}}$	Nominal frequency		32.768		kHz

<sup>10</sup> Constant temperature within ±0.5 °C, calibration performed at least every 8 seconds, averaging interval > 7.5 ms, defined as 3 sigma

# 6 Peripherals

## 6.1 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

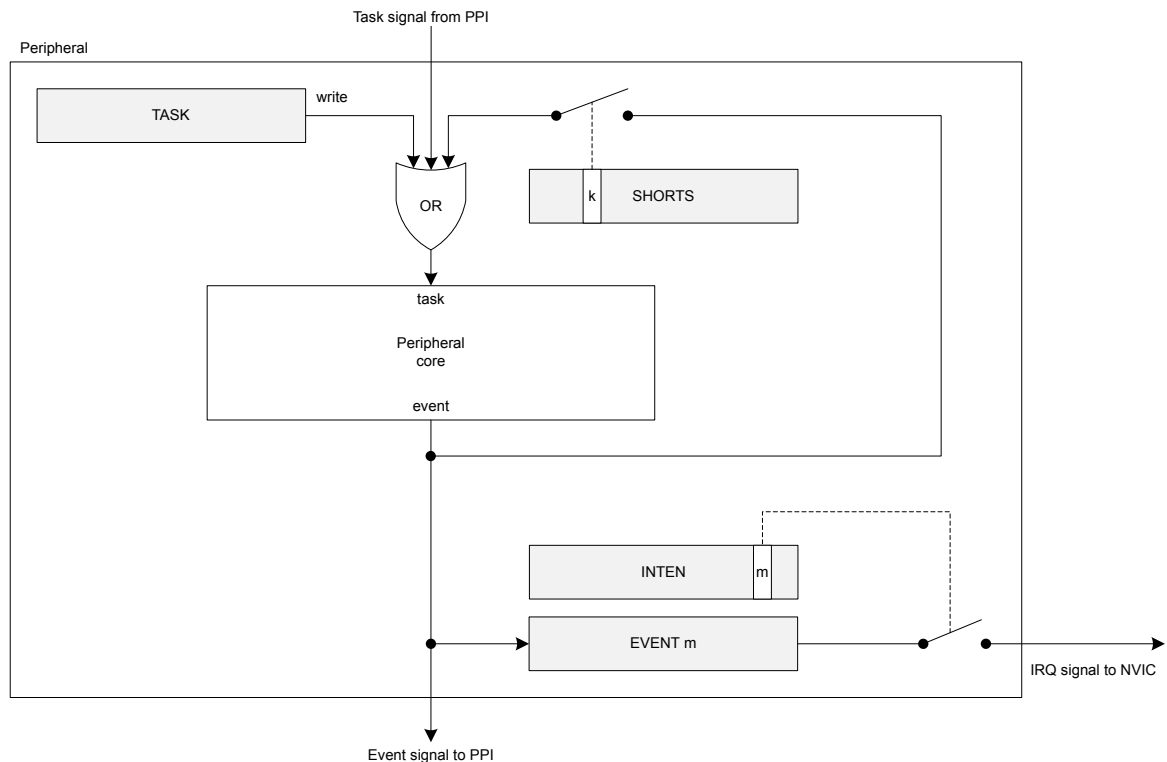


Figure 24: Tasks, events, shortcuts, and interrupts

### 6.1.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See [Instantiation](#) on page 18 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

## 6.1.2 Peripherals with shared ID

In general (with the exception of ID 0), peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one peripheral at the time on this specific ID.

When switching between two peripherals sharing an ID, the user should do the following to prevent unwanted behavior:

1. Disable the previously used peripheral.
2. Remove any programmable peripheral interconnect (PPI) connections set up for the peripheral that is being disabled.
3. Clear all bits in the INTEN register, i.e. `INTENCLR = 0xFFFFFFFF`.
4. Explicitly configure the peripheral that you are about to enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
5. Enable the now configured peripheral.

See which peripherals are sharing ID in [Instantiation](#) on page 18.

## 6.1.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

The peripheral must be enabled before tasks and events can be used.

## 6.1.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing 1 to a bit in SET or CLR register will set or clear the same bit in the main register respectively. Writing 0 to a bit in SET or CLR register has no effect. Reading the SET or CLR register returns the value of the main register.

**Note:** The main register may not be visible and hence not directly accessible in all cases.

## 6.1.5 Tasks

Tasks are used to trigger actions in a peripheral, for example to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes 1 to the task register, or when the peripheral itself or another peripheral toggles the corresponding task signal. See [Tasks, events, shortcuts, and interrupts](#) on page 85.

## 6.1.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See [Tasks, events, shortcuts, and interrupts](#) on page 85. An event register is only cleared when firmware writes 0 to it.

Events can be generated by the peripheral even when the event register is set to 1.

### 6.1.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, the associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

### 6.1.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using the INTEN, INTENSET, and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR registers, and the INTEN register is not available on those peripherals. See the individual peripheral chapters for details. In all cases, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET, and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in [Tasks, events, shortcuts, and interrupts](#) on page 85.

#### Interrupt clearing

Clearing an interrupt by writing 0 to an event register, or disabling an interrupt using the INTENCLR register, can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediately, even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled but before four clock cycles have passed.

**Note:** To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers. For example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt. This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler.

Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after an event is cleared or an interrupt is disabled, then a read of a register is not required.

## 6.2 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the Resolvable Private Address Resolution Procedure described in the *Bluetooth Core specification v4.0*. Resolvable Private Address generation should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

### 6.2.1 EasyDMA

AAR implements EasyDMA for reading and writing to RAM. EasyDMA will have finished accessing RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the [IRKPTR](#) on page 93, [ADDRPTR](#) on page 93, and the [SCRATCHPTR](#) on page 93 is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

### 6.2.2 Resolving a resolvable address

As per *Bluetooth* specification, a private resolvable address is composed of six bytes.

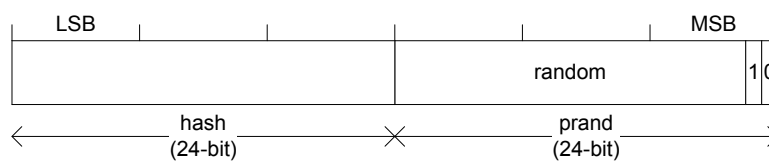


Figure 25: Resolvable address

To resolve an address the register [ADDRPTR](#) on page 93 must point to the start of the packet. The resolver is started by triggering the START task. A RESOLVED event is generated when AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. The register [NIRK](#) on page 92 specifies how many IRKs should be used. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth Core specification v4.0 [Vol 3]* chapter 10.8.2.3. The time it takes to resolve an address varies due to the location in the list of the resolvable address. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the [Electrical specifications](#) for more information about resolution time.

AAR only compares the received address to those programmed in the module without checking the address type.

AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. AAR will generate an END event after it has stopped.



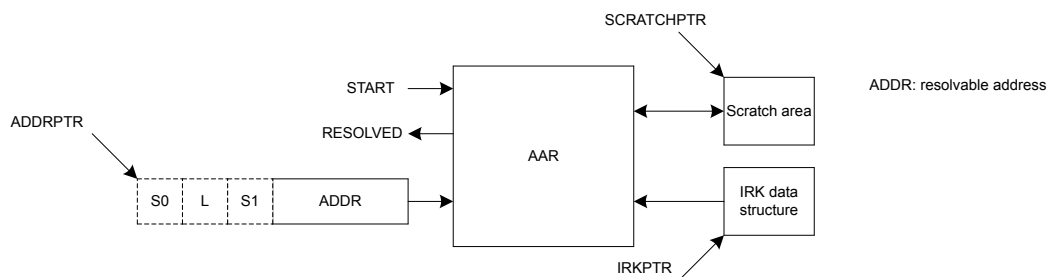


Figure 26: Address resolution with packet preloaded into RAM

### 6.2.3 Use case example for chaining RADIO packet reception with address resolution using AAR

AAR may be started as soon as the 6 bytes required by AAR have been received by RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

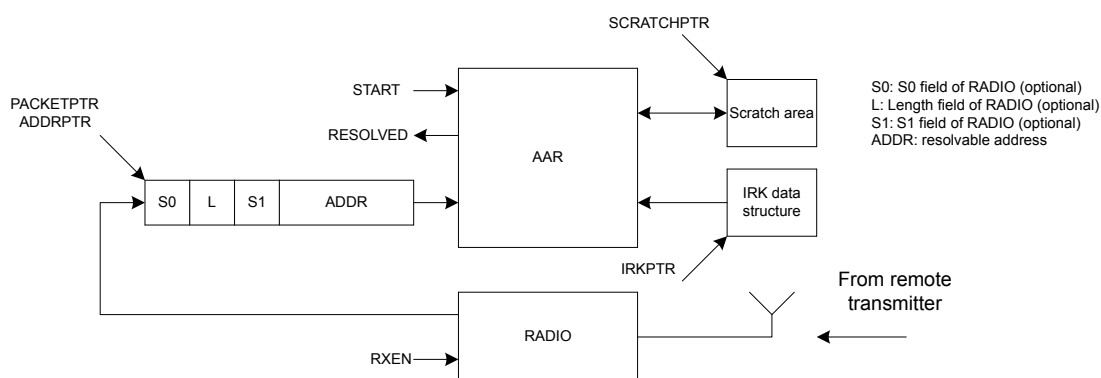


Figure 27: Address resolution with packet loaded into RAM by RADIO

### 6.2.4 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the IRKPTR register.

Property	Address offset	Description
IRK0	0	IRK number 0 (16 bytes)
IRK1	16	IRK number 1 (16 bytes)
..	..	..
IRK15	240	IRK number 15 (16 bytes)

Table 21: IRK data structure overview

### 6.2.5 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Accelerated address resolver	

Table 22: Instances

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete

Register	Offset	Description
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

Table 23: Register overview

### 6.2.5.1 TASKS\_START

Address offset: 0x000

Start resolving addresses based on IRKs specified in the IRK data structure

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_START			Start resolving addresses based on IRKs specified in the IRK data structure																											
			Trigger	1	Trigger task																											

### 6.2.5.2 TASKS\_STOP

Address offset: 0x008

Stop resolving addresses

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STOP			Stop resolving addresses																											
			Trigger	1	Trigger task																											

### 6.2.5.3 EVENTS\_END

Address offset: 0x100

Address resolution procedure complete

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_END			Address resolution procedure complete																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.2.5.4 EVENTS\_RESOLVED

Address offset: 0x104

Address resolved

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_RESOLVED			Address resolved																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.2.5.5 EVENTS\_NOTRESOLVED

Address offset: 0x108

Address not resolved

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_NOTRESOLVED			Address not resolved																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.2.5.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C B A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	END			Write '1' to enable interrupt for event END																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
B	RW	RESOLVED			Write '1' to enable interrupt for event RESOLVED																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											
C	RW	NOTRESOLVED			Write '1' to enable interrupt for event NOTRESOLVED																											
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
			Enabled	1	Read: Enabled																											

### 6.2.5.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																															C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																
ID	Acce	Field	Value ID	Value	Description																												
A	RW	END			Write '1' to disable interrupt for event <b>END</b>																												
			Clear	1	Disable																												
			Disabled	0	Read: Disabled																												
			Enabled	1	Read: Enabled																												
B	RW	RESOLVED			Write '1' to disable interrupt for event <b>RESOLVED</b>																												
			Clear	1	Disable																												
			Disabled	0	Read: Disabled																												
			Enabled	1	Read: Enabled																												
C	RW	NOTRESOLVED			Write '1' to disable interrupt for event <b>NOTRESOLVED</b>																												
			Clear	1	Disable																												
			Disabled	0	Read: Disabled																												
			Enabled	1	Read: Enabled																												

### 6.2.5.8 STATUS

Address offset: 0x400

Resolution status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce	Field	Value ID	Value	Description																													
A	R	STATUS		[0..15]	The IRK that was used last time an address was resolved																													

### 6.2.5.9 ENABLE

Address offset: 0x500

Enable AAR

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	ENABLE			Enable or disable AAR																											
			Disabled	0	Disable																											
			Enabled	3	Enable																											

### 6.2.5.10 NIRK

Address offset: 0x504

Number of IRKs

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000001</b>	<b>0 1</b>																																	
ID	Acce	Field	Value ID	Value	Description																													
A	RW	NIRK		[1..16]	Number of Identity root keys available in the IRK data structure																													

### 6.2.5.11 IRKPTR

Address offset: 0x508

Pointer to IRK data structure

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	IRKPTR			Pointer to the IRK data structure																											

### 6.2.5.12 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	ADDRPTR			Pointer to the resolvable address (6-bytes)																											

### 6.2.5.13 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	SCRATCHPTR			Pointer to a scratch data area used for temporary storage during resolution. A space of minimum 3 bytes must be reserved.																											

## 6.2.6 Electrical specification

### 6.2.6.1 AAR Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{AAR}$	Address resolution time per IRK. Total time for several IRKs is given as $(1 \mu s + n * t_{AAR})$ , where n is the number of IRKs. (Given priority to the actual destination RAM block).			6	$\mu s$
$t_{AAR,8}$	Time for address resolution of 8 IRKs. (Given priority to the actual destination RAM block).			49	$\mu s$

## 6.3 ACL — Access control lists

The Access control lists (ACL) peripheral is designed to assign and enforce access permissions to different regions of the on-chip flash memory map.

Flash memory regions can be assigned individual ACL permission schemes. The following registers are involved:

- PERM register, where the permissions are configured.
- ADDR register, where the word-aligned start address for the flash page is defined.
- SIZE register, where the size of the region the permissions are applied to is determined.

**Note:** The size of the region in bytes is restricted to a multiple of the flash page size, and the maximum region size is limited to half the flash size. See [Memory](#) on page 15 for more information.

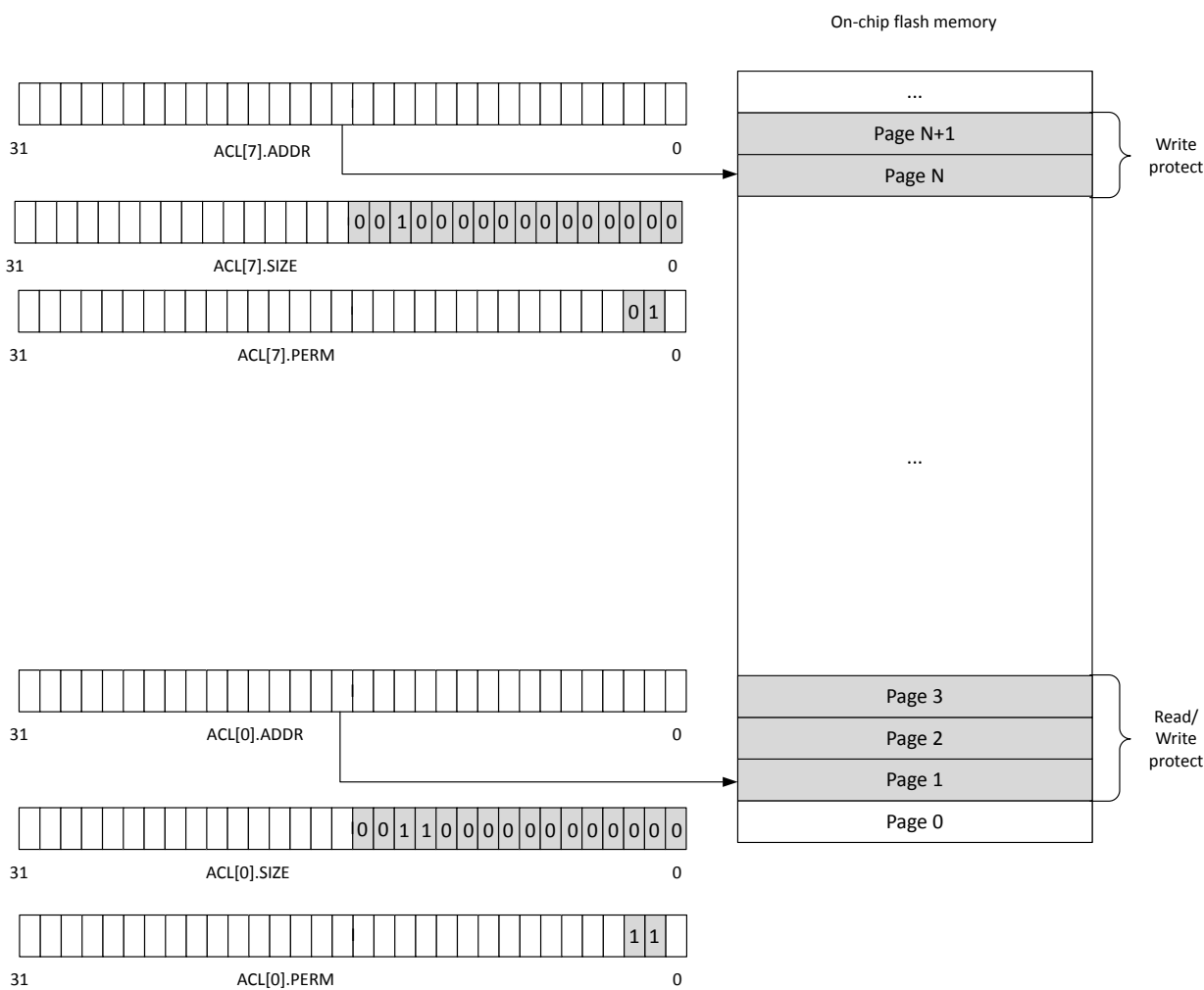


Figure 28: Protected regions of on-chip flash memory

There are four defined ACL permission schemes, with different combinations of read/write permissions:

Read	Write	Protection description
0	0	No protection. Entire region can be executed, read, written or erased.
0	1	Region can be executed and read, but not written or erased.
1	0	Region can be written and erased, but not executed or read.
1	1	Region is locked for all access until next reset.

Table 24: Permission schemes

**Note:** If a permission violation to a protected region is detected by the ACL peripheral, the request is blocked and a Bus Fault exception is triggered.

Access control to a configured region is enforced by the hardware two CPU clock cycles after the ADDR, SIZE, and PERM registers for an ACL instance have been successfully written. The protection is only enforced if a valid start address of the flash page boundary is written into the ADDR register, and the values of the SIZE and PERM registers are not zero.

The ADDR, SIZE, and PERM registers can only be written once. All ACL configuration registers are cleared on reset (by resetting the device from any reset source), which is also the only way of clearing the configuration registers. To ensure that the desired permission schemes are always enforced by the ACL peripheral, the device boot sequence must perform the necessary configuration.

Debugger read access to a read-protected region will be Read-As-Zero (RAZ), while debugger write access to a write-protected region will be Write-Ignored (WI).

### 6.3.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	ACL	ACL	Access control lists	

Table 25: Instances

Register	Offset	Description
ACL[0].ADDR	0x800	Start address of region to protect. The start address must be word-aligned.
ACL[0].SIZE	0x804	Size of region to protect counting from address ACL[0].ADDR. Write '0' as no effect.
ACL[0].PERM	0x808	Access permissions for region 0 as defined by start address ACL[0].ADDR and size ACL[0].SIZE
ACL[0].UNUSED0	0x80C	Reserved
ACL[1].ADDR	0x810	Start address of region to protect. The start address must be word-aligned.
ACL[1].SIZE	0x814	Size of region to protect counting from address ACL[1].ADDR. Write '0' as no effect.
ACL[1].PERM	0x818	Access permissions for region 1 as defined by start address ACL[1].ADDR and size ACL[1].SIZE
ACL[1].UNUSED0	0x81C	Reserved
ACL[2].ADDR	0x820	Start address of region to protect. The start address must be word-aligned.
ACL[2].SIZE	0x824	Size of region to protect counting from address ACL[2].ADDR. Write '0' as no effect.
ACL[2].PERM	0x828	Access permissions for region 2 as defined by start address ACL[2].ADDR and size ACL[2].SIZE
ACL[2].UNUSED0	0x82C	Reserved
ACL[3].ADDR	0x830	Start address of region to protect. The start address must be word-aligned.
ACL[3].SIZE	0x834	Size of region to protect counting from address ACL[3].ADDR. Write '0' as no effect.
ACL[3].PERM	0x838	Access permissions for region 3 as defined by start address ACL[3].ADDR and size ACL[3].SIZE
ACL[3].UNUSED0	0x83C	Reserved
ACL[4].ADDR	0x840	Start address of region to protect. The start address must be word-aligned.
ACL[4].SIZE	0x844	Size of region to protect counting from address ACL[4].ADDR. Write '0' as no effect.
ACL[4].PERM	0x848	Access permissions for region 4 as defined by start address ACL[4].ADDR and size ACL[4].SIZE
ACL[4].UNUSED0	0x84C	Reserved
ACL[5].ADDR	0x850	Start address of region to protect. The start address must be word-aligned.
ACL[5].SIZE	0x854	Size of region to protect counting from address ACL[5].ADDR. Write '0' as no effect.
ACL[5].PERM	0x858	Access permissions for region 5 as defined by start address ACL[5].ADDR and size ACL[5].SIZE
ACL[5].UNUSED0	0x85C	Reserved
ACL[6].ADDR	0x860	Start address of region to protect. The start address must be word-aligned.
ACL[6].SIZE	0x864	Size of region to protect counting from address ACL[6].ADDR. Write '0' as no effect.
ACL[6].PERM	0x868	Access permissions for region 6 as defined by start address ACL[6].ADDR and size ACL[6].SIZE
ACL[6].UNUSED0	0x86C	Reserved
ACL[7].ADDR	0x870	Start address of region to protect. The start address must be word-aligned.
ACL[7].SIZE	0x874	Size of region to protect counting from address ACL[7].ADDR. Write '0' as no effect.
ACL[7].PERM	0x878	Access permissions for region 7 as defined by start address ACL[7].ADDR and size ACL[7].SIZE

Register	Offset	Description
ACL[7].UNUSED0	0x87C	Reserved

Table 26: Register overview

### 6.3.1.1 ACL[n].ADDR (n=0..7)

Address offset:  $0x800 + (n \times 0x10)$

Start address of region to protect. The start address must be word-aligned.

This register can only be written once.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW1 ADDR			Start address of flash region n. The start address must point to a flash page boundary.																												

### 6.3.1.2 ACL[n].SIZE (n=0..7)

Address offset:  $0x804 + (n \times 0x10)$

Size of region to protect counting from address ACL[n].ADDR. Write '0' as no effect.

This register can only be written once.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW1 SIZE			Size of flash region n in bytes. Must be a multiple of the flash page size.																												

### 6.3.1.3 ACL[n].PERM (n=0..7)

Address offset:  $0x808 + (n \times 0x10)$

Access permissions for region n as defined by start address ACL[n].ADDR and size ACL[n].SIZE

This register can only be written once.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															C	B
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
B	RW1 WRITE			Configure write and erase permissions for region n. Write '0' has no effect.																												
		Enable	0	Allow write and erase instructions to region n																												
		Disable	1	Block write and erase instructions to region n																												
C	RW1 READ			Configure read permissions for region n. Write '0' has no effect.																												
		Enable	0	Allow read instructions to region n																												
		Disable	1	Block read instructions to region n																												



## 6.4 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in *Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the four byte MIC field in one operation. CCM and RADIO can be configured to work synchronously. CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF [RFC3610](#), and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in [NIST Special Publication 800-38C](#). The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for Bluetooth Low Energy.

The CCM block uses EasyDMA to load key counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM peripheral supports three operations: keystream generation, packet encryption, and packet decryption. These operations are performed in compliance with the *Bluetooth* AES CCM 128 bit block encryption, see *Bluetooth Core specification Version 4.0*.

The following figure illustrates keystream generation followed by encryption or decryption. The shortcut is optional.

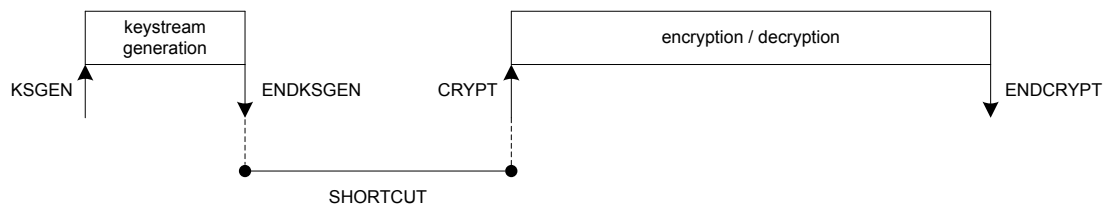


Figure 29: Keystream generation

### 6.4.1 Keystream generation

A new keystream needs to be generated before a new packet encryption or packet decryption operation can start.

A keystream is generated by triggering the KSGEN task. An ENDKSGEN event is generated after the keystream has been generated.

Keystream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by [CNFPTR](#) on page 107. It is necessary to configure this pointer and its underlying data structure, and register [MODE](#) on page 106 before the KSGEN task is triggered.

The keystream will be stored in the AES CCM peripheral's temporary memory area, specified by the [SCRATCHPTR](#) on page 107, where it will be used in subsequent encryption and decryption operations.

For default length packets ([MODE.LENGTH](#) = Default), the size of the generated keystream is 27 bytes. When using extended length packets ([MODE.LENGTH](#) = Extended), register [MAXPACKETSIZE](#) on page 108 specifies the length of the keystream to be generated. The length of the generated keystream must be greater or equal to the length of the subsequent packet payload to be encrypted or decrypted. The maximum length of the keystream in extended mode is 251 bytes, which means that the maximum packet payload size is 251.

If a shortcut is used between the ENDKSGEN event and CRYPT task, pointer [INPTR](#) on page 107 and the pointers [OUTPTR](#) on page 107 must also be configured before the KSGEN task is triggered.

## 6.4.2 Encryption

The AES CCM peripheral is able to read an unencrypted packet, encrypt it, and append a four byte MIC field to the packet.

During packet encryption, the AES CCM peripheral performs the following:

- Reads the unencrypted packet located in RAM address specified in the INPTR pointer
- Encrypts the packet
- Appends a four byte long Message Integrity Check (MIC) field to the packet

Encryption is started by triggering the CRYPT task with register [MODE](#) on page 106 set to ENCRYPTION. An ENDCRYPT event is generated when packet encryption is completed.

The AES CCM peripheral will also modify the length field of the packet to adjust for the appended MIC field. It adds four bytes to the length and stores the resulting packet in RAM at the address specified in pointer [OUTPTR](#) on page 107, see [Encryption](#) on page 98.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM peripheral.

AES CCM supports different widths of the LENGTH field in the data structure for encrypted packets. This is configured in register [MODE](#) on page 106.

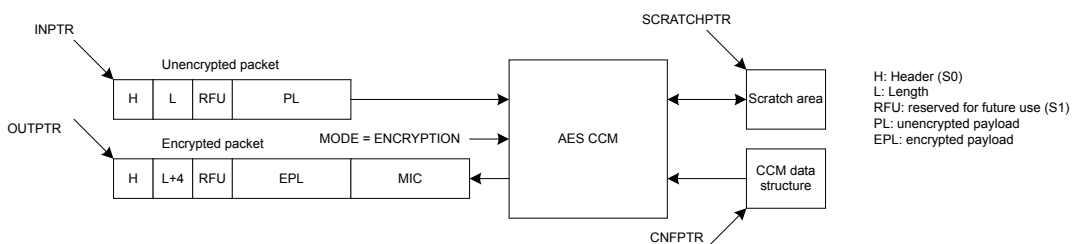


Figure 30: Encryption

## 6.4.3 Decryption

The AES CCM peripheral is able to read an encrypted packet, decrypt it, authenticate the MIC field, and generate an appropriate MIC status.

During packet decryption, the AES CCM peripheral performs the following:

- Reads the encrypted packet located in RAM at the address specified in the INPTR pointer
- Decrypts the packet
- Authenticates the packet's MIC field
- Generates the appropriate MIC status

Decryption is started by triggering the CRYPT task with register [MODE](#) on page 106 set to DECRYPTION. An ENDCRYPT event is generated when packet decryption is completed.

The AES CCM peripheral modifies the length field of the packet to adjust for the MIC field. It subtracts four bytes from the length and stores the decrypted packet in RAM at the address specified in the pointer [OUTPTR](#), see [Decryption](#) on page 99.

CCM is only able to decrypt packet payloads that are at least five bytes long (one byte or more encrypted payload (EPL) and four bytes of MIC). CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3, or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM peripheral. These packets will always pass the MIC check.

CCM supports different widths of the LENGTH field in the data structure for decrypted packets. This is configured in register [MODE](#) on page 106.

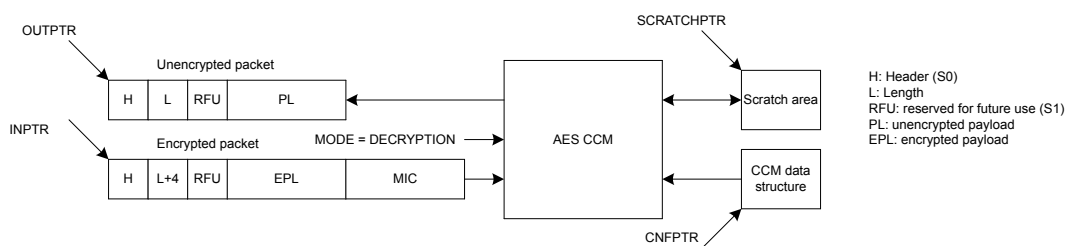


Figure 31: Decryption

### 6.4.4 AES CCM and RADIO concurrent operation

The CCM peripheral is able to encrypt/decrypt data synchronously to data being transmitted or received on the radio.

In order for CCM to run synchronously with the radio, the data rate setting in register [MODE](#) on page 106 needs to match the radio data rate. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered.

The data rate setting of register [MODE](#) on page 106 can also be overridden on-the-fly during an ongoing encrypt/decrypt operation by the contents of register [RATEOVERRIDE](#) on page 108. The data rate setting in this register applies whenever the RATEOVERRIDE task is triggered. This feature can be useful in cases where the radio data rate is changed during an ongoing packet transaction.

### 6.4.5 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM peripheral encrypts a packet on-the-fly while RADIO is transmitting it, RADIO must read the encrypted packet from the same memory location that the AES CCM peripheral is writing to.

The [OUTPTR](#) on page 107 pointer in the AES CCM must point to the same memory location as the [PACKETPTR](#) pointer in the radio, see [Configuration of on-the-fly encryption](#) on page 99.

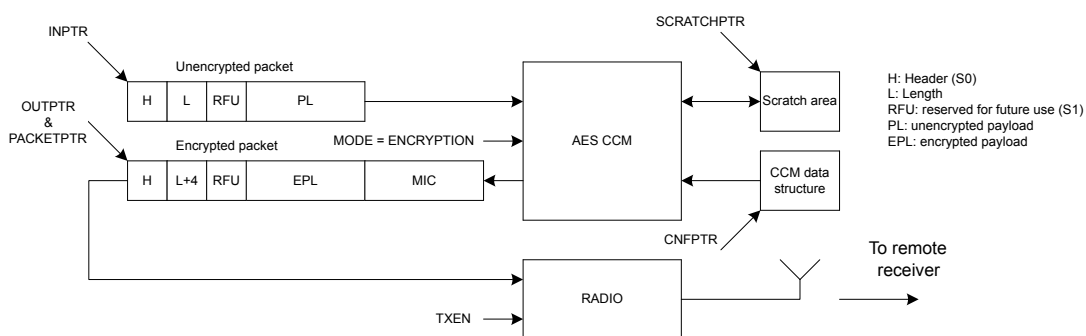


Figure 32: Configuration of on-the-fly encryption

In order to match RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before packet encryption begins.

For short packets ([MODE.LENGTH = Default](#)), the KSGEN task must be triggered before or at the same time as the START task in RADIO is triggered. In addition, the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in [On-the-fly encryption of short packets \(MODE.LENGTH = Default\) using a PPI connection](#) on page 100. It uses a PPI connection between the READY event in RADIO and the KSGEN task in the AES CCM peripheral.

For long packets (MODE.LENGTH = Extended), the keystream generation needs to start earlier, such as when the TXEN task in RADIO is triggered.

Refer to [Timing specification](#) on page 109 for information about the time needed for generating a keystream.

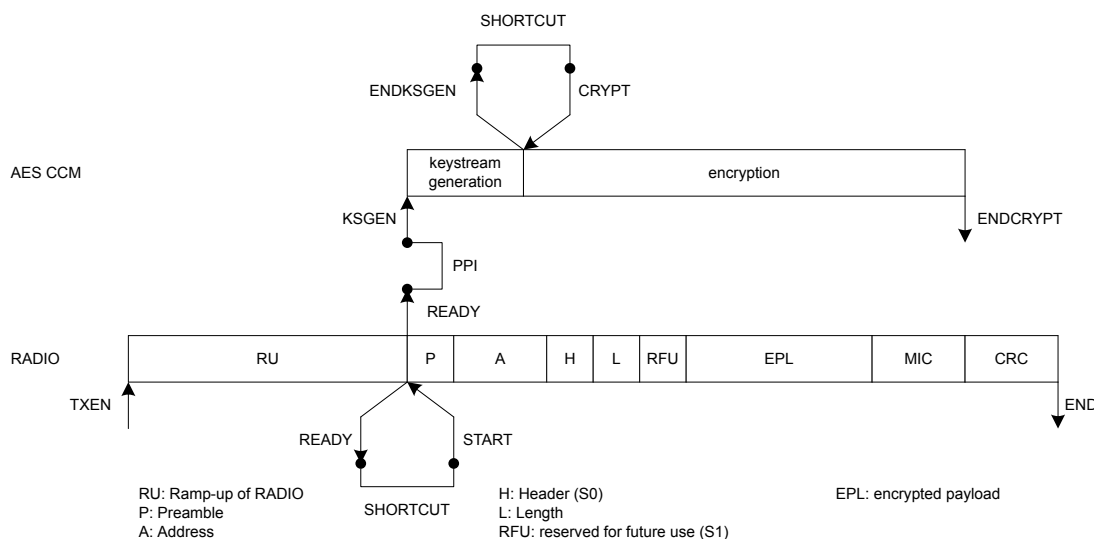


Figure 33: On-the-fly encryption of short packets (MODE.LENGTH = Default) using a PPI connection

### 6.4.6 Decrypting packets on-the-fly in RADIO receive mode

When the AES CCM peripheral decrypts a packet on-the-fly while RADIO is receiving it, the AES CCM peripheral must read the encrypted packet from the same memory location that RADIO is writing to.

The INPTR on page 107 pointer in the AES CCM must point to the same memory location as the PACKETPTR pointer in RADIO, see [Configuration of on-the-fly decryption](#) on page 100.

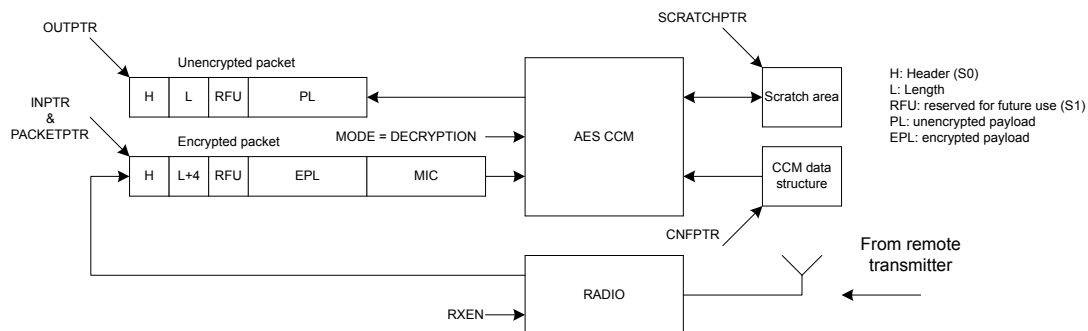


Figure 34: Configuration of on-the-fly decryption

In order to match RADIO's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the decryption of the packet shall start.

For short packets (MODE.LENGTH = Default) the KSGEN task must be triggered no later than when the START task in RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by RADIO, the AES CCM peripheral will guarantee that the decryption is completed no later than when the END event in RADIO is generated.

This use-case is illustrated in [On-the-fly decryption of short packets \(MODE.LENGTH = Default\) using a PPI connection](#) on page 101 using a PPI connection between the ADDRESS event in RADIO and the CRYPT

task in the AES CCM peripheral. The KSGEN task is triggered from the READY event in RADIO through a PPI connection.

For long packets (MODE.LENGTH = Extended) the keystream generation will need to start even earlier, such as when the RXEN task in RADIO is triggered.

Refer to [Timing specification](#) on page 109 for information about the time needed for generating a keystream.

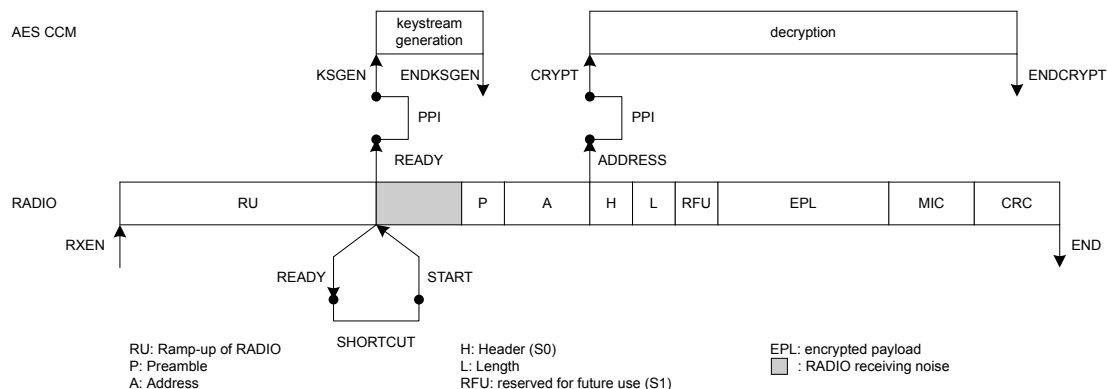


Figure 35: On-the-fly decryption of short packets (MODE.LENGTH = Default) using a PPI connection

## 6.4.7 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV, ..., Octet7 (MSO) of IV

Table 27: CCM data structure overview

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from [CCM data structure overview](#) on page 101 .

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 28: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in encrypted payload including length of MIC LENGTH will be 0 for empty packets since the MIC is not added to empty packets
RFU	2	Reserved Future Use
PAYLOAD	3	Encrypted payload
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC MIC is not added to empty packets

Table 29: Data structure for encrypted packet

## 6.4.8 EasyDMA and ERROR event

CCM implements an EasyDMA mechanism for reading and writing to RAM.

When the CPU and EasyDMA enabled peripherals access the same RAM block at the same time, increased bus collisions might disrupt on-the-fly encryption. This will generate an ERROR event.

EasyDMA stops accessing RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR, and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

## 6.4.9 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	CCM	CCM	AES counter with CBC-MAC (CCM) mode block encryption	

Table 30: Instances

Register	Offset	Description
TASKS_KSGEN	0x000	Start generation of keystream. This operation will stop by itself when completed.
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x008	Stop encryption/decryption
TASKS_RATEOVERRIDE	0x00C	Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption
EVENTS_ENDKSGEN	0x100	Keystream generation complete
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete
EVENTS_ERROR	0x108	CCM error event
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MICSTATUS	0x400	MIC check result
ENABLE	0x500	Enable
MODE	0x504	Operation mode
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector
INPTR	0x50C	Input pointer
OUTPTR	0x510	Output pointer
SCRATCHPTR	0x514	Pointer to data area used for temporary storage
MAXPACKETSIZE	0x518	Length of keystream generated when MODE.LENGTH = Extended.
RATEOVERRIDE	0x51C	Data rate override setting.

Table 31: Register overview

### 6.4.9.1 TASKS\_KSGEN

Address offset: 0x000

Start generation of keystream. This operation will stop by itself when completed.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_KSGEN			Start generation of keystream. This operation will stop by itself when completed.																											
		Trigger	1	Trigger task																											

### 6.4.9.2 TASKS\_CRYPT

Address offset: 0x004

Start encryption/decryption. This operation will stop by itself when completed.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_CRYPT			Start encryption/decryption. This operation will stop by itself when completed.																											
		Trigger	1	Trigger task																											

### 6.4.9.3 TASKS\_STOP

Address offset: 0x008

Stop encryption/decryption

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_STOP			Stop encryption/decryption																											
		Trigger	1	Trigger task																											

### 6.4.9.4 TASKS\_RATEOVERRIDE

Address offset: 0x00C

Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																												
A	W	TASKS_RATEOVERRIDE			Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption																												
			Trigger	1	Trigger task																												

### 6.4.9.5 EVENTS\_ENDKSGEN

Address offset: 0x100

Keystream generation complete

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDKSGEN			Keystream generation complete																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.4.9.6 EVENTS\_ENDCRYPT

Address offset: 0x104

Encrypt/decrypt complete

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDCRYPT			Encrypt/decrypt complete																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.4.9.7 EVENTS\_ERROR ( Deprecated )

Address offset: 0x108

CCM error event

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_ERROR			CCM error event																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.4.9.8 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ENDKSGEN_CRYPT			Shortcut between event <a href="#">ENDKSGEN</a> and task <a href="#">CRYPT</a>																												
		Disabled	0	Disable shortcut																												
		Enabled	1	Enable shortcut																												

### 6.4.9.9 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C B A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ENDKSGEN			Write '1' to enable interrupt for event <a href="#">ENDKSGEN</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW ENDCRYPT			Write '1' to enable interrupt for event <a href="#">ENDCRYPT</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW ERROR			Write '1' to enable interrupt for event <a href="#">ERROR</a> <span style="float: right;">Deprecated</span>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.4.9.10 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																C B A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ENDKSGEN			Write '1' to disable interrupt for event <a href="#">ENDKSGEN</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW ENDCRYPT			Write '1' to disable interrupt for event <a href="#">ENDCRYPT</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW ERROR			Write '1' to disable interrupt for event <a href="#">ERROR</a> <span style="float: right;">Deprecated</span>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.4.9.11 MICSTATUS

Address offset: 0x400

MIC check result

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	R	MICSTATUS			The result of the MIC check performed during the previous decryption operation																											
			CheckFailed	0	MIC check failed																											
			CheckPassed	1	MIC check passed																											

### 6.4.9.12 ENABLE

Address offset: 0x500

Enable

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	ENABLE			Enable or disable CCM																											
			Disabled	0	Disable																											
			Enabled	2	Enable																											

### 6.4.9.13 MODE

Address offset: 0x504

Operation mode

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID											C											B B											A
Reset 0x00000001	0 1																																
ID	Acce	Field	Value ID	Value	Description																												
A	RW	MODE			The mode of operation to be used. The settings in this register apply whenever either the KSGEN or CRYPT tasks are triggered.																												
			Encryption	0	AES CCM packet encryption mode																												
			Decryption	1	AES CCM packet decryption mode																												
B	RW	DATARATE			Radio data rate that the CCM shall run synchronous with																												
			1Mbit	0	1 Mbps																												
			2Mbit	1	2 Mbps																												
			125Kbps	2	125 Kbps																												
			500Kbps	3	500 Kbps																												
C	RW	LENGTH			Packet length configuration																												
			Default	0	Default length. Effective length of LENGTH field in encrypted/decrypted packet is 5 bits. A keystream for packet payloads up to 27 bytes will be generated.																												



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	SCRATCHPTR		<p>Pointer to a scratch data area used for temporary storage during keystream generation, MIC generation and encryption/decryption.</p> <p>The scratch area is used for temporary storage of data during keystream generation and encryption.</p> <p>When MODE.LENGTH = Default, a space of 43 bytes is required for this temporary storage. MODE.LENGTH = Extended (16 + MAXPACKETSIZE) bytes of storage is required.</p>

### 6.4.9.18 MAXPACKETSIZE

Address offset: 0x518

Length of keystream generated when MODE.LENGTH = Extended.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																										A	A	A	A	A	A	A	
<b>Reset 0x000000FB</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1

ID	Acce Field	Value ID	Value	Description
A	RW	MAXPACKETSIZE	[0x001B..0x00FB]	<p>Length of keystream generated when MODE.LENGTH = Extended. This value must be greater or equal to the subsequent packet payload to be encrypted/decrypted.</p>

### 6.4.9.19 RATEOVERRIDE

Address offset: 0x51C

Data rate override setting.

Override value to be used instead of the setting of MODE.DATARATE. This override value applies when the RATEOVERRIDE task is triggered.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	A
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

ID	Acce Field	Value ID	Value	Description
A	RW	RATEOVERRIDE		Data rate override setting.
		1Mbit	0	1 Mbps
		2Mbit	1	2 Mbps
		125Kbps	2	125 Kbps
		500Kbps	3	500 Kbps

## 6.4.10 Electrical specification

### 6.4.10.1 Timing specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{ngen}}$	Time needed for keystream generation (given priority access to destination RAM block).			50	$\mu\text{s}$

## 6.5 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived either from an analog input pin (AIN0-AIN6) or VDDH/5. VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
  - Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
  - Configurable hysteresis
- Reference inputs (VREF):
  - VDD
  - External reference from AIN0 to AIN7 (between 0 V and VDD)
  - Internal references 1.2 V, 1.8 V, and 2.4 V
- Three speed/power consumption modes: low-power, normal, and high-speed
- Event generation on output changes
  - UP event on VIN- > VIN+
  - DOWN event on VIN- < VIN+
  - CROSS event on VIN+ and VIN- crossing
  - READY event on core and internal reference (if used) ready

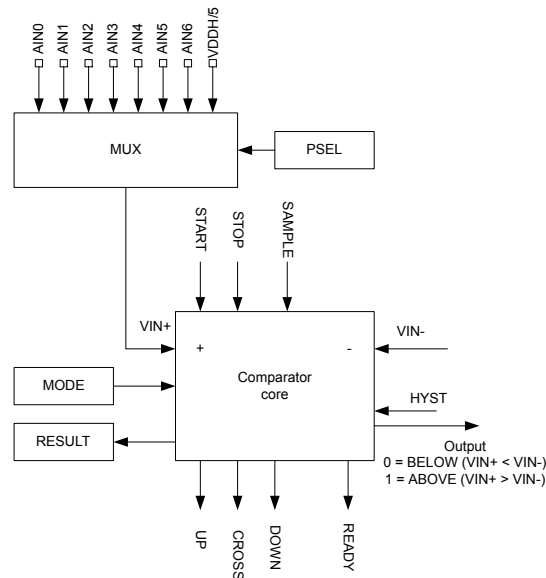


Figure 36: Comparator overview

Once enabled (using the [ENABLE](#) register), the comparator is started by triggering the START task and stopped by triggering the STOP task. The comparator will generate a READY event to indicate when it is ready for use and the output is correct. The delay between START and READY is  $t_{INT\_REF,START}$  if an internal reference is selected, or  $t_{COMP,START}$  if an external reference is used. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.

## Operation modes

The comparator can be configured to operate in two main operation modes: differential mode and single-ended mode. See the [MODE](#) register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the [PSEL](#) register to select any of the AIN0-AIN6 pins (or VDDH/5) as VIN+ input, regardless of the operation mode selected for the comparator. The source of VIN- depends on which of the following operation mode are used:

- Differential mode - Derived directly from AIN0 to AIN7
- Single-ended mode - Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the [HYST](#) register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see [Comparator in single-ended mode](#) on page 112). This hysteresis is in the order of magnitude of  $V_{DIFFHYST}$ , and shall prevent noise on the signal to create unwanted events. See [Hysteresis example where VIN+ starts below VUP](#) on page 113 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to [RESULT](#) register by triggering the SAMPLE task.

## 6.5.1 Differential mode

In differential mode, the reference input  $V_{IN-}$  is derived directly from one of the  $A_{INx}$  pins.

Before enabling the comparator via the **ENABLE** register, the following registers must be configured for the differential mode:

- **PSEL**
- **MODE**
- **EXTREFSEL**

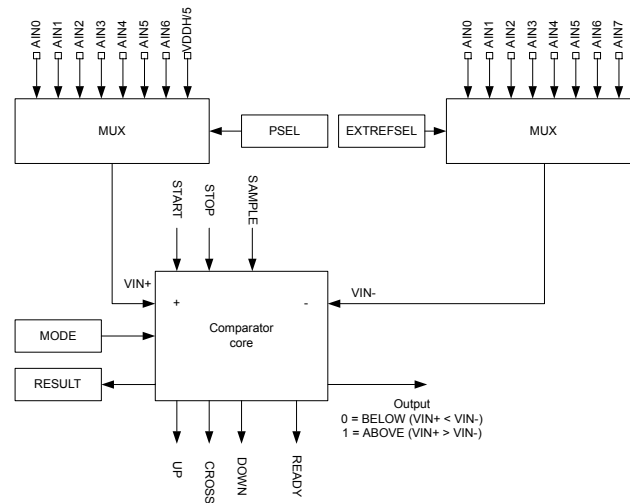


Figure 37: Comparator in differential mode

**Note:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for **PSEL** and **EXTREFSEL** for more information about which analog pins are available on a particular device.

When the **HYST** register is turned on during this mode, the output of the comparator and associated events do the following:

- Change from ABOVE to BELOW when  $V_{IN+}$  drops below  $V_{IN-} - (V_{DIFFHYST}/2)$
- Change from BELOW to ABOVE when  $V_{IN+}$  raises above  $V_{IN-} + (V_{DIFFHYST}/2)$

This behavior is illustrated in the following figure.

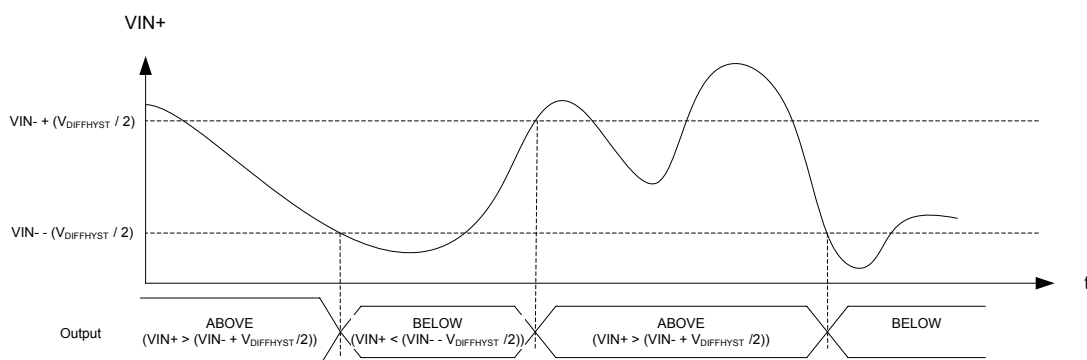


Figure 38: Hysteresis enabled in differential mode

## 6.5.2 Single-ended mode

In single-ended mode, VIN- is derived from the reference ladder.

Before enabling the comparator via the **ENABLE** register, the following registers must be configured for the single-ended mode:

- **PSEL**
- **MODE**
- **REFSEL**
- **EXTREFSEL**
- **TH**

The reference ladder uses the reference voltage (VREF) to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured using THUP and THDOWN respectively in the **TH** register. VREF can be derived from any of the available reference sources, configured using the **EXTREFSEL** and **REFSEL** registers as illustrated in [Comparator in single-ended mode](#) on page 112. When AREF is selected in the **REFSEL** register, the **EXTREFSEL** register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.

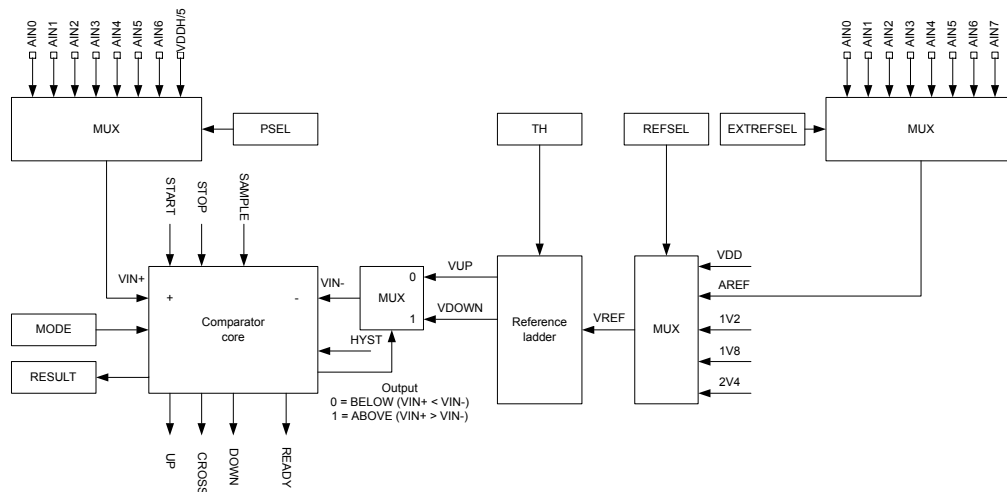


Figure 39: Comparator in single-ended mode

**Note:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for **PSEL** and **EXTREFSEL** for more information about which analog pins are available on a particular device.

When the comparator core detects that  $VIN+ > VIN-$ , i.e. ABOVE as per the **RESULT** register,  $VIN-$  will switch to VDOWN. When  $VIN+$  falls below  $VIN-$  again,  $VIN-$  will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis can be generated as illustrated in [Hysteresis example where  \$VIN+\$  starts below VUP](#) on page 113 and [Hysteresis example where  \$VIN+\$  starts above VUP](#) on page 113.

Writing to **HYST** has no effect in single-ended mode, and the content of this register is ignored.



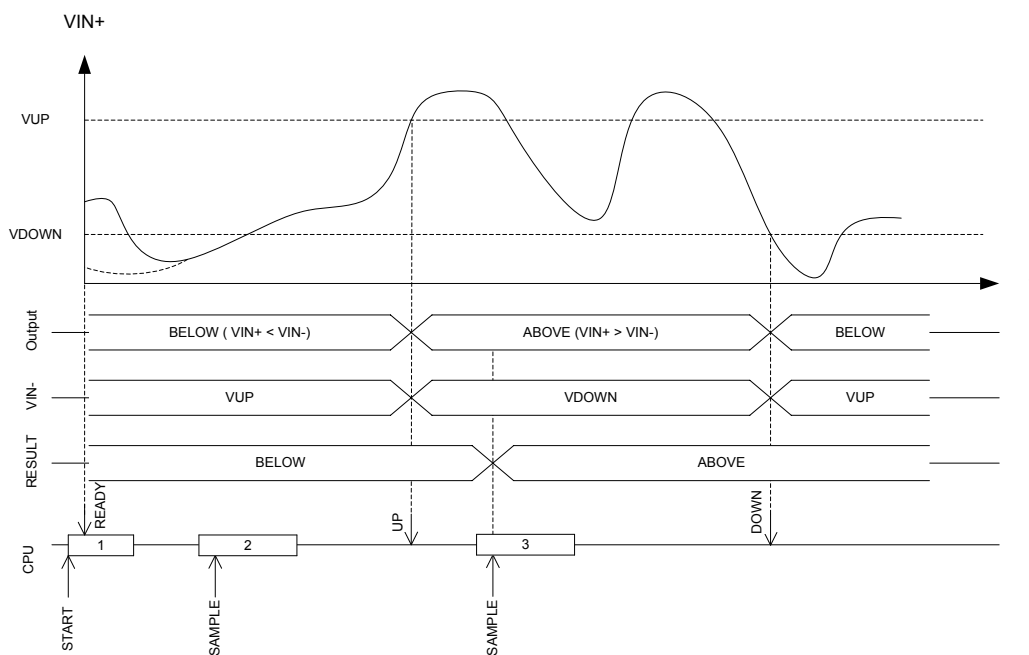


Figure 40: Hysteresis example where  $VIN+$  starts below  $VUP$

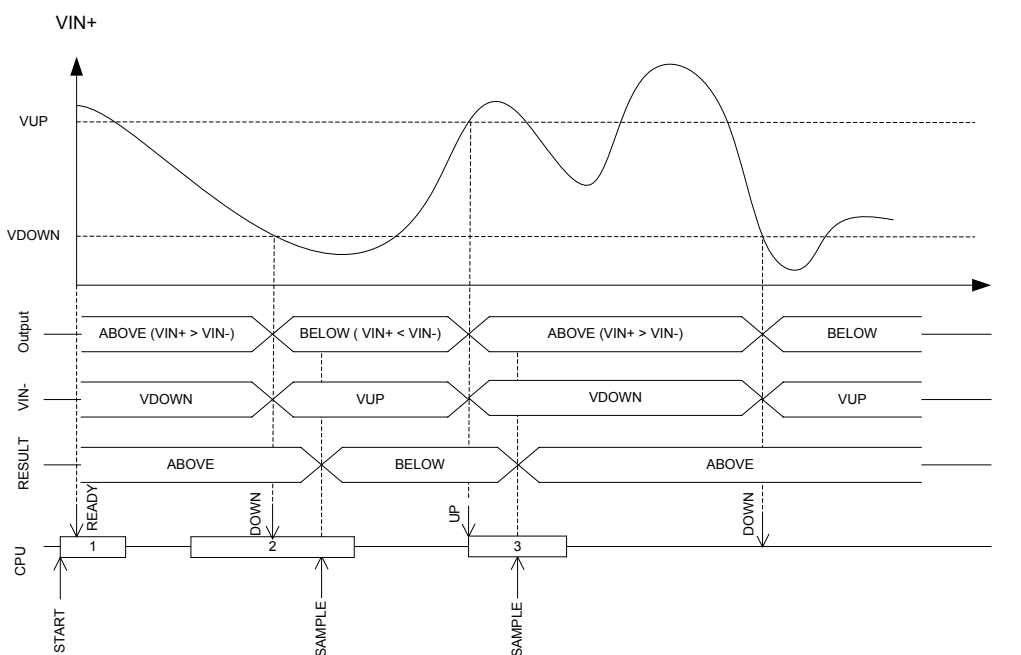


Figure 41: Hysteresis example where  $VIN+$  starts above  $VUP$

### 6.5.3 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40013000	COMP	COMP	General purpose comparator	

Table 32: Instances

Register	Offset	Description
TASKS_START	0x000	Start comparator

Register	Offset	Description
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcuts between local events and tasks
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select for single-ended mode
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable

Table 33: Register overview

### 6.5.3.1 TASKS\_START

Address offset: 0x000

Start comparator

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_START			Start comparator																											
			Trigger	1	Trigger task																											

### 6.5.3.2 TASKS\_STOP

Address offset: 0x004

Stop comparator

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STOP			Stop comparator																											
			Trigger	1	Trigger task																											

### 6.5.3.3 TASKS\_SAMPLE

Address offset: 0x008

Sample comparator value

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_SAMPLE	Trigger	1	Sample comparator value Trigger task																												

### 6.5.3.4 EVENTS\_READY

Address offset: 0x100

COMP is ready and output is valid

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_READY	NotGenerated	0	COMP is ready and output is valid Event not generated																												
		Generated	1	Event generated																												

### 6.5.3.5 EVENTS\_DOWN

Address offset: 0x104

Downward crossing

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_DOWN	NotGenerated	0	Downward crossing Event not generated																												
		Generated	1	Event generated																												

### 6.5.3.6 EVENTS\_UP

Address offset: 0x108

Upward crossing

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_UP	NotGenerated	0	Upward crossing Event not generated																												
		Generated	1	Event generated																												

### 6.5.3.7 EVENTS\_CROSS

Address offset: 0x10C

Downward or upward crossing

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_CROSS			Downward or upward crossing																											
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.5.3.8 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																E D C B A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	READY_SAMPLE			Shortcut between event <a href="#">READY</a> and task <a href="#">SAMPLE</a>																											
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											
B	RW	READY_STOP			Shortcut between event <a href="#">READY</a> and task <a href="#">STOP</a>																											
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											
C	RW	DOWN_STOP			Shortcut between event <a href="#">DOWN</a> and task <a href="#">STOP</a>																											
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											
D	RW	UP_STOP			Shortcut between event <a href="#">UP</a> and task <a href="#">STOP</a>																											
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											
E	RW	CROSS_STOP			Shortcut between event <a href="#">CROSS</a> and task <a href="#">STOP</a>																											
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											

### 6.5.3.9 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																D C B A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	READY			Enable or disable interrupt for event <a href="#">READY</a>																											
			Disabled	0	Disable																											
			Enabled	1	Enable																											
B	RW	DOWN			Enable or disable interrupt for event <a href="#">DOWN</a>																											
			Disabled	0	Disable																											
			Enabled	1	Enable																											
C	RW	UP			Enable or disable interrupt for event <a href="#">UP</a>																											
			Disabled	0	Disable																											
			Enabled	1	Enable																											
D	RW	CROSS			Enable or disable interrupt for event <a href="#">CROSS</a>																											
			Disabled	0	Disable																											

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
		Enabled	1	Enable																												

### 6.5.3.10 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	READY		Write '1' to enable interrupt for event <b>READY</b>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW	DOWN		Write '1' to enable interrupt for event <b>DOWN</b>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW	UP		Write '1' to enable interrupt for event <b>UP</b>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
D	RW	CROSS		Write '1' to enable interrupt for event <b>CROSS</b>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.5.3.11 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	READY		Write '1' to disable interrupt for event <b>READY</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW	DOWN		Write '1' to disable interrupt for event <b>DOWN</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW	UP		Write '1' to disable interrupt for event <b>UP</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											D	C	B	A		
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
D	RW CROSS			Write '1' to disable interrupt for event CROSS																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.5.3.12 RESULT

Address offset: 0x400

Compare result

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A					
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	R RESULT			Result of last compare. Decision point SAMPLE task.																												
		Below	0	Input voltage is below the threshold (VIN+ < VIN-)																												
		Above	1	Input voltage is above the threshold (VIN+ > VIN-)																												

### 6.5.3.13 ENABLE

Address offset: 0x500

COMP enable

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A				
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW ENABLE			Enable or disable COMP																												
		Disabled	0	Disable																												
		Enabled	2	Enable																												

### 6.5.3.14 PSEL

Address offset: 0x504

Pin select

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A			
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW PSEL			Analog pin select																												
		AnalogInput0	0	AIN0 selected as analog input																												
		AnalogInput1	1	AIN1 selected as analog input																												
		AnalogInput2	2	AIN2 selected as analog input																												
		AnalogInput3	3	AIN3 selected as analog input																												
		VddhDiv5	7	VDDH/5 selected as analog input																												



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																										A	A				
Reset	0x00000000																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	SP			Speed and power modes																											
			Low	0	Low-power mode																											
			Normal	1	Normal mode																											
			High	2	High-speed mode																											
B	RW	MAIN			Main operation modes																											
			SE	0	Single-ended mode																											
			Diff	1	Differential mode																											

### 6.5.3.19 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
Reset	0x00000000																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	HYST			Comparator hysteresis																											
			NoHyst	0	Comparator hysteresis disabled																											
			Hyst50mV	1	Comparator hysteresis enabled																											

## 6.5.4 Electrical specification

### 6.5.4.1 COMP Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{PROPDLY,LP}}$	Propagation delay, low-power mode <sup>11</sup>		0.6		$\mu\text{s}$
$t_{\text{PROPDLY,N}}$	Propagation delay, normal mode <sup>11</sup>		0.2		$\mu\text{s}$
$t_{\text{PROPDLY,HS}}$	Propagation delay, high-speed mode <sup>11</sup>		0.1		$\mu\text{s}$
$V_{\text{DIFFHYST}}$	Optional hysteresis applied to differential input	2	30	90	mV
$V_{\text{VDD-VREF}}$	Required difference between VDD and a selected VREF, VDD > VREF	0.3			V
$t_{\text{INT\_REF,START}}$	Startup time for the internal bandgap reference		50	80	$\mu\text{s}$
$E_{\text{INT\_REF}}$	Internal bandgap reference error	-3		3	%
$E_{\text{VDDH\_DIV5}}$	VddhDiv5 resistor ladder tolerance		$\pm 1$		%
$V_{\text{INPUTOFFSET}}$	Input offset	-15		15	mV
$t_{\text{COMP,START}}$	Startup time for the comparator core		3		$\mu\text{s}$

## 6.6 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

<sup>11</sup> Propagation delay is with 10 mV overdrive.



AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks, and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

### 6.6.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority, and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

### 6.6.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

### 6.6.3 ECB data structure

Block encrypt input and output is stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block

Table 34: ECB data structure overview

### 6.6.4 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000E000	ECB	ECB	AES electronic code book (ECB) mode block encryption	

Table 35: Instances

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

Table 36: Register overview

### 6.6.4.1 TASKS\_STARTECB

Address offset: 0x000

Start ECB block encrypt

If a crypto operation is already running in the AES core, the STARTECB task will not start a new encryption and an ERRORECB event will be triggered.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A					
Reset 0x00000000	0 0																															
ID	Acce	Field	Value	ID	Value	Description																										
A	W	TASKS_STARTECB				Start ECB block encrypt																										
			Trigger	1		If a crypto operation is already running in the AES core, the STARTECB task will not start a new encryption and an ERRORECB event will be triggered. Trigger task																										

### 6.6.4.2 TASKS\_STOPECB

Address offset: 0x004

Abort a possible executing ECB operation

If a running ECB operation is aborted by STOPECB, the ERRORECB event is triggered.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A					
Reset 0x00000000	0 0																															
ID	Acce	Field	Value	ID	Value	Description																										
A	W	TASKS_STOPECB				Abort a possible executing ECB operation																										
			Trigger	1		If a running ECB operation is aborted by STOPECB, the ERRORECB event is triggered. Trigger task																										

### 6.6.4.3 EVENTS\_ENDECB

Address offset: 0x100

ECB block encrypt complete

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ENDECB		ECB block encrypt complete																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

#### 6.6.4.4 EVENTS\_ERRORECB

Address offset: 0x104

ECB block encrypt aborted because of a STOPECB task or due to an error

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ERRORECB		ECB block encrypt aborted because of a STOPECB task or due to an error																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

#### 6.6.4.5 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															B	A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	ENDECB		Write '1' to enable interrupt for event ENDECB																												
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
	Enabled	1	Read: Enabled																													
B	RW	ERRORECB		Write '1' to enable interrupt for event ERRORECB																												
			Set	1	Enable																											
			Disabled	0	Read: Disabled																											
	Enabled	1	Read: Enabled																													

#### 6.6.4.6 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															B	A
Reset	0x00000000																															
0	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ENDECB			Write '1' to disable interrupt for event <a href="#">ENDECB</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW ERRORECB			Write '1' to disable interrupt for event <a href="#">ERRORECB</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.6.4.7 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A																														A	A
Reset	0x00000000																															
0	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ECBDATAPTR			Pointer to the ECB data structure (see Table 1 ECB data structure overview)																												

## 6.6.5 Electrical specification

### 6.6.5.1 ECB Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{ECB}$	Run time per 16 byte block in all modes			7.2	$\mu$ s

## 6.7 EGU — Event generator unit

Event generator unit (EGU) provides support for interlayer signaling. This means providing support for atomic triggering of both CPU execution and hardware tasks, from both firmware (by CPU) and hardware (by PPI). This feature can be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's interrupt service routine (ISR) execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Software-enabled interrupt triggering
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of EGU implements a set of tasks which can individually be triggered to generate the corresponding event. For example, the corresponding event for `TASKS_TRIGGER[n]` is `EVENTS_TRIGGERED[n]`. See [Instances](#) on page 125 for a list of EGU instances.

## 6.7.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event generator unit 0	
0x40015000	EGU	EGU1	Event generator unit 1	
0x40016000	EGU	EGU2	Event generator unit 2	
0x40017000	EGU	EGU3	Event generator unit 3	
0x40018000	EGU	EGU4	Event generator unit 4	
0x40019000	EGU	EGU5	Event generator unit 5	

Table 37: Instances

Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task
EVENTS_TRIGGERED[5]	0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED[6]	0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERED[7]	0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED[8]	0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED[9]	0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED[10]	0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERED[11]	0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED[12]	0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED[13]	0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED[14]	0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED[15]	0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

Table 38: Register overview

### 6.7.1.1 TASKS\_TRIGGER[n] (n=0..15)

Address offset: 0x000 + (n × 0x4)

Trigger n for triggering the corresponding TRIGGERED[n] event

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_TRIGGER			Trigger n for triggering the corresponding TRIGGERED[n] event																											
		Trigger	1	Trigger task																											

### 6.7.1.2 EVENTS\_TRIGGERED[n] (n=0..15)

Address offset: 0x100 + (n × 0x4)

Event number n generated by triggering the corresponding TRIGGER[n] task

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_TRIGGERED			Event number n generated by triggering the corresponding TRIGGER[n] task																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.7.1.3 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																P O N M L K J I H G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A-P	RW TRIGGERED[i] (i=0..15)			Enable or disable interrupt for event TRIGGERED[i]																											
		Disabled	0	Disable																											
		Enabled	1	Enable																											

### 6.7.1.4 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																P O N M L K J I H G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A-P	RW TRIGGERED[i] (i=0..15)			Write '1' to enable interrupt for event TRIGGERED[i]																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.7.1.5 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																	
ID																	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A																	
Reset 0x00000000																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value	ID	Value	Description																																											
A-P	RW	TRIGGERED[i] (i=0..15)				Write '1' to disable interrupt for event TRIGGERED[i]																																											
			Clear	1		Disable																																											
			Disabled	0		Read: Disabled																																											
			Enabled	1		Read: Enabled																																											

## 6.7.2 Electrical specification

### 6.7.2.1 EGU Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{EGU,EVT}}$	Latency between setting an EGU event flag and the system setting an interrupt		1		cycles

## 6.8 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports, with each port having up to 32 GPIOs.

The number of ports and GPIOs per port varies with product variant and package. Refer to [Registers](#) on page 130 and [Pin assignments](#) on page 415 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through the PPI and GPIOTE channels
- Any pin can be mapped to a peripheral for layout flexibility
- GPIO state changes captured on the SENSE signal can be stored by the LATCH register

The GPIO port peripheral implements up to 32 pins,  $\text{PIN}_0$  through  $\text{PIN}_{31}$ . Each of these pins can be individually configured in the  $\text{PIN\_CNF}[n]$  registers ( $n=0..31$ ).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect

- Analog input (for selected pins)

The PIN\_CNF registers are retained registers. See [POWER — Power supply](#) on page 49 for more information about retained registers.

### 6.8.1 Pin configuration

Pins can be individually configured through the SENSE field in the PIN\_CNF[n] register to detect either a high or low level input.

When the correct level is detected on a configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal. Default behavior, defined by the DETECTMODE register, combines all DETECT signals from the pins in the GPIO port into one common DETECT signal and routes it through the system to be utilized by other peripherals. This mechanism is functional in both System ON and System OFF mode. See [GPIO port and the GPIO pin details](#) on page 128.

The following figure illustrates the GPIO port containing 32 individual pins, where PIN0 is shown in more detail for reference. All signals on the left side of the illustration are used by other peripherals in the system and therefore not directly available to the CPU.

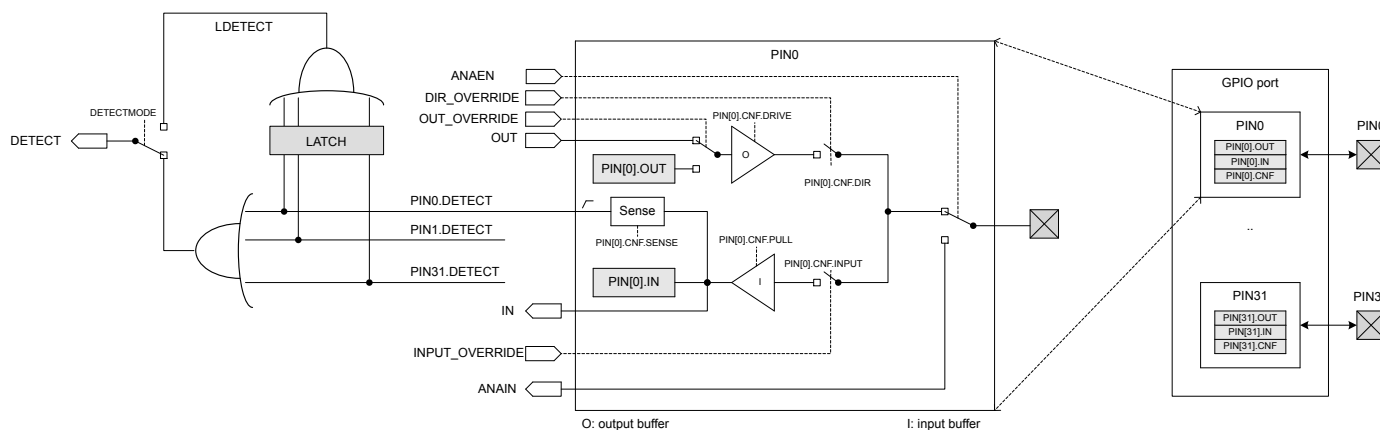


Figure 42: GPIO port and the GPIO pin details

Pins should be in a level that cannot trigger the sense mechanism before being enabled. If the SENSE condition configured in the PIN\_CNF registers is met when the sense mechanism is enabled, the DETECT signal will immediately go high. A PORT event is triggered if the DETECT signal was low before enabling the sense mechanism. See [GPIOTE — GPIO tasks and events](#) on page 135.

See the following peripherals for more information about how the DETECT signal is used:

- [POWER — Power supply](#) on page 49 - uses the DETECT signal to exit from System OFF mode.
- [GPIOTE — GPIO tasks and events](#) on page 135 - uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag is set in the LATCH register. For example, when the PIN0.DETECT signal goes high, bit 0 in the LATCH register is set to 1. If the CPU performs a clear operation on a bit in the LATCH register, when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared. The LATCH register will only be cleared if the CPU explicitly clears it by writing a 1 to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

The LDETECT signal will be set high when one or more bits in the LATCH register are 1. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to 0.

If one or more bits in the LATCH register are 1 after the CPU has performed a clear operation on the LATCH register, a rising edge will be generated on the LDETECT signal. This is illustrated in [DETECT signal behavior](#) on page 129.



**Note:** The CPU can read the LATCH register at any time to check if a SENSE condition has been met on any of the GPIO pins. This is still valid if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register. It is possible to change from default behavior to the DETECT signal that is derived directly from the LDETECT signal. See [GPIO port and the GPIO pin details](#) on page 128. The following figure illustrates the DETECT signal behavior for these two alternatives.

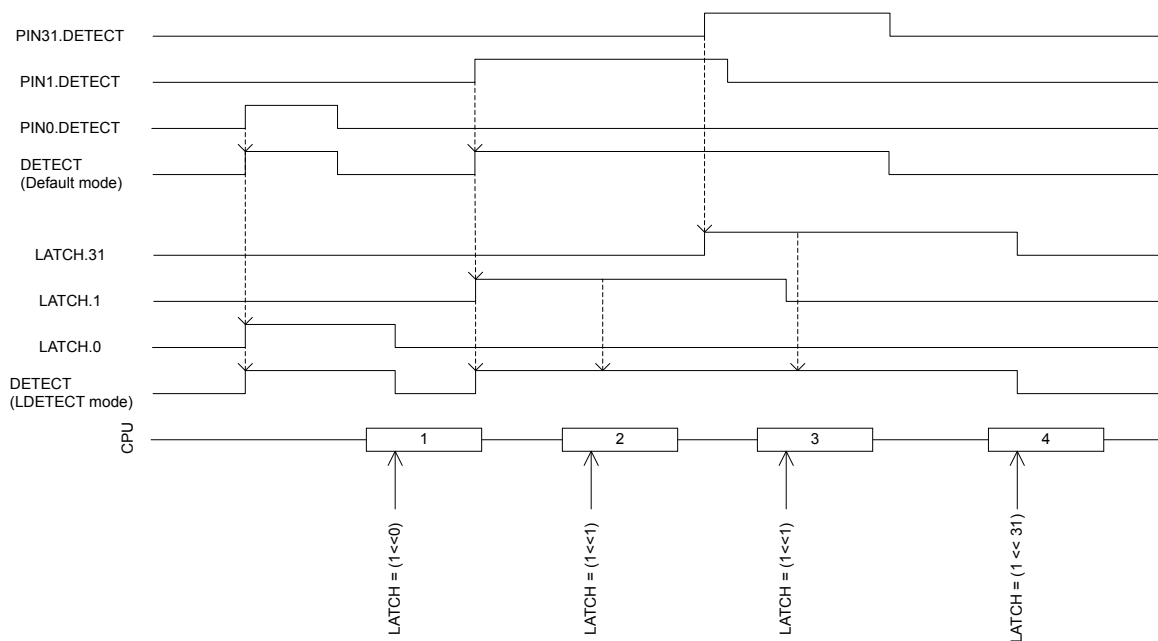


Figure 43: DETECT signal behavior

A GPIO pin input buffer can be disconnected from the pin to enable power savings when the pin is not used as an input, see [GPIO port and the GPIO pin details](#) on page 128. Input buffers must be connected to get a valid input value in the IN register, and for the sense mechanism to get access to the pin.

Other peripherals in the system can connect to GPIO pins and override their output value and configuration, or read their analog or digital input value. See [GPIO port and the GPIO pin details](#) on page 128.

Selected pins also support analog input signals, see ANAIN in [GPIO port and the GPIO pin details](#) on page 128. The assignment of the analog pins can be found in [Pin assignments](#) on page 415.

**Note:** When a pin is configured as digital input, increased current consumption occurs when the input voltage is between  $V_{IL}$  and  $V_{IH}$ . It is good practice to ensure that the external circuitry does not drive that pin to levels between  $V_{IL}$  and  $V_{IH}$  for a long period of time.

## 6.8.2 Registers

Base address	Peripheral	Instance	Description	Configuration
0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
0x50000000	GPIO	P0	General purpose input and output, port 0.	P0.00 - P0.08, P0.14 - P0.18, P0.20, and P0.28 - P0.30 implemented

Table 39: Instances

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers
DETECTMODE	0x524	Select between default DETECT signal behavior and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins

Register	Offset	Description
PIN_CNF[31]	0x77C	Configuration of GPIO pins

Table 40: Register overview

### 6.8.2.1 OUT

Address offset: 0x504

Write GPIO port

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A-f	RW PIN[i] (i=0..31)			Pin i																												
		Low	0	Pin driver is low																												
		High	1	Pin driver is high																												

### 6.8.2.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A-f	RW PIN[i] (i=0..31)			Pin i																												
		Low	0	Read: pin driver is low																												
		High	1	Read: pin driver is high																												
		Set	1	Write: a '1' sets the pin high; a '0' has no effect																												

### 6.8.2.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port

Read: reads value of OUT register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A-f	RW PIN[i] (i=0..31)			Pin i																												
		Low	0	Read: pin driver is low																												
		High	1	Read: pin driver is high																												
		Clear	1	Write: a '1' sets the pin low; a '0' has no effect																												

### 6.8.2.4 IN

Address offset: 0x510

## Read GPIO port

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A-f	R	PIN[i] (i=0..31)		Pin i																												
		Low	0	Pin input is low																												
		High	1	Pin input is high																												

## 6.8.2.5 DIR

Address offset: 0x514

Direction of GPIO pins

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A-f	RW	PIN[i] (i=0..31)		Pin i																												
		Input	0	Pin set as input																												
		Output	1	Pin set as output																												

## 6.8.2.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A-f	RW	PIN[i] (i=0..31)		Set as output pin i																												
		Input	0	Read: pin set as input																												
		Output	1	Read: pin set as output																												
		Set	1	Write: a '1' sets pin to output; a '0' has no effect																												

## 6.8.2.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																									
ID																E	E				D	D	D																C	C	B	A
<b>Reset 0x00000002</b>	<b>0 1 0</b>																																									
ID	Acce Field	Value ID	Value	Description																																						
C	RW PULL	Disabled	0	Pull configuration No pull																																						
		Pulldown	1	Pull down on pin																																						
		Pullup	3	Pull up on pin																																						
D	RW DRIVE	S0S1	0	Drive configuration Standard '0', standard '1'																																						
		H0S1	1	High drive '0', standard '1'																																						
		S0H1	2	Standard '0', high drive '1'																																						
		H0H1	3	High drive '0', high 'drive '1''																																						
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or connections)																																						
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)																																						
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and connections)																																						
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and connections)																																						
E	RW SENSE	Disabled	0	Pin sensing mechanism Disabled																																						
		High	2	Sense for high level																																						
		Low	3	Sense for low level																																						

## 6.8.3 Electrical specification

### 6.8.3.1 GPIO Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input high voltage	0.7 x VDD		VDD	V
V <sub>IL</sub>	Input low voltage	VSS		0.3 x VDD	V
V <sub>OH,SD</sub>	Output high voltage, standard drive, 0.5 mA, VDD ≥ 1.7	VDD - 0.4		VDD	V
V <sub>OH,HDH</sub>	Output high voltage, high drive, 5 mA, VDD ≥ 2.7 V	VDD - 0.4		VDD	V
V <sub>OH,HDL</sub>	Output high voltage, high drive, 3 mA, VDD ≥ 1.7 V	VDD - 0.4		VDD	V
V <sub>OL,SD</sub>	Output low voltage, standard drive, 0.5 mA, VDD ≥ 1.7	VSS		VSS + 0.4	V
V <sub>OL,HDH</sub>	Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V	VSS		VSS + 0.4	V
V <sub>OL,HDL</sub>	Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V	VSS		VSS + 0.4	V
I <sub>OL,SD</sub>	Current at VSS+0.4 V, output set low, standard drive, VDD ≥ 1.7	1	2	4	mA
I <sub>OL,HDH</sub>	Current at VSS+0.4 V, output set low, high drive, VDD ≥ 2.7 V	6	10	15	mA
I <sub>OL,HDL</sub>	Current at VSS+0.4 V, output set low, high drive, VDD ≥ 1.7 V	3			mA
I <sub>OH,SD</sub>	Current at VDD-0.4 V, output set high, standard drive, VDD ≥ 1.7	1	2	4	mA
I <sub>OH,HDH</sub>	Current at VDD-0.4 V, output set high, high drive, VDD ≥ 2.7 V	6	9	14	mA
I <sub>OH,HDL</sub>	Current at VDD-0.4 V, output set high, high drive, VDD ≥ 1.7 V	3			mA

Symbol	Description	Min.	Typ.	Max.	Units
$t_{RF,15pF}$	Rise/fall time, standard drive mode, 10-90%, 15 pF load <sup>12</sup>		9		ns
$t_{RF,25pF}$	Rise/fall time, standard drive mode, 10-90%, 25 pF load <sup>12</sup>		13		ns
$t_{RF,50pF}$	Rise/fall time, standard drive mode, 10-90%, 50 pF load <sup>12</sup>		25		ns
$t_{HRF,15pF}$	Rise/Fall time, high drive mode, 10-90%, 15 pF load <sup>12</sup>		4		ns
$t_{HRF,25pF}$	Rise/Fall time, high drive mode, 10-90%, 25 pF load <sup>12</sup>		5		ns
$t_{HRF,50pF}$	Rise/Fall time, high drive mode, 10-90%, 50 pF load <sup>12</sup>		8		ns
$R_{PU}$	Pull-up resistance	11	13	16	k $\Omega$
$R_{PD}$	Pull-down resistance	11	13	16	k $\Omega$
$C_{PAD}$	Pad capacitance		3		pF

## 6.9 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Tasks and events are briefly introduced in [Peripheral interface](#) on page 85, and GPIO is described in more detail in [GPIO — General purpose input/output](#) on page 127.

Low power detection of pin state changes is possible when in System ON or System OFF.

Instance	Number of GPIOTE channels
GPIOTE	8

Table 41: GPIOTE properties

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change

### 6.9.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks SET[n], CLR[n], and OUT[n] can write to individual pins, and events IN[n] can be generated from input changes of individual pins.

The SET task will set the pin selected in GPIOTE.CONFIG[n].PSEL to high. The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY. It can set the pin high, set it low, or toggle it.

<sup>12</sup> Rise and fall times based on simulations

Tasks and events are configured using the CONFIG[n] registers. One CONFIG[n] register is associated with a set of SET[n], CLR[n], and OUT[n] tasks and IN[n] events.

As long as a SET[n], CLR[n], and OUT[n] task or an IN[n] event is configured to control pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value, as specified in the GPIO, will be ignored as long as the pin is controlled by GPIOTE. Attempting to write to the pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, the associated pin gets the output and configuration values specified in the GPIO module, see MODE field in CONFIG[n] register.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the priority of the tasks is as described in the following table.

Priority	Task
1	OUT
2	CLR
3	SET

Table 42: Task priorities

When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, based on the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

## 6.9.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See [GPIO — General purpose input/output](#) on page 127 for more information about the DETECT signal.

The GPIO DETECT signal will not wake the system up again if the system is put into System ON IDLE while the DETECT signal is high. Clear all DETECT sources before entering sleep. If the LATCH register is used as a source, a new rising edge will be generated on DETECT if any bit in LATCH is still high after clearing all or part of the register. This could occur if one of the PINx.DETECT signals is still high, for example. See [Pin configuration](#) on page 128 for more information.

Setting the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled even if the peripheral itself appears to be IDLE, meaning no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON when all peripherals and the CPU are idle, meaning the lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the following must be performed:

1. Disable interrupts on the PORT event (through INTENCLR.PORT).
2. Configure the sources (PIN\_CNF[n].SENSE).
3. Clear any potential event that could have occurred during configuration (write '0' to EVENTS\_PORT).
4. Enable interrupts (through INTENSET.PORT).

## 6.9.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE,



the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

**Note:** A pin can only be assigned to one GPIOTE channel at a time. Failing to do so may result in unpredictable behavior.

## 6.9.4 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	

Table 43: Instances

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in CONFIG[1].POLARITY.
TASKS_OUT[2]	0x008	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in CONFIG[2].POLARITY.
TASKS_OUT[3]	0x00C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in CONFIG[3].POLARITY.
TASKS_OUT[4]	0x010	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is configured in CONFIG[4].POLARITY.
TASKS_OUT[5]	0x014	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is configured in CONFIG[5].POLARITY.
TASKS_OUT[6]	0x018	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is configured in CONFIG[6].POLARITY.
TASKS_OUT[7]	0x01C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is configured in CONFIG[7].POLARITY.
TASKS_SET[0]	0x030	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it high.
TASKS_SET[1]	0x034	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it high.
TASKS_SET[2]	0x038	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high.
TASKS_SET[3]	0x03C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high.
TASKS_SET[4]	0x040	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high.
TASKS_SET[5]	0x044	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high.
TASKS_SET[6]	0x048	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_SET[7]	0x04C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high.
TASKS_CLR[0]	0x060	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[1]	0x064	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[1]	0x104	Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[5]	0x114	Event generated from pin specified in CONFIG[5].PSEL

Register	Offset	Description
EVENTS_IN[6]	0x118	Event generated from pin specified in CONFIG[6].PSEL
EVENTS_IN[7]	0x11C	Event generated from pin specified in CONFIG[7].PSEL
EVENTS_PORT	0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG[0]	0x510	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[1]	0x514	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[2]	0x518	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[3]	0x51C	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[4]	0x520	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[5]	0x524	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[6]	0x528	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event
CONFIG[7]	0x52C	Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event

Table 44: Register overview

### 6.9.4.1 TASKS\_OUT[n] (n=0..7)

Address offset:  $0x000 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value	ID	Value	Description																										
A	W	TASKS_OUT				Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.																										
			Trigger		1	Trigger task																										

### 6.9.4.2 TASKS\_SET[n] (n=0..7)

Address offset:  $0x030 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value	ID	Value	Description																										
A	W	TASKS_SET				Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.																										
			Trigger		1	Trigger task																										

### 6.9.4.3 TASKS\_CLR[n] (n=0..7)

Address offset:  $0x060 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_CLR		Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.																												
		Trigger	1	Trigger task																												

#### 6.9.4.4 EVENTS\_IN[n] (n=0..7)

Address offset: 0x100 + (n × 0x4)

Event generated from pin specified in CONFIG[n].PSEL

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_IN		Event generated from pin specified in CONFIG[n].PSEL																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

#### 6.9.4.5 EVENTS\_PORT

Address offset: 0x17C

Event generated from multiple input GPIO pins with SENSE mechanism enabled

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_PORT		Event generated from multiple input GPIO pins with SENSE mechanism enabled																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

#### 6.9.4.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
ID	I																										H G F E D C B A									
Reset 0x00000000	0 0																																			
ID	Acce Field	Value ID	Value	Description																																
A-H	RW	IN[i] (i=0..7)		Write '1' to enable interrupt for event IN[i]																																
		Set	1	Enable																																
		Disabled	0	Read: Disabled																																
		Enabled	1	Read: Enabled																																
I	RW	PORT		Write '1' to enable interrupt for event PORT																																
		Set	1	Enable																																
		Disabled	0	Read: Disabled																																
		Enabled	1	Read: Enabled																																

### 6.9.4.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	I															H G F E D C B A															
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A-H	RW IN[i] (i=0..7)			Write '1' to disable interrupt for event IN[i]																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
I	RW PORT			Write '1' to disable interrupt for event PORT																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.9.4.8 CONFIG[n] (n=0..7)

Address offset: 0x510 + (n × 0x4)

Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																E D D B B B B B A A															
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW MODE			Mode																											
		Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.																											
		Event	1	Event mode  The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.																											
		Task	3	Task mode  The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.																											
B	RW PSEL		[0..31]	GPIO number associated with SET[n], CLR[n], and OUT[n] tasks and IN[n] event																											
D	RW POLARITY			When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.																											
		None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.																											
		LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.																											
		HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																				
ID																E	D	D	B				B	B	B											A	A
Reset	0x00000000																																				
ID	Acces	Field	Value ID	Value	Description																																
			Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.																																
E	RW	OUTINIT			When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.																																
			Low	0	Task mode: Initial value of pin before task triggering is low																																
			High	1	Task mode: Initial value of pin before task triggering is high																																

### 6.9.5 Electrical specification

## 6.10 PPI – Programmable peripheral interconnect

The programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

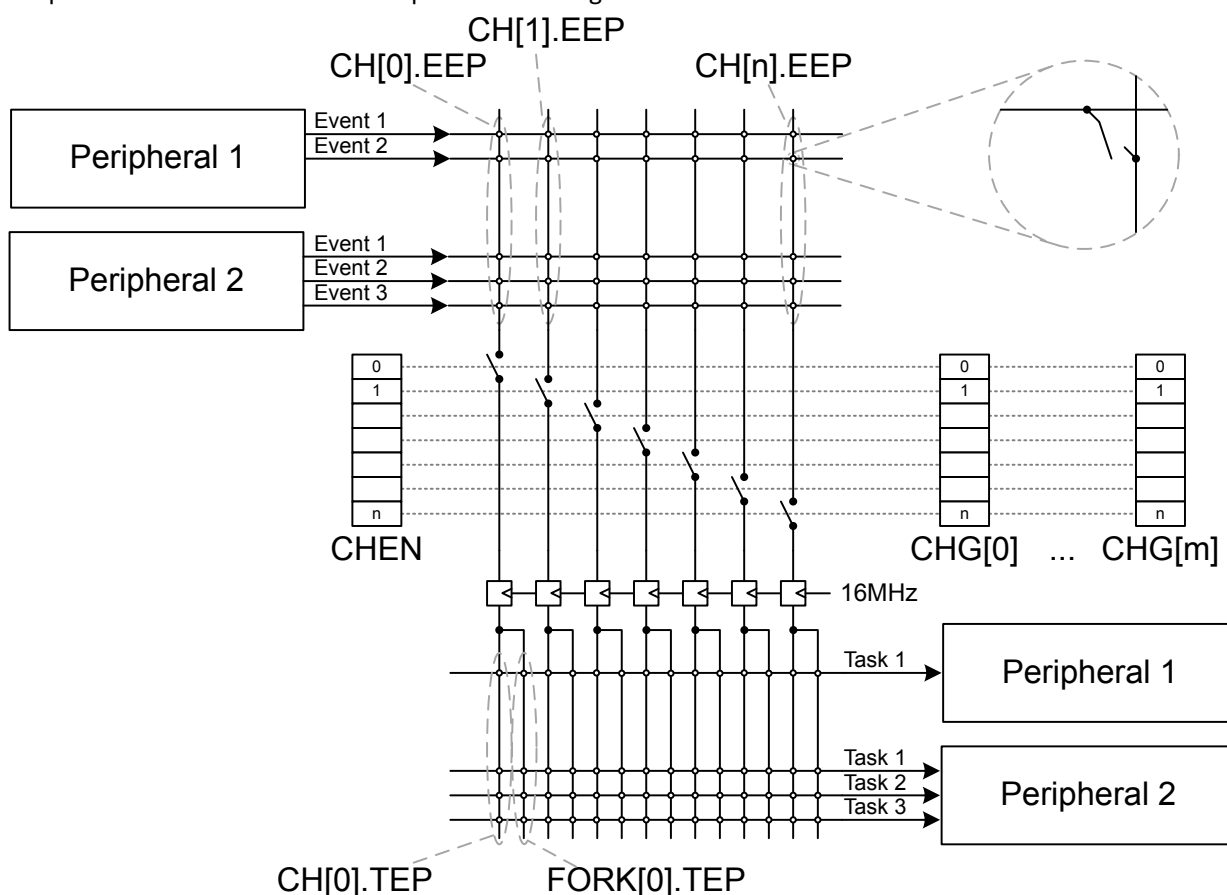


Figure 44: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups (see CHG[n] registers), in the same way as ordinary PPI channels.

Instance	Channel	Number of channels
PPI	0-19	20
PPI (fixed)	20-31	12

Table 45: Configurable and fixed PPI channels

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP, and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.

**Note:** Shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks. Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belong to which groups.

**Note:** When a channel belongs to two groups m and n, and the tasks CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), the CHG[m].EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

### 6.10.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the following table.

Channel	EEP	TEP
20	TIMER0->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMER0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMER0->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMER0->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMER0->TASKS_CAPTURE[2]
28	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTC0->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTC0->EVENTS_COMPARE[0]	TIMER0->TASKS_CLEAR
31	RTC0->EVENTS_COMPARE[0]	TIMER0->TASKS_START

Table 46: Pre-programmed channels

## 6.10.2 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	Programmable peripheral interconnect	

Table 47: Instances

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event endpoint
CH[0].TEP	0x514	Channel 0 task endpoint
CH[1].EEP	0x518	Channel 1 event endpoint
CH[1].TEP	0x51C	Channel 1 task endpoint
CH[2].EEP	0x520	Channel 2 event endpoint
CH[2].TEP	0x524	Channel 2 task endpoint
CH[3].EEP	0x528	Channel 3 event endpoint
CH[3].TEP	0x52C	Channel 3 task endpoint
CH[4].EEP	0x530	Channel 4 event endpoint
CH[4].TEP	0x534	Channel 4 task endpoint
CH[5].EEP	0x538	Channel 5 event endpoint
CH[5].TEP	0x53C	Channel 5 task endpoint
CH[6].EEP	0x540	Channel 6 event endpoint
CH[6].TEP	0x544	Channel 6 task endpoint

Register	Offset	Description
CH[7].EEP	0x548	Channel 7 event endpoint
CH[7].TEP	0x54C	Channel 7 task endpoint
CH[8].EEP	0x550	Channel 8 event endpoint
CH[8].TEP	0x554	Channel 8 task endpoint
CH[9].EEP	0x558	Channel 9 event endpoint
CH[9].TEP	0x55C	Channel 9 task endpoint
CH[10].EEP	0x560	Channel 10 event endpoint
CH[10].TEP	0x564	Channel 10 task endpoint
CH[11].EEP	0x568	Channel 11 event endpoint
CH[11].TEP	0x56C	Channel 11 task endpoint
CH[12].EEP	0x570	Channel 12 event endpoint
CH[12].TEP	0x574	Channel 12 task endpoint
CH[13].EEP	0x578	Channel 13 event endpoint
CH[13].TEP	0x57C	Channel 13 task endpoint
CH[14].EEP	0x580	Channel 14 event endpoint
CH[14].TEP	0x584	Channel 14 task endpoint
CH[15].EEP	0x588	Channel 15 event endpoint
CH[15].TEP	0x58C	Channel 15 task endpoint
CH[16].EEP	0x590	Channel 16 event endpoint
CH[16].TEP	0x594	Channel 16 task endpoint
CH[17].EEP	0x598	Channel 17 event endpoint
CH[17].TEP	0x59C	Channel 17 task endpoint
CH[18].EEP	0x5A0	Channel 18 event endpoint
CH[18].TEP	0x5A4	Channel 18 task endpoint
CH[19].EEP	0x5A8	Channel 19 event endpoint
CH[19].TEP	0x5AC	Channel 19 task endpoint
CHG[0]	0x800	Channel group 0
CHG[1]	0x804	Channel group 1
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 3
CHG[4]	0x810	Channel group 4
CHG[5]	0x814	Channel group 5
FORK[0].TEP	0x910	Channel 0 task endpoint
FORK[1].TEP	0x914	Channel 1 task endpoint
FORK[2].TEP	0x918	Channel 2 task endpoint
FORK[3].TEP	0x91C	Channel 3 task endpoint
FORK[4].TEP	0x920	Channel 4 task endpoint
FORK[5].TEP	0x924	Channel 5 task endpoint
FORK[6].TEP	0x928	Channel 6 task endpoint
FORK[7].TEP	0x92C	Channel 7 task endpoint
FORK[8].TEP	0x930	Channel 8 task endpoint
FORK[9].TEP	0x934	Channel 9 task endpoint
FORK[10].TEP	0x938	Channel 10 task endpoint
FORK[11].TEP	0x93C	Channel 11 task endpoint
FORK[12].TEP	0x940	Channel 12 task endpoint
FORK[13].TEP	0x944	Channel 13 task endpoint
FORK[14].TEP	0x948	Channel 14 task endpoint
FORK[15].TEP	0x94C	Channel 15 task endpoint
FORK[16].TEP	0x950	Channel 16 task endpoint
FORK[17].TEP	0x954	Channel 17 task endpoint
FORK[18].TEP	0x958	Channel 18 task endpoint
FORK[19].TEP	0x95C	Channel 19 task endpoint
FORK[20].TEP	0x960	Channel 20 task endpoint



Register	Offset	Description
FORK[21].TEP	0x964	Channel 21 task endpoint
FORK[22].TEP	0x968	Channel 22 task endpoint
FORK[23].TEP	0x96C	Channel 23 task endpoint
FORK[24].TEP	0x970	Channel 24 task endpoint
FORK[25].TEP	0x974	Channel 25 task endpoint
FORK[26].TEP	0x978	Channel 26 task endpoint
FORK[27].TEP	0x97C	Channel 27 task endpoint
FORK[28].TEP	0x980	Channel 28 task endpoint
FORK[29].TEP	0x984	Channel 29 task endpoint
FORK[30].TEP	0x988	Channel 30 task endpoint
FORK[31].TEP	0x98C	Channel 31 task endpoint

Table 48: Register overview

### 6.10.2.1 TASKS\_CHG[n].EN (n=0..5)

Address offset:  $0x000 + (n \times 0x8)$

Enable channel group n

Bit number																															
ID	A																														
Reset	0x00000000																														
ID	Acce Field	Value ID	Value	Description																											
A	W EN	Trigger	1	Enable channel group n Trigger task																											

### 6.10.2.2 TASKS\_CHG[n].DIS (n=0..5)

Address offset:  $0x004 + (n \times 0x8)$

Disable channel group n

Bit number																															
ID	A																														
Reset	0x00000000																														
ID	Acce Field	Value ID	Value	Description																											
A	W DIS	Trigger	1	Disable channel group n Trigger task																											

### 6.10.2.3 CHEN

Address offset: 0x500

Channel enable register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A-T	RW CH[i] (i=0..19)	Disabled	0	Enable or disable channel i Disable channel																												
		Enabled	1	Enable channel																												
U-f	RW CH[i] (i=20..31)	Disabled	0	Enable or disable channel i Disable channel																												
		Enabled	1	Enable channel																												

### 6.10.2.4 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A-T	RW CH[i] (i=0..19)	Disabled	0	Channel i enable set register. Writing '0' has no effect. Read: channel disabled																												
		Enabled	1	Read: channel enabled																												
		Set	1	Write: Enable channel																												
U-f	RW CH[i] (i=20..31)	Disabled	0	Channel i enable set register. Writing '0' has no effect. Read: channel disabled																												
		Enabled	1	Read: channel enabled																												
		Set	1	Write: Enable channel																												

### 6.10.2.5 CHENCLR

Address offset: 0x508

Channel enable clear register

Read: reads value of CH{i} field in CHEN register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A-T	RW CH[i] (i=0..19)	Disabled	0	Channel i enable clear register. Writing '0' has no effect. Read: channel disabled																												
		Enabled	1	Read: channel enabled																												
		Clear	1	Write: disable channel																												
U-f	RW CH[i] (i=20..31)	Disabled	0	Channel i enable clear register. Writing '0' has no effect. Read: channel disabled																												
		Enabled	1	Read: channel enabled																												
		Clear	1	Write: disable channel																												

### 6.10.2.6 CH[n].EEP (n=0..19)

Address offset: 0x510 + (n × 0x8)

## Channel n event endpoint

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EEP			Pointer to event register. Accepts only addresses to registers from the Event group.																												

## 6.10.2.7 CH[n].TEP (n=0..19)

Address offset: 0x514 + (n × 0x8)

## Channel n task endpoint

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW TEP			Pointer to task register. Accepts only addresses to registers from the Task group.																												

## 6.10.2.8 CHG[n] (n=0..5)

Address offset: 0x800 + (n × 0x4)

## Channel group n

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A-T	RW CH[i] (i=0..19)			Include or exclude channel i																												
		Excluded	0	Exclude																												
		Included	1	Include																												
U-f	RW CH[i] (i=20..31)			Include or exclude channel i																												
		Excluded	0	Exclude																												
		Included	1	Include																												

## 6.10.2.9 FORK[n].TEP (n=0..19, 20..31)

Address offset: 0x910 + (n × 0x4)

## Channel n task endpoint

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW TEP			Pointer to task register																												

## 6.11 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

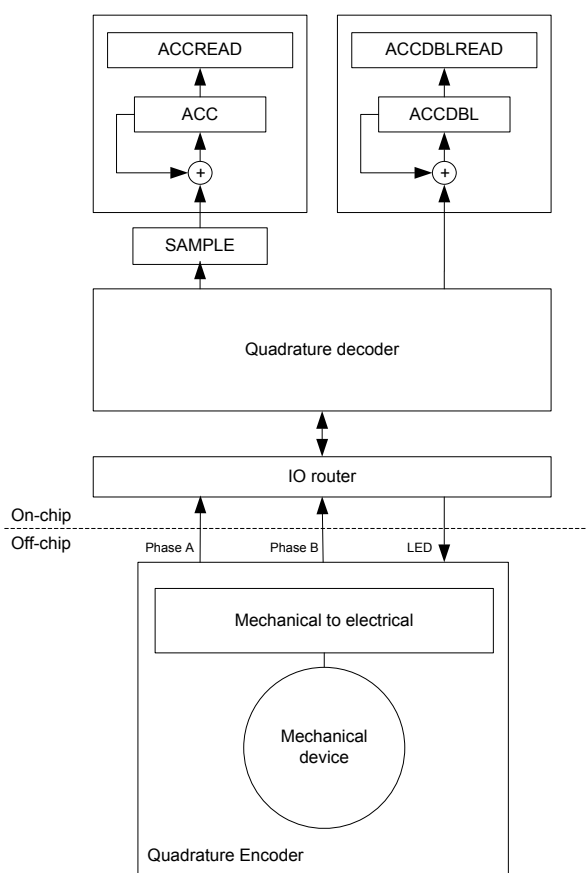


Figure 45: Quadrature decoder configuration

### 6.11.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by the waveform that changes level first. Invalid transitions may occur, meaning the two waveforms simultaneously switch. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.

The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behavior.

It is good practice to only change registers LEDPOL, REPORTPER, DBFEN, and LEDPRE when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Previous sample pair(n-1)		Current samples pair(n)		SAMPLE register	ACC operation	ACCDBL operation	Description
A	B	A	B				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

Table 49: Sampled value encoding

## 6.11.2 LED output

The LED output follows the sample period. The LED is switched on for a set period before sampling and then switched off immediately after. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

When using off-chip mechanical encoders not requiring an LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case, the QDEC will not acquire access to a pin for the LED output.

## 6.11.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register). The filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter. Any signal with a steady state shorter than SAMPLEPER will always

be suppressed by the filter. It is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.

When the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

### 6.11.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL. These registers accumulate valid motion sample values and the number of detected invalid samples (double transitions), respectively.

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register, the application can fetch data when necessary instead of reading all SAMPLE register output. The ACC register holds the relative movement of the external mechanical device from the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automated capture of multiple samples before sending an event. When a non-null displacement is captured and accumulated, a REPORTRDY event is sent. When one or more double-displacements are captured and accumulated, a DBLRDY event is sent. The REPORTPER field in this register determines how many samples must be accumulated before the contents are evaluated and a REPORTRDY or DBLRDY event is sent.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY\_RDCLRACC shortcut), ACCREAD can then be read.

When a double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY\_RDCLRDBL shortcut), ACCDBLREAD can then be read.

### 6.11.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

## 6.11.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in [GPIO configuration before enabling peripheral](#) on page 151 before enabling the QDEC. This configuration must be retained in the GPIO for the selected I/Os as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

QDEC signal	QDEC pin	Direction	Output value	Comment
Phase A	As specified in PSEL.A	Input	Not applicable	
Phase B	As specified in PSEL.B	Input	Not applicable	
LED	As specified in PSEL.LED	Input	Not applicable	

Table 50: GPIO configuration before enabling peripheral

## 6.11.7 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 51: Instances

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal

Register	Offset	Description
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDL	0x544	Register accumulating the number of detected double transitions
ACCDLREAD	0x548	Snapshot of the ACCDL, updated by the READCLRACC or RDCLRDBL task

Table 52: Register overview

### 6.11.7.1 TASKS\_START

Address offset: 0x000

Task starting the quadrature decoder

When started, the SAMPLE register will be continuously updated at the rate given in the SAMPLEPER register.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_START		Task starting the quadrature decoder																											
				When started, the SAMPLE register will be continuously updated at the rate given in the SAMPLEPER register.																											
		Trigger	1	Trigger task																											

### 6.11.7.2 TASKS\_STOP

Address offset: 0x004

Task stopping the quadrature decoder

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_STOP		Task stopping the quadrature decoder																											
		Trigger	1	Trigger task																											

### 6.11.7.3 TASKS\_READCLRACC

Address offset: 0x008

Read and clear ACC and ACCDL

Task transferring the content of ACC to ACCREAD and the content of ACCDL to ACCDLREAD, and then clearing the ACC and ACCDL registers. These read-and-clear operations will be done atomically.



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_READCLRACC		Read and clear ACC and ACCDBL																												
				Task transferring the content of ACC to ACCREAD and the content of ACCDBL to ACCDBLREAD, and then clearing the ACC and ACCDBL registers. These read-and-clear operations will be done atomically.																												
		Trigger	1	Trigger task																												

#### 6.11.7.4 TASKS\_RDCLRACC

Address offset: 0x00C

Read and clear ACC

Task transferring the content of ACC to ACCREAD, and then clearing the ACC register. This read-and-clear operation will be done atomically.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_RDCLRACC		Read and clear ACC																												
				Task transferring the content of ACC to ACCREAD, and then clearing the ACC register. This read-and-clear operation will be done atomically.																												
		Trigger	1	Trigger task																												

#### 6.11.7.5 TASKS\_RDCLRDBL

Address offset: 0x010

Read and clear ACCDBL

Task transferring the content of ACCDBL to ACCDBLREAD, and then clearing the ACCDBL register. This read-and-clear operation will be done atomically.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_RDCLRDBL		Read and clear ACCDBL																												
				Task transferring the content of ACCDBL to ACCDBLREAD, and then clearing the ACCDBL register. This read-and-clear operation will be done atomically.																												
		Trigger	1	Trigger task																												

#### 6.11.7.6 EVENTS\_SAMPLERDY

Address offset: 0x100

Event being generated for every new sample value written to the SAMPLE register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	RW	EVENTS_SAMPLERDY		Event being generated for every new sample value written to the SAMPLE register																													
		NotGenerated	0	Event not generated																													
		Generated	1	Event generated																													

### 6.11.7.7 EVENTS\_REPORTRDY

Address offset: 0x104

Non-null report ready

Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_REPORTRDY		Non-null report ready																												
		NotGenerated	0	Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).																												
		Generated	1	Event generated																												

### 6.11.7.8 EVENTS\_ACCOF

Address offset: 0x108

ACC or ACCDBL register overflow

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ACCOF		ACC or ACCDBL register overflow																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.11.7.9 EVENTS\_DBLRDY

Address offset: 0x10C

Double displacement(s) detected

Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_DBLRDY		Double displacement(s) detected																											
				Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.11.7.10 EVENTS\_STOPPED

Address offset: 0x110

QDEC has been stopped

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_STOPPED		QDEC has been stopped																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.11.7.11 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																													G F E D C B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	REPORTRDY_READCLRACC		Shortcut between event <a href="#">REPORTRDY</a> and task <a href="#">READCLRACC</a>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											
B	RW	SAMPLERDY_STOP		Shortcut between event <a href="#">SAMPLERDY</a> and task <a href="#">STOP</a>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											
C	RW	REPORTRDY_RDCLRACC		Shortcut between event <a href="#">REPORTRDY</a> and task <a href="#">RDCLRACC</a>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											
D	RW	REPORTRDY_STOP		Shortcut between event <a href="#">REPORTRDY</a> and task <a href="#">STOP</a>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											
E	RW	DBLRDY_RDCLRDBL		Shortcut between event <a href="#">DBLRDY</a> and task <a href="#">RDCLRDBL</a>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											
F	RW	DBLRDY_STOP		Shortcut between event <a href="#">DBLRDY</a> and task <a href="#">STOP</a>																											
		Disabled	0	Disable shortcut																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																				
ID																															G	F	E	D	C	B	A
<b>Reset 0x00000000</b>											0 0																										
ID	Acce Field	Value ID	Value	Description																																	
		Enabled	1	Enable shortcut																																	
G	RW SAMPLERDY_READCLRACC			Shortcut between event <a href="#">SAMPLERDY</a> and task <a href="#">READCLRACC</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	

### 6.11.7.12 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID																															E	D	C	B	A
<b>Reset 0x00000000</b>											0 0																								
ID	Acce Field	Value ID	Value	Description																															
A	RW SAMPLERDY			Write '1' to enable interrupt for event <a href="#">SAMPLERDY</a>																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
		Enabled	1	Read: Enabled																															
B	RW REPORTRDY			Write '1' to enable interrupt for event <a href="#">REPORTRDY</a>																															
				Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
		Enabled	1	Read: Enabled																															
C	RW ACCOF			Write '1' to enable interrupt for event <a href="#">ACCOF</a>																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
		Enabled	1	Read: Enabled																															
D	RW DBLRDY			Write '1' to enable interrupt for event <a href="#">DBLRDY</a>																															
				Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
		Enabled	1	Read: Enabled																															
E	RW STOPPED			Write '1' to enable interrupt for event <a href="#">STOPPED</a>																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
		Enabled	1	Read: Enabled																															

### 6.11.7.13 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															E D C B A
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW SAMPLERDY			Write '1' to disable interrupt for event <a href="#">SAMPLERDY</a>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		B	RW REPORTRDY			Write '1' to disable interrupt for event <a href="#">REPORTRDY</a>																									
						Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).																									
Clear	1			Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		C	RW ACCOF			Write '1' to disable interrupt for event <a href="#">ACCOF</a>																									
Clear	1			Disable																											
Disabled	0			Read: Disabled																											
		Enabled	1	Read: Enabled																											
		D	RW DBLRDY			Write '1' to disable interrupt for event <a href="#">DBLRDY</a>																									
						Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).																									
Clear	1			Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		E	RW STOPPED			Write '1' to disable interrupt for event <a href="#">STOPPED</a>																									
Clear	1			Disable																											
Disabled	0			Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.11.7.14 ENABLE

Address offset: 0x500

Enable the quadrature decoder

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															A
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW ENABLE			Enable or disable the quadrature decoder																											
				When enabled the decoder pins will be active. When disabled the quadrature decoder pins are not active and can be used as GPIO .																											
		Disabled	0	Disable																											
		Enabled	1	Enable																											

### 6.11.7.15 LEDPOL

Address offset: 0x504

LED output pin polarity

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW LEDPOL			LED output pin polarity																												
		ActiveLow	0	Led active on output pin low																												
		ActiveHigh	1	Led active on output pin high																												

### 6.11.7.16 SAMPLEPER

Address offset: 0x508

Sample period

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID																																A	A	A	A
Reset 0x00000000	0																																		
ID	Acce Field	Value ID	Value	Description																															
A	RW SAMPLEPER			Sample period. The SAMPLE register will be updated for every new sample																															
		128us	0	128 $\mu$ s																															
		256us	1	256 $\mu$ s																															
		512us	2	512 $\mu$ s																															
		1024us	3	1024 $\mu$ s																															
		2048us	4	2048 $\mu$ s																															
		4096us	5	4096 $\mu$ s																															
		8192us	6	8192 $\mu$ s																															
		16384us	7	16384 $\mu$ s																															
		32ms	8	32768 $\mu$ s																															
		65ms	9	65536 $\mu$ s																															
		131ms	10	131072 $\mu$ s																															

### 6.11.7.17 SAMPLE

Address offset: 0x50C

Motion sample value

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0																															
ID	Acce Field	Value ID	Value	Description																												
A	R SAMPLE		[-1..2]	Last motion sample																												
				The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.																												

### 6.11.7.18 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID																																A	A	A	A
<b>Reset 0x00000000</b>	0 0																																		
ID	Acce Field	Value ID	Value	Description																															
A	RW	REPORTPER		Specifies the number of samples to be accumulated in the ACC register before the REPORTRDY and DBLRDY events can be generated.  The report period in [ $\mu$ s] is given as: $RPUS = SP * RP$ Where RPUS is the report period in [ $\mu$ s/report], SP is the sample period in [ $\mu$ s/sample] specified in SAMPLEPER, and RP is the report period in [samples/report] specified in REPORTPER .																															
		10Smpl	0	10 samples/report																															
		40Smpl	1	40 samples/report																															
		80Smpl	2	80 samples/report																															
		120Smpl	3	120 samples/report																															
		160Smpl	4	160 samples/report																															
		200Smpl	5	200 samples/report																															
		240Smpl	6	240 samples/report																															
		280Smpl	7	280 samples/report																															
		1Smpl	8	1 sample/report																															

### 6.11.7.19 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																												
ID	A																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0 0																																																												
ID	Acce Field	Value ID	Value	Description																																																									
A	R	ACC	[-1024..1023]	Register accumulating all valid samples (not double transition) read from the SAMPLE register.  Double transitions ( SAMPLE = 2 ) will not be accumulated in this register. The value is a 32 bit 2's complement value.  If a sample that would cause this register to overflow or underflow is received, the sample will be ignored and an overflow event ( ACCOF ) will be generated. The ACC register is cleared by triggering the READCLRACC or the RDCLRACC task.																																																									

### 6.11.7.20 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	R	ACCREAD	[-1024..1023]	Snapshot of the ACC register.  The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered.																												

### 6.11.7.21 PSEL.LED

Address offset: 0x51C

Pin select for LED signal

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	C																												A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																													
A	RW	PIN	[0..31]	Pin number																													
C	RW	CONNECT		Connection																													
		Disconnected	1	Disconnect																													
		Connected	0	Connect																													

### 6.11.7.22 PSEL.A

Address offset: 0x520

Pin select for A signal

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	C																												A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																													
A	RW	PIN	[0..31]	Pin number																													
C	RW	CONNECT		Connection																													
		Disconnected	1	Disconnect																													
		Connected	0	Connect																													

### 6.11.7.23 PSEL.B

Address offset: 0x524

Pin select for B signal

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	C																												A	A	A	A	A
Reset 0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	Acce Field	Value ID	Value	Description																													
A	RW	PIN	[0..31]	Pin number																													
C	RW	CONNECT		Connection																													
		Disconnected	1	Disconnect																													
		Connected	0	Connect																													



### 6.11.7.24 DBFEN

Address offset: 0x528

Enable input debounce filters

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															A
<b>Reset 0x00000000</b>	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW DBFEN			Enable input debounce filters																											
		Disabled	0	Debounce input filters disabled																											
		Enabled	1	Debounce input filters enabled																											

### 6.11.7.25 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																													A	A	A	A	A	A	A	A
<b>Reset 0x00000010</b>	0 1																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW LEDPRE		[1..511]	Period in $\mu$ s the LED is switched on prior to sampling																																

### 6.11.7.26 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																													A	A	A	A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R ACCDBL		[0..15]	Register accumulating the number of detected double or illegal transitions. ( SAMPLE = 2 ).																												
				When this register has reached its maximum value, the accumulation of double/illegal transitions will stop. An overflow event (ACCOF) will be generated if any double or illegal transitions are detected after the maximum value was reached. This field is cleared by triggering the READCLRACC or RDCLRDBL task.																												

### 6.11.7.27 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												A	A	A	A	
Reset	0x00000000																															
Reset	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	ACCDBLREAD	[0..15]	Snapshot of the ACCDBL register. This field is updated when the READCLRACC or RDCLRDBL task is triggered.																												

## 6.11.8 Electrical specification

### 6.11.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>SAMPLE</sub>	Time between sampling signals from quadrature decoder	128		131072	μs
t <sub>LED</sub>	Time from LED is turned on to signals are sampled	0		511	μs

## 6.12 RADIO — 2.4 GHz radio

The 2.4 GHz radio transceiver is compatible with multiple radio standards such as 1 Mbps and 2 Mbps *Bluetooth*<sup>®</sup> Low Energy modes, Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes, IEEE 802.15.4 250 kbps mode, as well as Nordic's proprietary 1 Mbps and 2 Mbps modes.

Listed here are main features for the RADIO:

- Multidomain 2.4 GHz radio transceiver
  - 1 Mbps and 2 Mbps *Bluetooth*<sup>®</sup> Low Energy modes
  - Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes
  - Angle-of-arrival (AoA) and angle-of-departure (AoD) direction finding using *Bluetooth*<sup>®</sup> Low Energy
  - IEEE 802.15.4 250 kbps mode
  - 1 Mbps and 2 Mbps Nordic proprietary modes
- Best in class link budget and low power operation
- Efficient data interface with EasyDMA support
- Automatic address filtering and pattern matching

EasyDMA, in combination with an automated packet assembler, packet disassembler, automated CRC generator and CRC checker, makes it easy to configure and use the RADIO. See the following figure for details.

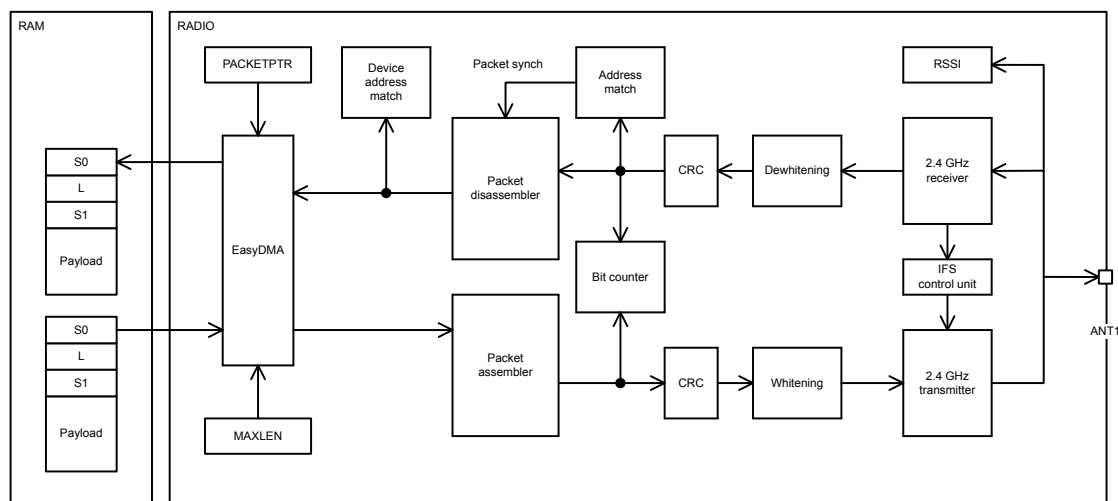


Figure 46: RADIO block diagram

The RADIO includes a device address match unit and an interframe spacing control unit that can be utilized to simplify address whitelisting and interframe spacing respectively in *Bluetooth*<sup>®</sup> low energy and similar applications.

The RADIO also includes a received signal strength indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits are sent or received by the RADIO.

### 6.12.1 Packet configuration

A RADIO packet contains the fields PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD, and CRC. For Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes, fields CI, TERM1, and TERM2 are also included.

The content of a RADIO packet is illustrated in the figures below. The RADIO sends the fields in the packet according to the order illustrated in the figures, starting on the left.

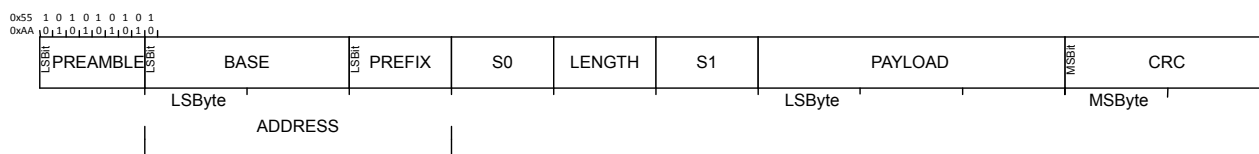


Figure 47: On-air packet layout

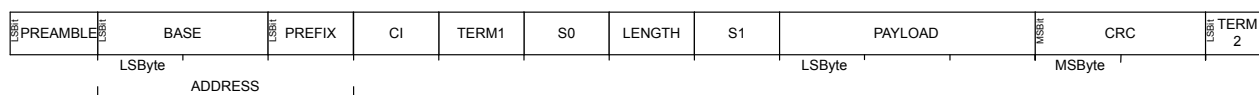


Figure 48: On-air packet layout for Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes

Not shown in the figures is the static payload add-on (the length of which is defined in `PCNF1.STATLEN`, and which is 0 bytes in a standard BLE packet). The static payload add-on is sent between PAYLOAD and CRC fields. The RADIO sends the different fields in the packet in the order they are illustrated above, from left to right.

PREAMBLE is sent with least significant bit first on air. The size of the PREAMBLE depends on the mode selected in the `MODE` register:

- The PREAMBLE is one byte for `MODE = Ble_1Mbit` as well as all Nordic proprietary operating modes (`MODE = Nrf_1Mbit` and `MODE = Nrf_2Mbit`), and `PCNF0.PLEN` has to be set accordingly. If the first bit of the ADDRESS is 0, the preamble will be set to 0xAA. Otherwise the PREAMBLE will be set to 0x55.

- For **MODE** = Ble\_2Mbit, the PREAMBLE must be set to 2 bytes through **PCNF0.PLEN**. If the first bit of the ADDRESS is 0, the preamble will be set to 0xAAAA. Otherwise the PREAMBLE will be set to 0x5555.
- For **MODE** = Ble\_LR125Kbit and **MODE** = Ble\_LR500Kbit, the PREAMBLE is 10 repetitions of 0x3C.
- For **MODE** = leee802154\_250Kbit, the PREAMBLE is 4 bytes and set to all zeros.

Radio packets are stored in memory inside instances of a RADIO packet data structure as illustrated below. The PREAMBLE, ADDRESS, CI, TERM1, TERM2, and CRC fields are omitted in this data structure. Fields S0, LENGTH, and S1 are optional.

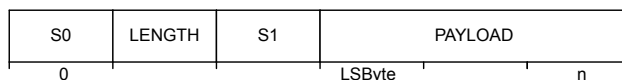


Figure 49: Representation of a RADIO packet in RAM

The byte ordering on air is always least significant byte first for the ADDRESS and PAYLOAD fields, and most significant byte first for the CRC field. The ADDRESS fields are always transmitted and received least significant bit first. The CRC field is always transmitted and received most significant bit first. The endianness, i.e. the order in which the bits are sent and received, of the S0, LENGTH, S1, and PAYLOAD fields can be configured via **PCNF1.ENDIAN**.

The sizes of the S0, LENGTH, and S1 fields can be individually configured via **S0LEN**, **LFLen**, and **S1LEN** in **PCNF0** respectively. If any of these fields are configured to be less than 8 bits, the least significant bits of the fields are used.

If S0, LENGTH, or S1 are specified with zero length, their fields will be omitted in memory. Otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

Independent of the configuration of **PCNF1.MAXLEN**, the combined length of S0, LENGTH, S1, and PAYLOAD cannot exceed 258 bytes.

## 6.12.2 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via **PCNF1.BALEN**. The base address is truncated from the least significant byte if the **PCNF1.BALEN** is less than 4. See [Definition of logical addresses](#) on page 164.

The on-air addresses are defined in the **BASE0/BASE1** and **PREFIX0/PREFIX1** registers. It is only when writing these registers that the user must relate to the actual on-air addresses. For other radio address registers, such as the **TXADDRESS**, **RXADDRESSES**, and **RXMATCH** registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in the following table.

Logical address	Base address	Prefix byte
0	BASE0	PREFIX0.AP0
1	BASE1	PREFIX0.AP1
2	BASE1	PREFIX0.AP2
3	BASE1	PREFIX0.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

Table 53: Definition of logical addresses

### 6.12.3 Data whitening

The RADIO is able to do packet whitening and de-whitening, enabled in [PCNF1.WHITEEN](#). When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial  $g(D) = D^7 + D^4 + 1$ , which then is XORed with the data packet that is to be whitened, or de-whitened. The linear feedback shift register is initialized via [DATAWHITEIV](#). See the following figure.

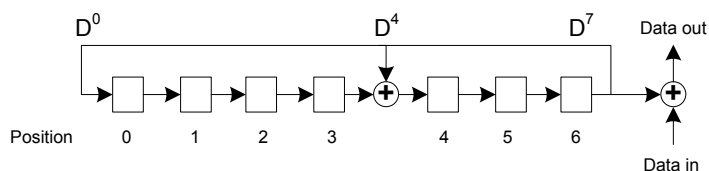


Figure 50: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet except for the preamble and the address fields.

### 6.12.4 CRC

The CRC generator in RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well.

See [CRC CNF](#) register for more information.

The CRC polynomial is configurable as illustrated in the following figure, where bit 0 in the [CRC POLY](#) register corresponds to  $X^0$  and bit 1 corresponds to  $X^1$  etc. See [CRC POLY](#) on page 210 for more information.

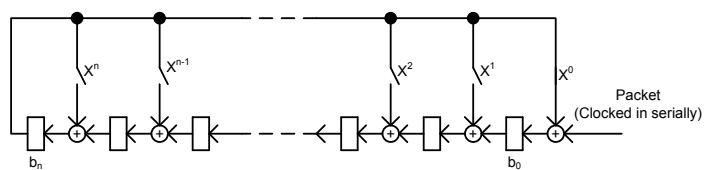


Figure 51: CRC generation of an  $n$  bit CRC

The figure shows that the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches  $b_0$  through  $b_n$  will be initialized with a predefined value specified in the [CRC INIT](#) register. After the whole packet has been clocked through the CRC generator,  $b_0$  through  $b_n$  will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception. Latches  $b_0$  through  $b_n$  are not available to be read by the CPU at any time. However, a received CRC can be read by the CPU via the [RX CRC](#) register.

The length ( $n$ ) of the CRC is configurable, see [CRC CNF](#) for more information.

Once the entire packet, including the CRC, has been received and no errors were detected, RADIO generates a [CRC OK](#) event. If CRC errors were detected, a [CRC ERROR](#) event is generated.

The status of the CRC check can be read from the [CRC STATUS](#) register after a packet has been received.

## 6.12.5 Radio states

Tasks and events are used to control the operating state of RADIO.

RADIO can enter the states described in the following table.

State	Description
DISABLED	No operations are going on inside the RADIO and the power consumption is at a minimum
RXRU	RADIO is ramping up and preparing for reception
RXIDLE	RADIO is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	RADIO is ramping up and preparing for transmission
TXIDLE	RADIO is ready for transmission to start
TX	RADIO is transmitting a packet
RXDISABLE	RADIO is disabling the receiver
TXDISABLE	RADIO is disabling the transmitter

Table 54: RADIO state diagram

A state diagram showing an overview of RADIO is shown in the following figure.

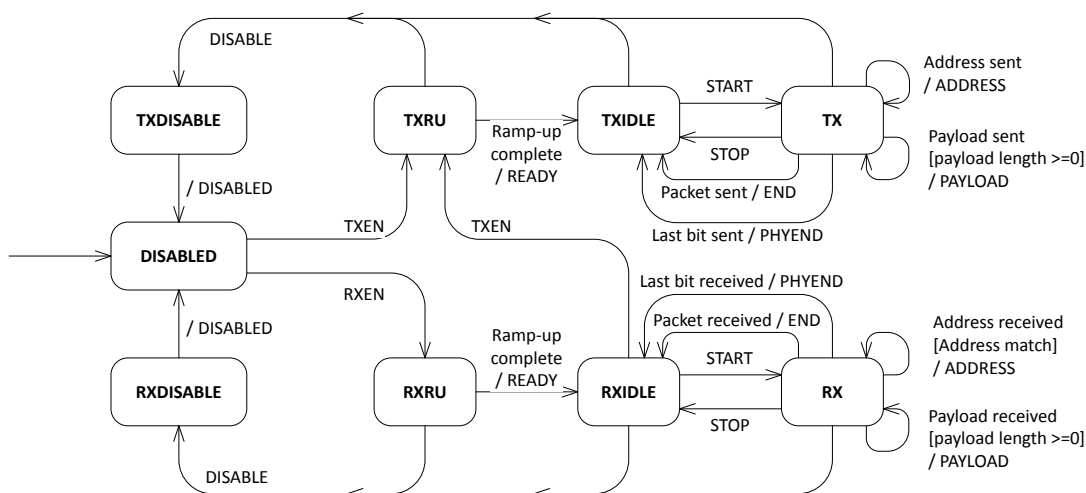


Figure 52: Radio states

This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the **RXEN** task is triggered from the **RXDISABLE** state, this may lead to incorrect behavior. The **PAYLOAD** event is always generated even if the payload is zero.

The **END** to **START** shortcut should not be used with IEEE 802.15.4 250 kbps mode. Use the **PHYEND** to **START** shortcut instead.

The **END** to **START** shortcut should not be used with Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes. Use the **PHYEND** to **START** shortcut instead.

## 6.12.6 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode. See **TXRU** in [Radio states](#) on page 166 and [Transmit sequence](#) on page 167. A **TXRU** ramp-up sequence is initiated when the **TXEN** task is triggered. After the RADIO has successfully ramped up it will generate the **READY** event

indicating that a packet transmission can be initiated. A packet transmission is initiated by triggering the **START** task. The **START** task can first be triggered after the RADIO has entered into the TXIDLE state.

The following figure illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between **READY** and **START**, and between **END** and **DISABLE**. As illustrated in [Transmit sequence](#) on page 167 the RADIO will by default transmit 1s between **READY** and **START**, and between **END** and **DISABLED**. What is transmitted can be programmed through the DTX field in the **MODECNF0** register.

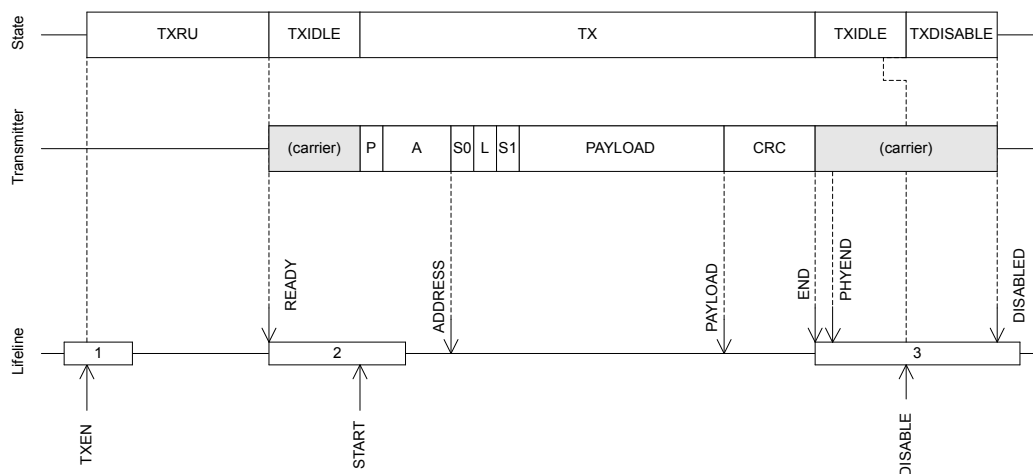


Figure 53: Transmit sequence

The following figure shows a slightly modified version of the transmit sequence where RADIO is configured to use shortcuts between **READY** and **START**, and between **END** and **DISABLE**, which means that no delay is introduced.

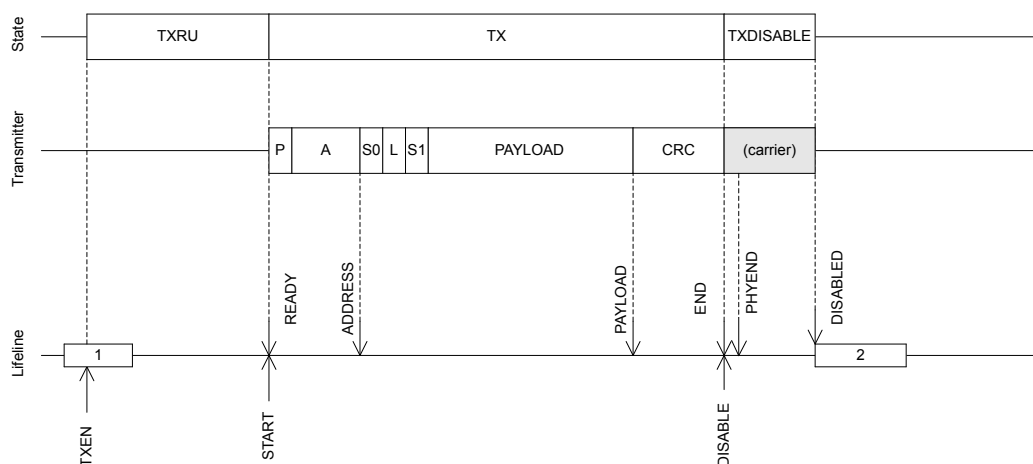


Figure 54: Transmit sequence using shortcuts to avoid delays

RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, as illustrated in the following figure.

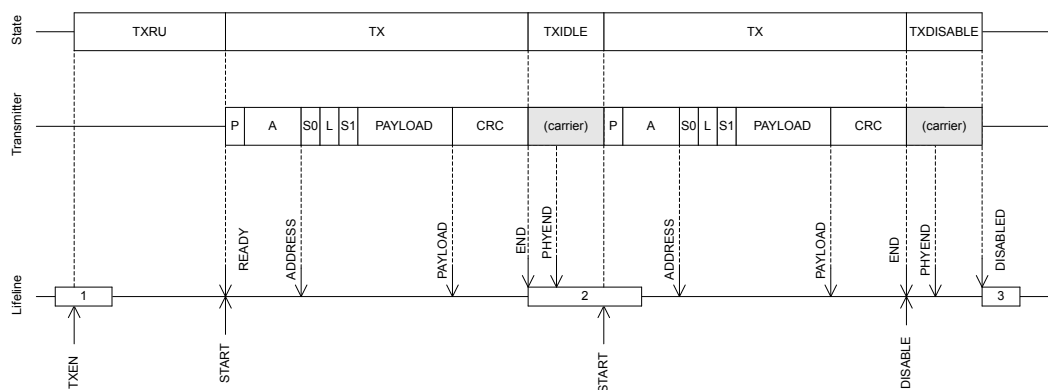


Figure 55: Transmission of multiple packets

### 6.12.7 Receive sequence

Before RADIO is able to receive a packet, it must first ramp up in RX mode. See RXRU in [Radio states](#) on page 166 and [Receive sequence](#) on page 168 for more information.

An RXRU ramp up sequence is initiated when the [RXEN](#) task is triggered. After RADIO has successfully ramped up it will generate the [READY](#) event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the [START](#) task. As illustrated in [Radio states](#) on page 166, the [START](#) task can first be triggered after RADIO has entered into the RXIDLE state.

The following figure shows a single packet reception where the CPU manually triggers the different tasks needed to control the flow of RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between [READY](#) and [START](#), and between [END](#) and [DISABLE](#). RADIO will be listening and possibly receiving undefined data, represented with an 'X', from [START](#) and until a packet with valid preamble (P) is received.

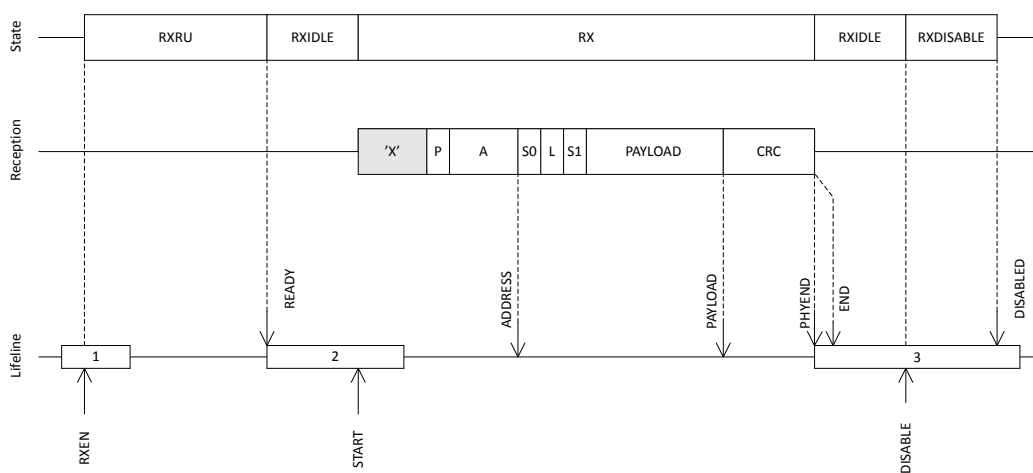


Figure 56: Receive sequence

The following figure shows a modified version of the receive sequence, where RADIO is configured to use shortcuts between [READY](#) and [START](#), and between [END](#) and [DISABLE](#), which means that no delay is introduced.



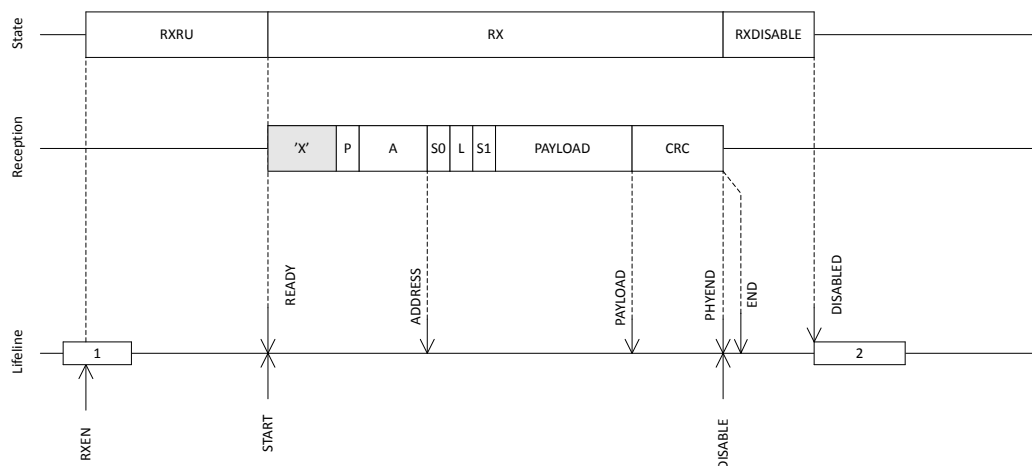


Figure 57: Receive sequence using shortcuts to avoid delays

RADIO is able to receive consecutive packets without having to disable and re-enable RADIO between packets, as illustrated in the following figure.

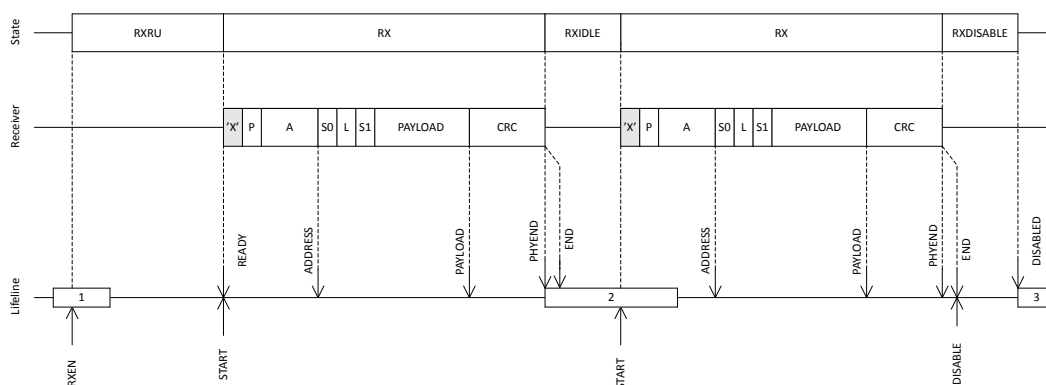


Figure 58: Reception of multiple packets

### 6.12.8 Received signal strength indicator (RSSI)

RADIO implements a mechanism for measuring the power in the received signal. This feature is called received signal strength indicator (RSSI).

The RSSI is measured continuously and the value filtered using a single-pole IIR filter. After a signal level change, the RSSI will settle after approximately  $RSSI_{SETTLE}$ .

Sampling of the received signal strength is started by using the `RSSISTART` task. The sample can be read from the `RSSISAMPLE` register.

The sample period of the RSSI is defined by  $RSSI_{PERIOD}$ . The `RSSISAMPLE` will hold the filtered received signal strength after this sample period.

For the RSSI sample to be valid, the RADIO has to be enabled in receive mode (`RXEN` task) and the reception has to be started (`READY` event followed by `START` task).

### 6.12.9 Interframe spacing (IFS)

Interframe spacing (IFS) is defined as the time, in microseconds, between two consecutive packets, starting from when the end of the last bit of the previous packet is received, to the beginning of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this interval, as specified in the `TIFS` register, as long as the `TIFS` is not specified to be shorter than the RADIO's turnaround time, i.e.

the time needed to switch off the receiver, and then switch the transmitter back on. The **TIFS** register can be written any time before the last bit on air is received.

This timing is illustrated in the figure below.

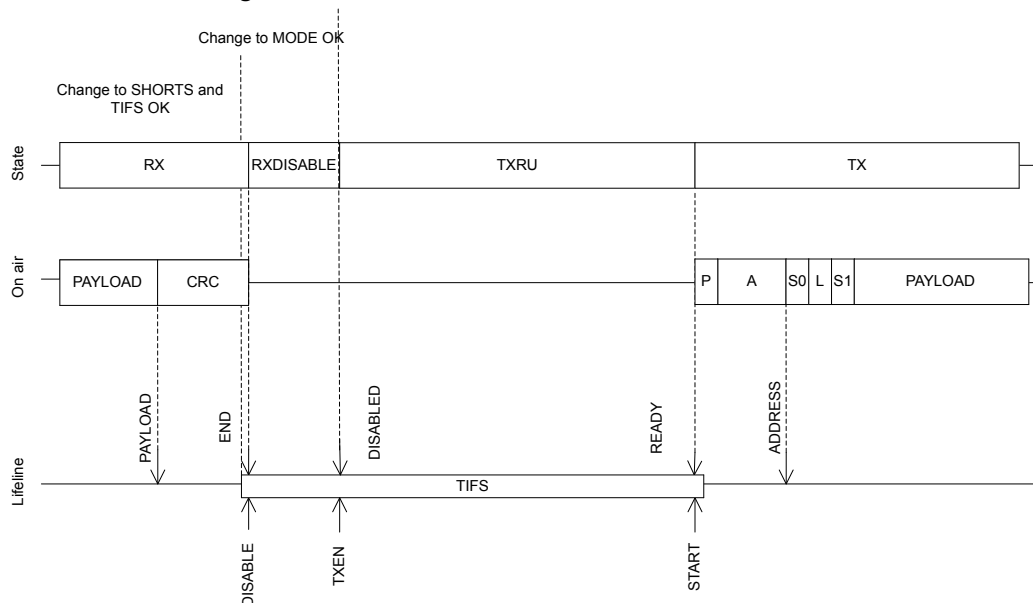


Figure 59: IFS timing detail

The **TIFS** duration starts after the last bit on air (just before the **END** event), and elapses with first bit being transmitted on air (just after **READY** event).

**TIFS** is only enforced if the shortcuts **END** to **DISABLE** and **DISABLED** to **TXEN** or **END** to **DISABLE** and **DISABLED** to **RXEN** are enabled.

**TIFS** is qualified for use in IEEE 802.15.4 250kbps mode, Long Range (125 kbps and 500 kbps) *Bluetooth*<sup>®</sup> Low Energy modes, and 1 Mbps and 2 Mbps *Bluetooth*<sup>®</sup> Low Energy modes, using the default ramp-up mode.

**SHORTS** and **TIFS** registers are not double-buffered, and can be updated at any point before the last bit on air is received. The **MODE** register is double-buffered and sampled at the **TXEN** or **RXEN** task.

### 6.12.10 Device address match

The device address match feature is tailored for address whitelisting in *Bluetooth*<sup>®</sup> low energy and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and when the RADIO is configured for little endian, see **PCNF1.ENDIAN**.

The device address match unit assumes that the first 48 bits of the payload are the device address and that bit number 6 in **S0** is the TxAdd bit. See the *Bluetooth*<sup>®</sup> Core Specification for more information about device addresses, TxAdd, and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the **DACNF** register.

### 6.12.11 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and count relative to these.

The bit counter is started by triggering the **BCSTART** task, and stopped by triggering the **BCSTOP** task. A **BCMATCH** event will be generated when the bit counter has counted the number of bits specified in the **BCC** register. The bit counter will continue to count bits until the **DISABLED** event is generated or until the **BCSTOP** task is triggered. After a **BCMATCH** event, the CPU can reconfigure the **BCC** value for new **BCMATCH** events within the same packet.

The bit counter can only be started after the RADIO has received the **ADDRESS** event.

The bit counter will stop and reset on either the **BCSTOP**, **STOP**, or **DISABLE** task, or the **END** event.

The following figure shows how the bit counter can be used to generate a **BCMATCH** event in the beginning of the packet payload, and again generate a second **BCMATCH** event after sending 2 bytes (16 bits) of the payload.

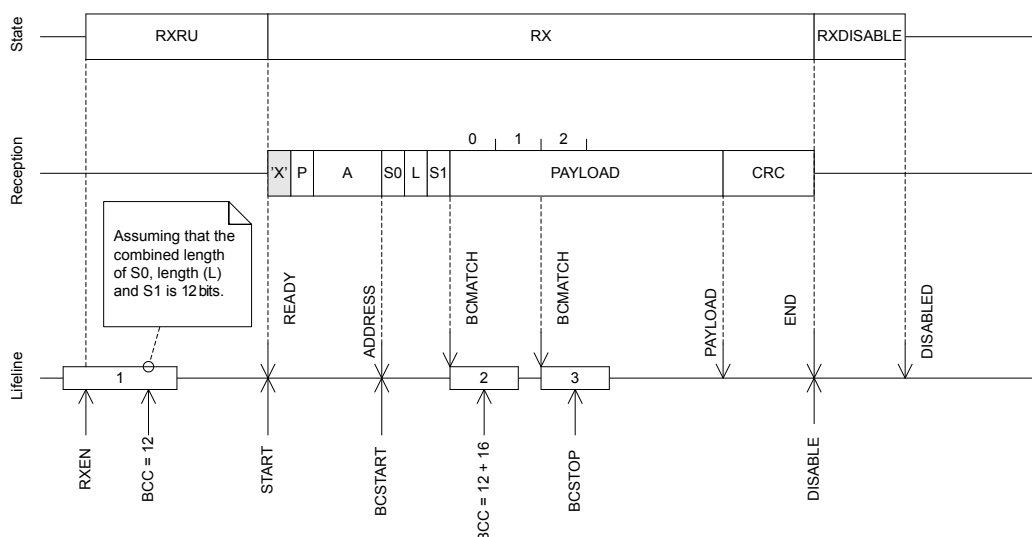


Figure 60: Bit counter example

### 6.12.12 Direction finding

The RADIO implements the Angle-of-Arrival (AoA) and Angle-of-Departure (AoD) Bluetooth Low Energy feature, which can be used to determine the direction of a peer device. The feature is available for the BLE 1 Mbps and BLE 2 Mbps modes.

When using this feature, the transmitter sends a packet with a continuous tone extension (CTE) appended to the packet, after the CRC. During the CTE, the receiver can take IQ samples of the incoming signal.

An antenna array is employed at the transmitter (AoD) or at the receiver (AoA). The AoD transmitter, or AoA receiver, switches between the antennas, in order to collect IQ samples from the different antenna pairs. The IQ samples can be used to calculate the relative path lengths between the antenna pairs, which can be used to estimate the direction of the transmitter.

#### 6.12.12.1 CTE format

The CTE is from 16  $\mu$ s to 160  $\mu$ s and consists of an unwhitened sequence of 1's, equivalent to a continuous tone nominally offset from the carrier by +250 kHz for the 1 Mbps PHY and +500 kHz for the 2 Mbps BLE PHYs. The format of the CTE, when switching and/or sampling, is shown in the following figure.

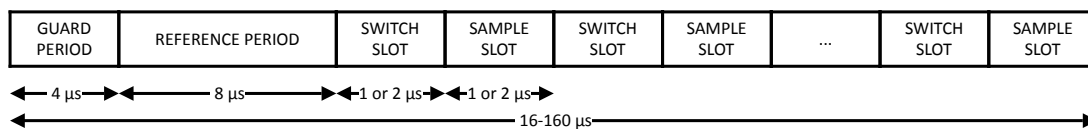


Figure 61: Constant tone extension (CTE) structure

Antenna switching is performed during switch slots and the guard period. The AoA/AoD feature requires that one IQ sample is taken for each microsecond within the reference period, and once for each sample slot. Oversampling is possible by changing the sample spacing as described in [IQ sampling](#) on page 175. The switch slot and sample slot durations are either 1 or 2  $\mu\text{s}$ , but must be equal. The format of the CTE and switching and sampling procedures may be configured prior to, or during, packet transmission and reception. Alternatively, during packet reception, these operations can be configured by reading specific fields of the packet contents.

### 6.12.12.2 Mode

Depending on the [DFEMODE](#), the device performs the procedures shown in the following table.

	DFEMODE			
	AOA		AOD	
	TX	RX	TX	RX
Generating and transmitting CTE	x		x	
Receiving, interpreting, and sampling CTE		x		x
Antenna switching		x	x	

Table 55: AoA/AoD Procedures performed as a function of DFEMODE and TX/RX mode

### 6.12.12.3 Inline configuration

When inline configuration is enabled during RX, further configuration of the AoA/AoD procedures is performed based on the values of the CP bit and the CTEInfo octet within the packet. This is enabled by setting [CTEINLINECONF.CTEINLINECTRLLEN](#). The CTEInfo octet is present only if the CP bit is set. The position of the CP bit and CTEInfo octet depends on whether the packet has a *Data Channel PDU* ([CTEINLINECONF.CTEINFOINS1=InS1](#)), or an *Advertising Channel PDU* ([CTEINLINECONF.CTEINFOINS1=NotInS1](#)).

#### Data channel PDU

For Data Channel PDUs, [PCNF0.SOLEN](#) must be 1 byte, and [PCNF0.LFLEN](#) must be 8 bits. To determine if S1 is present, the registers [CTEINLINECONF.S0MASK](#) and [CTEINLINECONF.S0CONF](#) forms a bitwise mask-and-test for the S0 field. If the bitwise AND between S0 and S0MASK equals S0CONF, then S1 is determined to be present. When present, the value of [PCNF0.S1LEN](#) will be ignored, as this is decided by the CP bit in the the following figure.

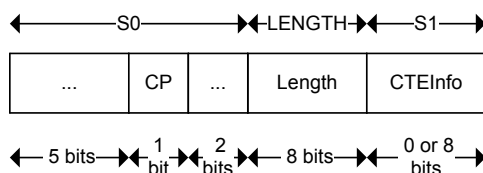


Figure 62: Data channel PDU header

When encrypting and decrypting BLE packets using the [CCM](#) peripheral, it is also required to set [PCNF0.S1INCL=1](#). The CCM mode must be configured to use an 8-bit length field. The value of the CP bit is included in the calculation of the MIC, while the S1 field is ignored by the CCM calculation.

## Advertising channel PDU

For advertising channel PDUs, the CTEInfo Flag replaces the CP bit. The CTEInfo Flag is within the extended header flag field in some of the advertising PDUs that employ the common extended advertising payload format (i.e. AUX\_SYNC\_IND, AUX\_CHAIN\_IND). The format of such packets is shown in the following figure.

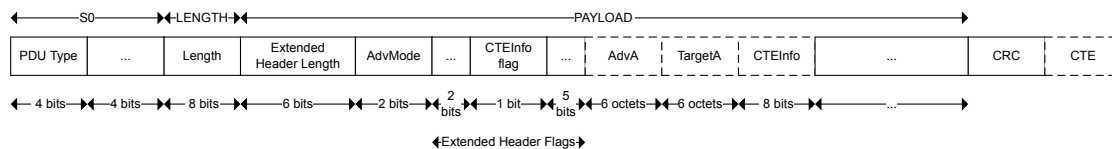


Figure 63: Advertising channel PDU header

The [CTEINLINECONF.SOCONF](#) and [CTEINLINECONF.SOMASK](#) fields can be configured to accept only certain advertising PDU Types. If the extended header length is non-zero, the CTEInfo extended header flag is checked to determine whether CTEInfo is present. If a bit before the CTEInfo flag within the extended header flags is set, then the CTEInfo position is postponed 6 octets.

## CTEInfo parsing

The CTEInfo field is shown in the following figure.

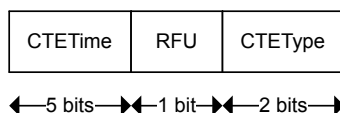


Figure 64: CTEInfo field

The CTETIME field defines the length of the CTE in 8  $\mu$ s units. The valid upper bound of values can be adjusted using [CTEINLINECONF.CTETIMEVALIDRANGE](#), including allowing use of the RFU bit within this field. If the CTETIME field is an invalid value of either 0 or 1, the CTE is assumed to be the minimum valid length of 16  $\mu$ s. The slot duration is determined by the CTEType field. In RX this determines whether the sample spacing as defined in [CTEINLINECONF.CTEINLINERXMODE1US](#) or [CTEINLINECONF.CTEINLINERXMODE2US](#) is used.

CTEType	Description	TX switch spacing	RX sample spacing during reference period	Sample spacing RX during reference period
0	AoA, no switching	-	TSAMPLESPACING1	TSAMPLESPACING2
1	AoD, 1 $\mu$ s slots	2 $\mu$ s	TSAMPLESPACING1	CTEINLINERXMODE1US
2	AoD, 2 $\mu$ s slots	4 $\mu$ s	TSAMPLESPACING1	CTEINLINERXMODE2US
3	Reserved for future use			

Table 56: Switching and sampling spacing based on CTEType

### 6.12.12.4 Manual configuration

If [CTEINLINECONF.CTEINLINECTRLLEN](#) is not set, then the packet is not parsed to determine the CTE parameters, and the antenna switching and sampling is controlled by other registers, see [Antenna switching](#) on page 174. The length of the CTE is given in 8  $\mu$ s units by [DFCTRL1.NUMBEROF8US](#). The start of the antenna switching and/or sampling (denoted as an AoA/AoD procedure), can be configured to start at some trigger with an additional offset. Using [DFCTRL1.DFEINEXTENSION](#), the trigger can be configured to be the end of the CRC, or alternatively, the ADDRESS event. The additional offset for antenna switching is configured using [DFCTRL2.TSWITCHOFFSET](#). Similarly, the additional offset for antenna sampling is configured using [DFCTRL2.TSAMPLEOFFSET](#).

### 6.12.12.5 Receive- and transmit sequences

The addition of the CTE to the transmitted packet is illustrated in the following figure.

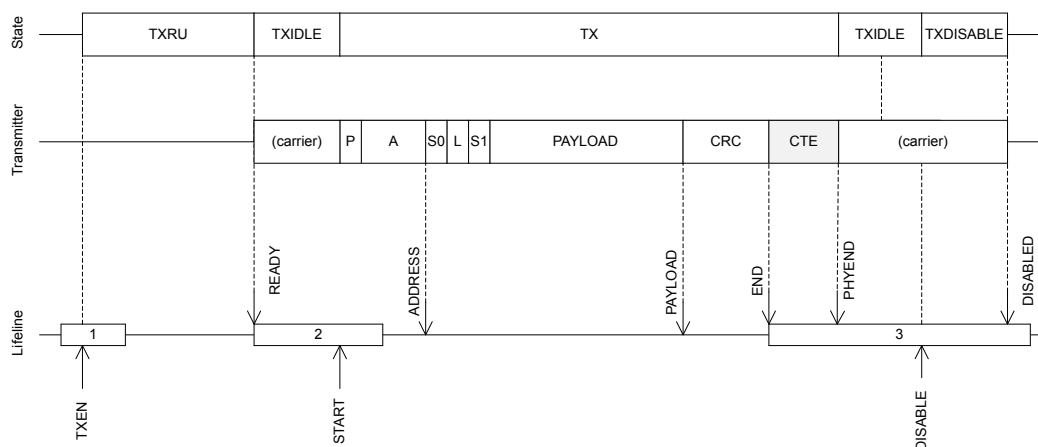


Figure 65: Transmit sequence with DFE

The presence of CTE within a received packet is signalled by the **CTEPRESENT** event illustrated in the figure below.

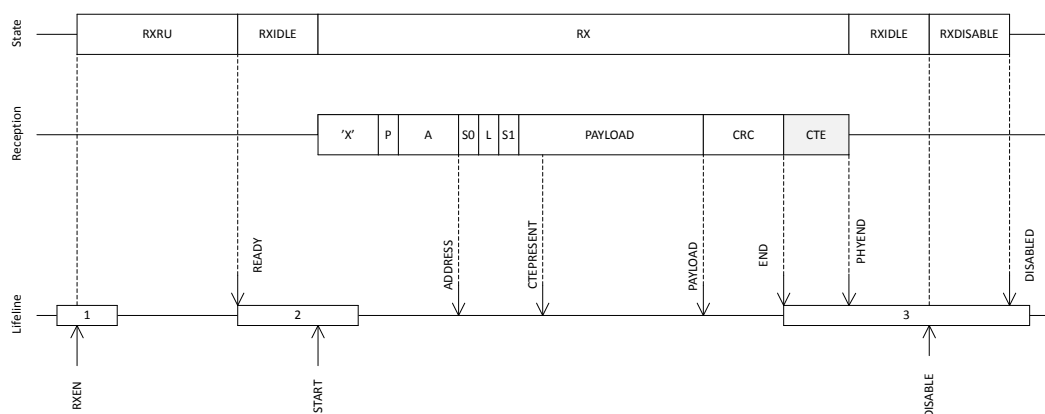


Figure 66: Receive sequence with DFE

### 6.12.12.6 Antenna switching

The RADIO can control up to 8 GPIO pins in order to control external antenna switches used in direction finding.

#### Pin configuration

The eight antenna selection signals are mapped to physical pins according to the pin numbers specified in the PSEL.DFEGPIO[n] registers. Only pins that have the PSEL.DFEGPIO[n].CONNECTED field set to *Connected* will be controlled by the RADIO. Pins that are *Disconnected* will be controlled by GPIO.

During transmission in AoD TX mode or reception in AoA RX mode, the RADIO automatically acquires the pins as needed. At times when the RADIO does not use the pin, the pin is released to its default state and controlled by the GPIO configuration. Thus, the pin must be configured using the GPIO peripheral.

Pin acquired by RADIO	Direction	Value	Comment
Yes	Output	Specified in <code>SWITCHPATTERN</code>	Pin acquired by RADIO, and in use for DFE.
No	Specified by <code>GPIO</code>	Specified by <code>GPIO</code>	DFE not in progress. Pin has not been acquired by RADIO, but is available for DFE use.

Table 57: Pin configuration matrix for a connected and enabled pin [n]

## Switch pattern configuration

The values of the GPIOs while switching during the CTE are configured by writing successively to the `SWITCHPATTERN` register. The first write to `SWITCHPATTERN` is the GPIO pattern applied from the call of `TASKS_TXEN` or `TASKS_RXEN` until the first antenna switch is triggered. The second write sets the pattern for the reference period and is applied at the start of the guard period. The following writes set the pattern for the remaining switch slots and are applied at the start of each switch slot. If writing beyond the total number of antenna slots, the pattern will wrap to `SWITCHPATTERN[2]` and start over again. During operation, when the end of the `SWITCHPATTERN` buffer is reached, the RADIO cycles back to `SWITCHPATTERN[2]`. At the end of the AoA/AoD procedure, `SWITCHPATTERN[0]` is applied to `DFCTRL1.TSWITCHSPACING` after the previous antenna switch. The `SWITCHPATTERN` buffer can be erased/cleared using `CLEARPATTERN`.

A minimum number of three patterns must be written to the `SWITCHPATTERN` register.

If `CTEINLINECONF.CTEINLINECTRLLEN` is not set, then the antenna switch spacing is determined by `DFCTRL1.TSWITCHSPACING` (otherwise described by [Switching and sampling spacing based on CTEType](#) on page 173). `DFCTRL2.TSWITCHOFFSET` determines the position of the first switch compared to the configurable start of CTE (see `DFCTRL1.DFEINEXTENSION`).

### 6.12.12.7 IQ sampling

The RADIO uses DMA to write IQ samples recorded during the CTE to RAM. Alternatively, the magnitude and phase of the samples can be recorded using the `DFCTRL1.SAMPLETYPE` field. The samples are written to the location in RAM specified by `DFEPACKET.PTR`. The maximum number of samples to transfer are specified by `DFEPACKET.MAXCNT` and the number of samples transferred are given in `DFEPACKET.AMOUNT`. The IQ samples are recorded with respect to the RX carrier frequency. The format of the samples is provided in the following table.

SAMPLETYPE	Field	Bits	Description
0: I_Q (default)	Q	31:16	12 bits signed, sign extended to 16 bits. Out of range samples are saturated at value -32768.
	I	15:0	
1: MagPhase	reserved	31:29	Always zero
	magnitude	28:16	13 bits unsigned. Equals $1.646756 * \sqrt{I^2 + Q^2}$ .
	phase	15:0	9 bits signed, sign extended to 16 bits. Equals $64 * \text{atan2}(Q, I)$ in the range [-201,201].

Table 58: Format of samples

Oversampling is configured separately for the reference period and for the time after the reference period. During the reference period, the sample spacing is determined by `DFCTRL1.TSAMPLESPACINGREF`. `DFCTRL2.TSAMPLEOFFSET` determines the position of the first sample relative to the end of the last bit of the CRC.

For the time after the reference period, if `CTEINLINECONF.CTEINLINECTRLLEN` is disabled, the sample spacing is set in `DFCTRL1.TSAMPLESPACING`. However, when `CTEINLINECONF.CTEINLINECTRLLEN` is enabled, the sample spacing is determined by two different registers, depending on whether the device is in AoA or AoD RX-mode.

For AoD RX mode, the sample spacing after the reference period is determined by the CTEType in the packet, as listed in the following table.

CTEType	Sample spacing
AoD 1 $\mu$ s slots	CTEINLINECONF.CTEINLINERXMODE1US
AoD 2 $\mu$ s slots	CTEINLINECONF.CTEINLINERXMODE2US
Other	DFECTRL1.TSAMPLESPACING

Table 59: Sample spacing when CTEINLINECONF.CTEINLINECTRLLEN is set and the device is in AoD RX mode

For AoA RX mode, the sample spacing after the reference period is determined by DFECTRL1.TSWITCHSPACING, as listed in the following table.

DFECTRL1.TSWITCHSPACING	Sample spacing
2 $\mu$ s	CTEINLINECONF.CTEINLINERXMODE1US
4 $\mu$ s	CTEINLINECONF.CTEINLINERXMODE2US
Other	DFECTRL1.TSAMPLESPACING

Table 60: Sample spacing when CTEINLINECONF.CTEINLINECTRLLEN is set and the device is in AoA RX mode

For the reference and switching periods, DFECTRL1.TSAMPLESPACINGREF and DFECTRL1.TSAMPLESPACING can be used to achieve oversampling.

### 6.12.13 IEEE 802.15.4 operation

With the `MODE=ieee802154_250kbit` the RADIO will comply with the IEEE 802.15.4-2006 standard implementing its 250 kbps, 2450 MHz, O-QPSK PHY.

The IEEE 802.15.4 standard differs from Nordic's proprietary and *Bluetooth*<sup>®</sup> low energy modes. Notable differences include modulation scheme, channel structure, packet structure, security, and medium access control.

The main features of the IEEE 802.15.4 mode are:

- Ultra-low power 250 kbps, 2450 MHz, IEEE 802.15.4-2006 compliant link
- Clear channel assessment
- Energy detection scan
- CRC generation

#### 6.12.13.1 Packet structure

The IEEE 802.15.4 standard defines an on-the-air frame/packet that is different from what is used in BLE mode.

The following figure provides an overview of the physical frame structure and its timing.

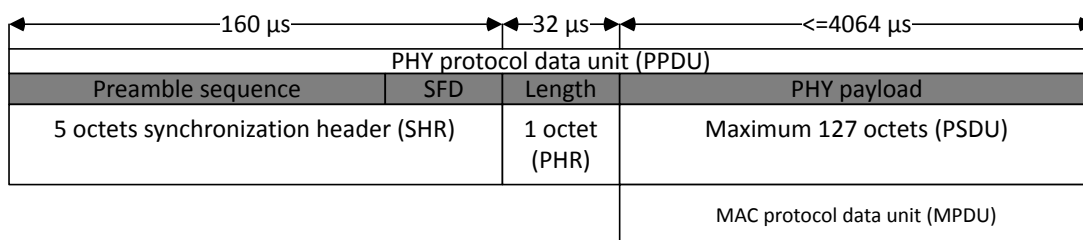


Figure 67: IEEE 802.15.4 frame format (PPDU)

The standard uses the term *octet* for an 8-bit storage unit within the PPDU. For timing, the value *symbol* is used, and it has a duration of 16  $\mu$ s.

The total usable payload (PSDU) is 127 octets, but when CRC is in use, this is reduced to 125 octets of usable payload.



The preamble sequence consists of four octets that are all zero, and are used for synchronizing the RADIO's receiver. Following the preamble is the single octet *start of frame delimiter (SFD)*, with a fixed value of 0xA7. An alternate SFD can be programmed through the **SFD** register, providing an initial level of frame filtering for those who choose non-standard compliance. It is a valuable feature when operating in a congested or private network. The preamble sequence and the SFD are generated by the RADIO, and are not programmed by the user into the frame buffer.

Following the five octet *synchronization header (SHR)* is the single octet *phy header (PHR)*. The least significant seven bits of PHR denote the frame length of the following PSDU. The most significant bit is reserved and is set to zero for frames that are standard compliant. The RADIO reports all eight bits which can be used to carry additional information. The PHR is the first byte written to the frame data memory pointed to by **PACKETPTR**. Frames with zero length are discarded, and the **FRAMESTART** event is not generated in this case.

The next N octets carry the data of the PHY packet, where N equals the value of the PHR. For an implementation also using the IEEE 802.15.4 MAC layer, the PHY data is a MAC frame of N-2 octets, since two octets occupy a CRC field.

An IEEE 802.15.4 MAC layer frame consists of the following:

- A header:
  - The frame control field (FCF)
  - The sequence number
  - Addressing fields
- A payload
- The 16-bit frame control sequence (FCS)

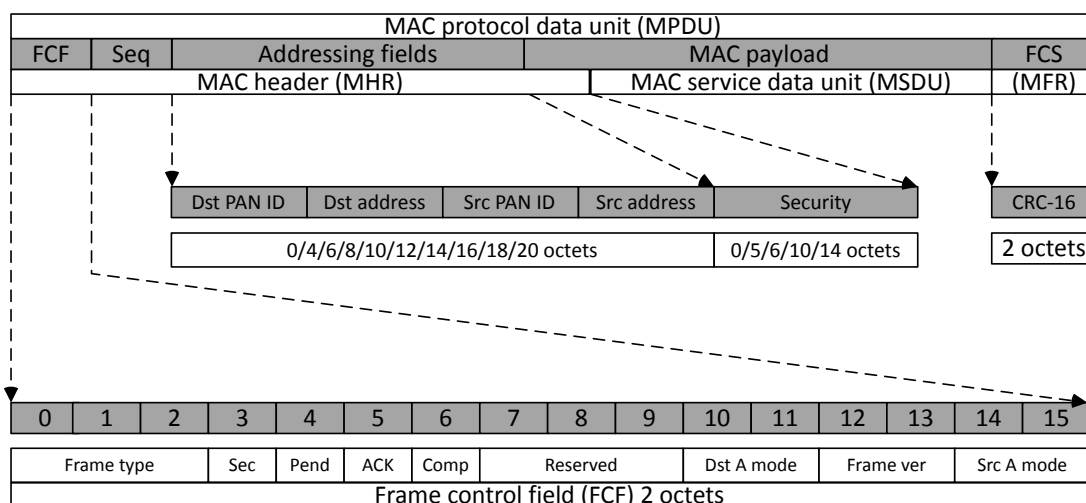


Figure 68: IEEE 802.15.4 frame format (MPDU)

The two FCF octets contain information about the frame type, addressing, and other control flags. This field is decoded when using the assisted operating modes offered by the RADIO.

The sequence number is a single octet in size and is unique for a frame. It is used in the associated acknowledgement frame sent upon successful frame reception.

The addressing field can be zero (acknowledgement frame) or up to 20 octets in size. The field is used to direct packets to the correct recipient and denote its origin. IEEE 802.15.4 bases its addressing on networks being organized in PANs with 16-bit identifier and nodes having a 16-bit or 64-bit address. In the assisted receive mode, these parameters are analyzed for address matching and acknowledgement.

The MAC payload carries the data of the next higher layer, or in the case of a MAC command frame, information used by the MAC layer itself.

The two last octets contain the 16-bit ITU-T CRC. The FCS is calculated over the MAC header (MHR) and MAC payload (MSDU) parts of the frame. This field is calculated automatically when sending a frame, or indicated in the `CRCSTATUS` register when a frame is received. If configured, this feature is taken care of autonomously by the CRC module.

### 6.12.13.2 Operating frequencies

The IEEE 802.15.4 standard defines 16 channels, 11 - 26, of 5 MHz each, in the 2450 MHz frequency band.

To choose the correct channel center frequency, the `FREQUENCY` register must be programmed according to the table below.

IEEE 802.15.4 channel	Center frequency (MHz)	FREQUENCY setting
Channel 11	2405	5
Channel 12	2410	10
Channel 13	2415	15
Channel 14	2420	20
Channel 15	2425	25
Channel 16	2430	30
Channel 17	2435	35
Channel 18	2440	40
Channel 19	2445	45
Channel 20	2450	50
Channel 21	2455	55
Channel 22	2460	60
Channel 23	2465	65
Channel 24	2470	70
Channel 25	2475	75
Channel 26	2480	80

Table 61: IEEE 802.15.4 center frequency definition

### 6.12.13.3 Energy detection (ED)

As required by the IEEE 802.15.4 standard, it must be possible to sample the received signal power within the bandwidth of a channel, for the purpose of determining presence of activity.

To prevent the channel signal from being decoded, the shortcut between the `READY` event and the `START` task should be disabled before putting the RADIO in receive mode. The energy detection (ED) measurement time, where RSSI samples are averaged, is 8 symbol periods, corresponding to 128  $\mu$ s. The standard further specifies the measurement to be a number between 0 and 255, where 0 shall indicate received power less than 10 dB above the selected receiver sensitivity. The power range of the ED values must be at least a 40 dB linear mapping with accuracy of  $\pm 6$  dB. See section 6.9.7 *Receiver ED* in the IEEE 802.15.4 standard for further details.

The following example shows how to perform a single energy detection measurement and convert to IEEE 802.15.4 scale.

**IEEE 802.15.4 ED measurement example**

```

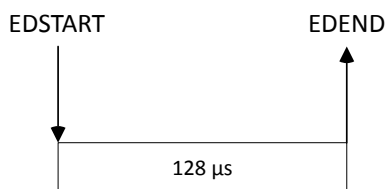
#define ED_RSSISCALE 4 // From electrical specifications
uint8_t sample_ed(void)
{
    int val;
    NRF_RADIO->TASKS_EDSTART = 1; // Start
    while (NRF_RADIO->EVENTS_EDEND != 1) {
        // CPU can sleep here or do something else
        // Use of interrupts are encouraged
    }
    val = NRF_RADIO->EDSAMPLE * ED_RSSISCALE; // Read level
    return (uint8_t)(val>255 ? 255 : val); // Convert to IEEE 802.15.4
    scale
}

```

For scaling between hardware value and dBm, see equation [Conversion between hardware value and dBm](#) on page 181.

The `mlme-scan.req` primitive of the MAC layer uses the ED measurement to detect channels where there might be wireless activity. To assist this primitive, a tailored mode of operation is available where the ED measurement runs for a defined number of iterations keeping track of the maximum ED level. This is engaged by writing the `EDCNT` register to a value different from 0, where it will run the specified number of iterations and report the maximum energy measurement in the `EDSAMPLE` register. The scan is started with `EDSTART` task and its end indicated with the `EDEND` event. This significantly reduces the interrupt frequency and therefore power consumption. The following figure shows how the ED measurement will operate depending on the `EDCNT` register.

**EDCNT = 0**



**EDCNT = N-1**

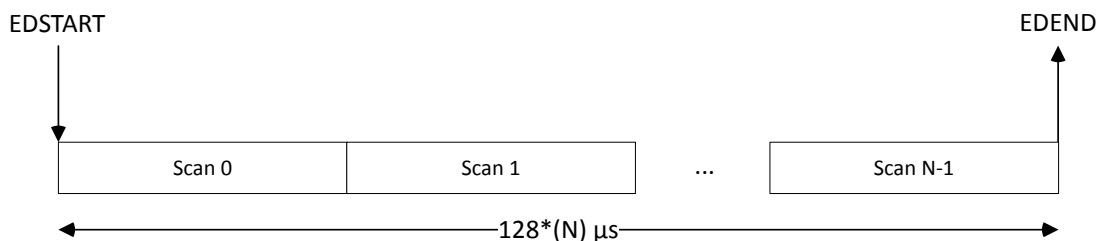


Figure 69: Energy detection measurement examples

The scan is stopped by writing the `EDSTOP` task. It will be followed by the `EDSTOPPED` event when the module has terminated.

#### 6.12.13.4 Clear channel assessment (CCA)

IEEE 802.15.4 implements a listen-before-talk channel access method to avoid collisions when transmitting, known as *carrier sense multiple access with collision avoidance (CSMA-CA)*. The key part of this is measuring if the wireless medium is busy or not.

The following clear channel assesment modes are supported:

- *CCA Mode 1* (energy above threshold) - The medium is reported busy upon detecting any energy above the ED threshold.
- *CCA Mode 2* (carrier sense only) - The medium is reported busy upon detection of a signal compliant with the IEEE 802.15.4 standard with the same modulation and spreading characteristics.
- *CCA Mode 3* (carrier sense with energy above threshold) - The medium is reported busy using a logical combination (AND/OR) between the results from CCA Mode 1 and CCA Mode 2.

The clear channel assessment should survey a period equal to 8 symbols or 128  $\mu$ s.

The RADIO must be in receive mode and be able to receive correct packets when performing the CCA. The shortcut between **READY** and **START** must be disabled if baseband processing is not to be performed while the measurement is running.

## CCA Mode 1

*CCA Mode 1* is enabled by first configuring the field `CCACTRL.CCAMODE=EdMode` and writing the `CCACTRL.CCAEDTHRES` field to a chosen value. Once the `CCASTART` task is written, the RADIO will perform a ED measurement for 8 symbols and compare the measured level with that found in the `CCACTRL.CCAEDTHRES` field. If the measured value is higher than or equal to this threshold, the `CCABUSY` event is generated. If the measured level is less than the threshold, the `CCAIDLE` event is generated.

## CCA Mode 2

*CCA Mode 2* is enabled by configuring `CCACTRL.CCAMODE=CarrierMode`. The RADIO will sample to see if a valid SFD is found during the 8 symbols. If a valid SFD is detected, the `CCABUSY` event is generated and the device should not send any data. The `CCABUSY` event is also generated if the scan was performed during an ongoing frame reception. In the case where the measurement period completes with no SFD detection, the `CCAIDLE` event is generated. When `CCACTRL.CCACORRCNT` is not zero, the algorithm will look at the correlator output in addition to the SFD detection signal. If a SFD is reported during the scan period, it will terminate immediately indicating busy medium. Similarly, if the number of peaks above `CCACTRL.CCACORRTHRES` crosses the `CCACTRL.CCACORRCNT`, the `CCACTRL.CCABUSY` event is generated. If less than `CCACORRCOUNT` crossings are found and no SFD is reported, the `CCAIDLE` event will be generated and the device can send data.

## CCA Mode 3

*CCA Mode 3* is enabled by configuring `CCACTRL.CCAMODE=CarrierAndEdMode` or `CCACTRL.CCAMODE=CarrierOrEdMode`, performing the required logical combination of the result from CCA Mode 1 and 2. The `CCABUSY` or `CCAIDLE` events are generated by ANDing or ORing the *energy above threshold* and *carrier detection* scans.

## Shortcuts

An ongoing CCA can always be stopped by issuing the `CCASTOP` task. This will trigger the associated `CCASTOPPED` event.

For CCA mode automation, a number of shortcuts are available.

- To automatically switch between RX (when performing the CCA) and to TX where the packet is sent, the shortcut between `CCAIDLE` and `TXEN`, in conjunction with the short between `CCAIDLE` and `STOP` must be used.

- To automatically disable the RADIO whenever the CCA reports a busy medium, the shortcut between `CCABUSY` and `DISABLE` can be used.
- To immediately start a CCA after ramping up into RX mode, the shortcut between `RXREADY` and `CCASTART` can be used.

## Conversion

The conversion from a `CCAEDTHRES`, `LQI`, or `EDSAMPLE` value to dBm can be done with the following equation, where `VALHARDWARE` is either `CCAEDTHRES`, `LQI`, or `EDSAMPLE`. `LQI` and `EDSAMPLE` are hardware-reported values, while `CCAEDTHRES` is set by software. Constants `ED_RSSISCALE` and `ED_RSSIOFFS` are from electrical specifications.

$$P_{RF}[\text{dBm}] = \text{ED\_RSSIOFFS} + \text{VAL}_{\text{HARDWARE}}$$

Figure 70: Conversion between hardware value and dBm

The `ED_RSSISCALE` constant is used to calculate power in 802.15.4 units (0-255):

$$P_{RF}[\text{802.15.4 units}] = \text{MIN}(\text{ED\_RSSISCALE} \times \text{VAL}_{\text{HARDWARE}}, 255)$$

Figure 71: Conversion between hardware value and 802.15.4 units (0-255)

### 6.12.13.5 Cyclic redundancy check (CRC)

IEEE 802.15.4 uses a 16-bit ITU-T cyclic redundancy check (CRC) calculated over the MAC header (MHR) and MAC service data unit (MSDU).

The standard defines the following generator polynomial:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

In receive mode the RADIO will trigger the CRC module when the first octet after the frame length (PHR) is received. The CRC will then update on each consecutive octet received. When a complete frame is received the `CRCSTATUS` register will be updated accordingly and the `CRCOK` or `CRCERROR` events generated. When the CRC module is enabled it will not write the two last octets (CRC) to the frame Data RAM. When transmitting, the CRC will be computed on the fly, starting with the first octet after PHR, and inserted as the two last octets in the frame. The EasyDMA will fetch frame length minus 2 octets from RAM and insert the CRC octets insitu.

The following code shows how to configure the CRC module for correct operation when in IEEE 802.15.4 mode. The `CRC CNF` is written to 16-bit CRC and the `CRC POLY` is written to 0x11021. The start value used by IEEE 802.15.4 is zero and `CRC INIT` is configured to reflect this.

```
/* 16-bit CRC with ITU-T polynomial with 0 as start condition*/
NRF_RADIO->CRCCNF = ((RADIO_CRCCNF_SKIPADDR_Ieee802154 << RADIO_CRCCNF_SKIPADDR_Pos) |
                    (RADIO_CRCCNF_LEN_Two << RADIO_CRCCNF_LEN_Pos));
NRF_RADIO->CRCPOLY = 0x11021;
NRF_RADIO->CRCINIT = 0;
```

The `ENDIANESS` subregister must be set to little-endian since the FCS field is transmitted from left bit to right.

### 6.12.13.6 Transmit sequence

The transmission is started by first putting the RADIO in receive mode and triggering the `RXEN` task.

An outline of the IEEE 802.15.4 transmission is illustrated in the following figure.

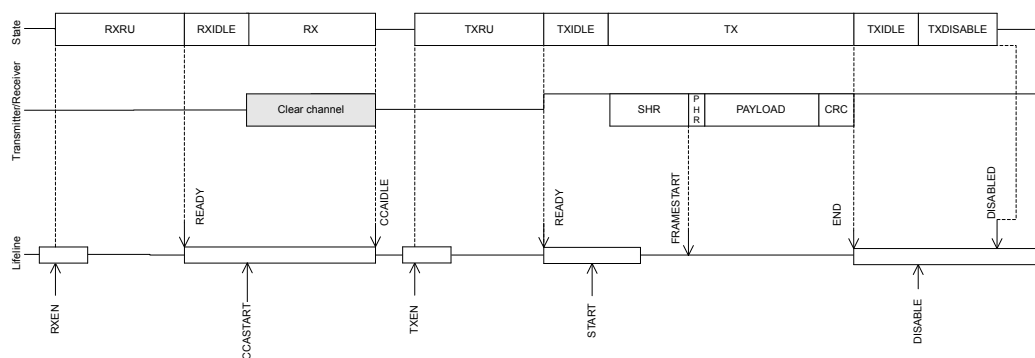


Figure 72: IEEE 802.15.4 transmit sequence

The receiver will ramp up and enter the RXIDLE state where the **READY** event is generated. Upon receiving the ready event, the CCA is started by triggering the **CCASTART** task. The chosen mode of assessment (**CCACTRL.CCAMODE** register) will be performed and signal the **CCAIDLE** or **CCABUSY** event 128  $\mu$ s later. If the **CCABUSY** event is received, the RADIO will have to retry the CCA after a specific back-off period. This is outlined in the *IEEE 802.15.4 standard, Figure 69 in section 7.5.1.4 The CSMA-CA algorithm*.

If the **CCAIDLE** event is generated, a write to the **TXEN** task register enters the RADIO in TXRU state. The **READY** event will be generated when the RADIO is in TXIDLE state and ready to transmit. With the **PACKETPTR** pointing to the length (PHR) field of the frame, the **START** task can be written. The RADIO will send the four octet preamble sequence followed by the start of frame delimiter (**SFD** register). The first byte read from the Data RAM is the length field (PHR) followed by the transmission of the number of bytes indicated as the frame length. If the CRC module is configured it will run for PHR-2 octets. The last two octets will be substituted with the results from running the CRC. The necessary CRC parameters are sampled on the **START** task. The FCS field of the frame is little endian.

In addition to the already available shortcuts, one is provided between **READY** event and **CCASTART** task so that a CCA can automatically start when the receiver is ready. A second shortcut has been added between **CCAIDLE** event and the **TXEN** task, so that upon detecting a clear channel the RADIO can immediately enter transmit mode.

### 6.12.13.7 Receive sequence

The reception is started by first putting the RADIO in receive mode. After writing to the **RXEN** task, the RADIO will start ramping up and enter the RXRU state.

When the **READY** event is generated, the RADIO enters the RXIDLE mode. For the baseband processing to be enabled, the **START** task must be written. An outline of the IEEE 802.15.4 reception can be found in the following figure.

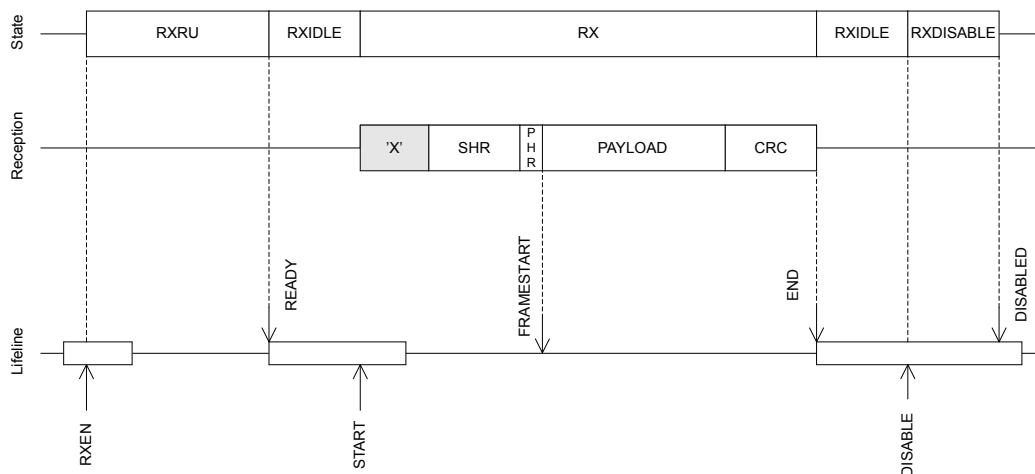


Figure 73: IEEE 802.15.4 receive sequence

When a valid SHR is received, the RADIO will start storing future octets (starting with PHR) to the data memory pointed to by `PACKETPTR`. After the SFD octet is received, the `FRAMESTART` event is generated. If the CRC module is enabled it will start updating with the second byte received (first byte in payload) and run for the full frame length. The two last bytes in the frame are not written to RAM when CRC is configured. However, if the result of the CRC after running the full frame is zero, the `CRCOK` event will be generated. The `END` event is generated when the last octet has been received and is available in data memory.

When a packet is received, a link quality indicator (LQI) is also generated and appended immediately after the last received octet. When using an IEEE 802.15.4 compliant frame, this will be just after the MSDU since the FCS is not reported. In the case of a non-compliant frame, it will be appended after the full frame. The LQI reported by hardware must be converted to IEEE 802.15.4 range by an 8-bit saturating multiplication of 4, as shown in [IEEE 802.15.4 ED measurement example](#) on page 179. The LQI is only valid for frames equal to or longer than three octets. When receiving a frame, the RSSI (reported as negative dB) will be measured at three points during the reception. These three values will be sorted and the middle one selected (median 3) to be remapped within the LQI range. The following figure illustrates the LQI measurement and how the data is arranged in data memory.

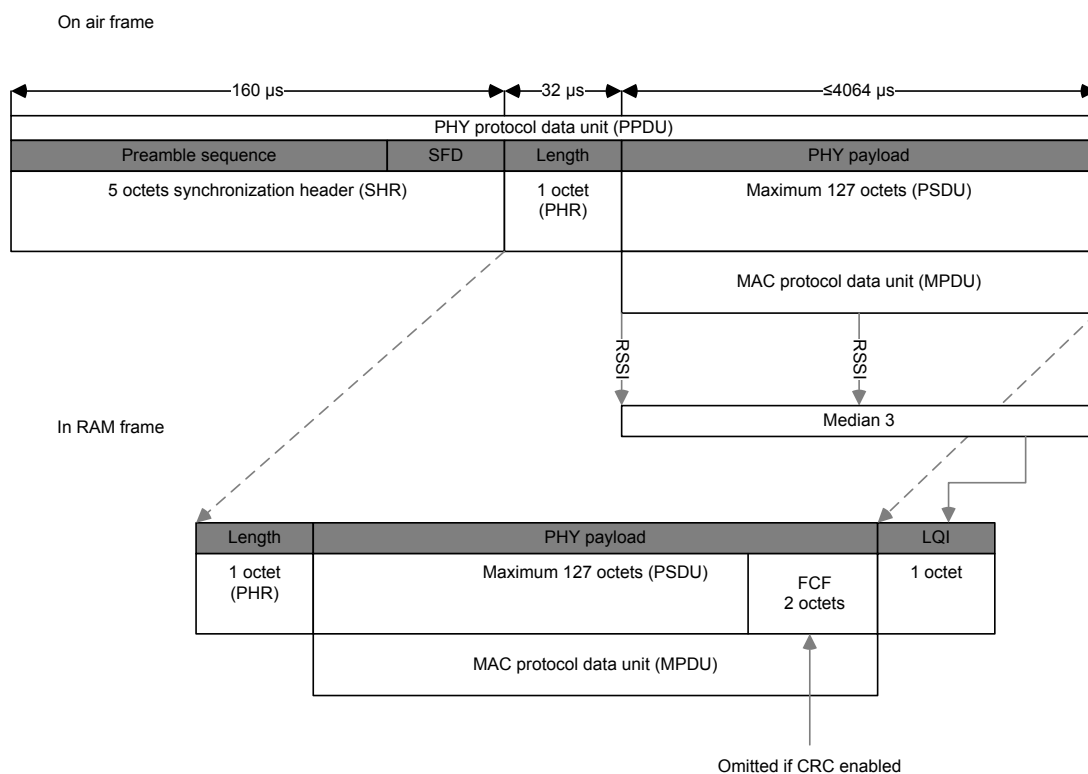


Figure 74: IEEE 802.15.4 frame in data memory

A shortcut has been added between the **FRAMESTART** event and the **BCSTART** task. This can be used to trigger a **BCMATCH** event after N bits, such as when inspecting the MAC addressing fields.

### 6.12.13.8 Interframe spacing (IFS)

The IEEE 802.15.4 standard defines a specific time that is allotted for the MAC sublayer to process received data. Interframe spacing (IFS) is used to prevent two frames from being transmitted too close together. If the transmission is requesting an acknowledgement, the space before the second frame shall be at least one IFS period.

The IFS is determined to be one of the following:

- IFS equals `macMinSIFSPeriod` (12 symbols) if the MPDU is less than or equal to `aMaxSIFSFrameSize` (18 octets) octets
- IFS equals `macMinLIFSPeriod` (40 symbols) if the MPDU is larger than `aMaxSIFSFrameSize`

Using the efficient assisted modes in the RADIO, the **TIFS** will be programmed with the correct value based on the frame being transmitted. If the assisted modes are not in use, the **TIFS** register must be updated manually. The following figure provides details on what IFS period is valid in both acknowledged and unacknowledged transmissions.



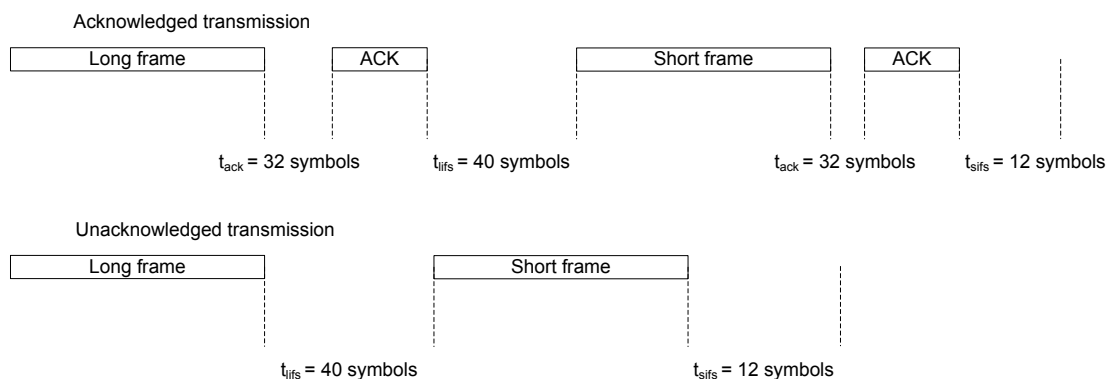


Figure 75: Interframe spacing examples

### 6.12.14 EasyDMA

The RADIO uses EasyDMA to read and write packets to RAM without CPU involvement.

As illustrated in [RADIO block diagram](#) on page 163, the RADIO's EasyDMA utilizes the same [PACKETPTR](#) for receiving and transmitting packets. This pointer should be reconfigured by the CPU each time before RADIO is started by the [START](#) task. The [PACKETPTR](#) register is double-buffered, meaning that it can be updated and prepared for the next transmission.

The [END](#) event indicates that the last bit has been processed by the RADIO. The [DISABLED](#) event is issued to acknowledge that a [DISABLE](#) task is done.

The structure of a packet is described in detail in [Packet configuration](#) on page 163. The data that is stored in Data RAM and transported by EasyDMA consists of the following fields:

- S0
- LENGTH
- S1
- PAYLOAD

In addition, a static add-on is sent immediately after the payload.

The size of each of the above fields in the frame is configurable (see [Packet configuration](#) on page 163), and the space occupied in RAM depends on these settings. The size of the field can be zero, as long as the resulting frame complies with the chosen RF protocol.

All fields are extended in size to align with a byte boundary in RAM. For instance, a 3-bit long field on air will occupy 1 byte in RAM while a 9-bit long field will be extended to 2 bytes.

The packet's elements can be configured as follows:

- CI, TERM1, and TERM2 fields are only present in *Bluetooth*<sup>®</sup> Low Energy Long Range mode
- S0 is configured through the [PCNF0.SOLEN](#) field
- LENGTH is configured through the [PCNF0.LFLEN](#) field
- S1 is configured through the [PCNF0.S1LEN](#) field
- Payload size is configured through the value in RAM corresponding to the LENGTH field
- Static add-on size is configured through the [PCNF1.STATLEN](#) field

The [PCNF1.MAXLEN](#) field configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the LENGTH field of the packet payload exceeds [PCNF1.STATLEN](#), and the LENGTH field in the packet specifies a packet larger than configured in [PCNF1.MAXLEN](#), the payload will be truncated to the length specified in [PCNF1.MAXLEN](#).

**Note:** The `PCNF1.MAXLEN` field includes the payload and the add-on, but excludes the size occupied by the `S0`, `LENGTH`, and `S1` fields. This has to be taken into account when allocating RAM.

If the payload and add-on length is specified larger than `PCNF1.MAXLEN`, the RADIO will still transmit or receive in the same way as before, except the payload is now truncated to `PCNF1.MAXLEN`. The packet's `LENGTH` field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to `PCNF1.MAXLEN`.

**Note:** If `PACKETPTR` is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

The `END` event indicates that the last bit has been processed by the RADIO. The `DISABLED` event is issued to acknowledge that an `DISABLE` task is done.

## 6.12.15 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40001000	RADIO	RADIO	2.4 GHz radio	

Table 62: Instances

Register	Offset	Description
<code>TASKS_TXEN</code>	0x000	Enable RADIO in TX mode
<code>TASKS_RXEN</code>	0x004	Enable RADIO in RX mode
<code>TASKS_START</code>	0x008	Start RADIO
<code>TASKS_STOP</code>	0x00C	Stop RADIO
<code>TASKS_DISABLE</code>	0x010	Disable RADIO
<code>TASKS_RSSISTART</code>	0x014	Start the RSSI and take one single sample of the receive signal strength
<code>TASKS_RSSISTOP</code>	0x018	Stop the RSSI measurement
<code>TASKS_BCSTART</code>	0x01C	Start the bit counter
<code>TASKS_BCSTOP</code>	0x020	Stop the bit counter
<code>TASKS_EDSTART</code>	0x024	Start the energy detect measurement used in IEEE 802.15.4 mode
<code>TASKS_EDSTOP</code>	0x028	Stop the energy detect measurement
<code>TASKS_CCSTART</code>	0x02C	Start the clear channel assessment used in IEEE 802.15.4 mode
<code>TASKS_CCSTOP</code>	0x030	Stop the clear channel assessment
<code>EVENTS_READY</code>	0x100	RADIO has ramped up and is ready to be started
<code>EVENTS_ADDRESS</code>	0x104	Address sent or received
<code>EVENTS_PAYLOAD</code>	0x108	Packet payload sent or received
<code>EVENTS_END</code>	0x10C	Packet sent or received
<code>EVENTS_DISABLED</code>	0x110	RADIO has been disabled
<code>EVENTS_DEVMATCH</code>	0x114	A device address match occurred on the last received packet
<code>EVENTS_DEVMISS</code>	0x118	No device address match occurred on the last received packet
<code>EVENTS_RSSIEND</code>	0x11C	Sampling of receive signal strength complete
<code>EVENTS_BCMATCH</code>	0x128	Bit counter reached bit count value
<code>EVENTS_CRCOK</code>	0x130	Packet received with CRC ok
<code>EVENTS_CRCERROR</code>	0x134	Packet received with CRC error
<code>EVENTS_FRAMESTART</code>	0x138	IEEE 802.15.4 length field received
<code>EVENTS_EDEND</code>	0x13C	Sampling of energy detection complete. A new ED sample is ready for readout from the <code>RADIO.EDSAMPLE</code> register.
<code>EVENTS_EDSTOPPED</code>	0x140	The sampling of energy detection has stopped
<code>EVENTS_CCAIDLE</code>	0x144	Wireless medium in idle - clear to send
<code>EVENTS_CCABUSY</code>	0x148	Wireless medium busy - do not send

Register	Offset	Description
EVENTS_CCASTOPPED	0x14C	The CCA has stopped
EVENTS_RATEBOOST	0x150	Ble_LR CI field received, receive mode is changed from Ble_LR125Kbit to Ble_LR500Kbit.
EVENTS_TXREADY	0x154	RADIO has ramped up and is ready to be started TX path
EVENTS_RXREADY	0x158	RADIO has ramped up and is ready to be started RX path
EVENTS_MHRMATCH	0x15C	MAC header match found
EVENTS_SYNC	0x168	Preamble indicator
EVENTS_PHYEND	0x16C	Generated when last bit is sent on air, or received from air
EVENTS_CTEPRESENT	0x170	CTE is present (early warning right after receiving CTEInfo byte)
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
RXCRC	0x40C	CRC field of previously received packet
DAI	0x410	Device address match index
PDUSTAT	0x414	Payload status
CTESTATUS	0x44C	CTEInfo parsed from received packet
DFESTATUS	0x458	DFE status information
PACKETPTR	0x504	Packet pointer
FREQUENCY	0x508	Frequency
TXPOWER	0x50C	Output power
MODE	0x510	Data rate and modulation
PCNF0	0x514	Packet configuration register 0
PCNF1	0x518	Packet configuration register 1
BASE0	0x51C	Base address 0
BASE1	0x520	Base address 1
PREFIX0	0x524	Prefixes bytes for logical addresses 0-3
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7
TXADDRESS	0x52C	Transmit address select
RXADDRESSES	0x530	Receive address select
CRC CNF	0x534	CRC configuration
CRC POLY	0x538	CRC polynomial
CRC INIT	0x53C	CRC initial value
TIFS	0x544	Interframe spacing in $\mu$ s
RSSISAMPLE	0x548	RSSI sample
STATE	0x550	Current radio state
DATAWHITEIV	0x554	Data whitening initial value
BCC	0x560	Bit counter compare
DAB[n]	0x600	Device address base segment n
DAP[n]	0x620	Device address prefix n
DACNF	0x640	Device address match configuration
MHRMATCHCONF	0x644	Search pattern configuration
MHRMATCHMAS	0x648	Pattern mask
MODECNF0	0x650	Radio mode configuration register 0
SFD	0x660	IEEE 802.15.4 start of frame delimiter
EDCNT	0x664	IEEE 802.15.4 energy detect loop count
EDSAMPLE	0x668	IEEE 802.15.4 energy detect level
CCACTRL	0x66C	IEEE 802.15.4 clear channel assessment control
DFEMODE	0x900	Whether to use Angle-of-Arrival (AOA) or Angle-of-Departure (AOD)
CTEINLINECONF	0x904	Configuration for CTE inline mode
DFCTRL1	0x910	Various configuration for Direction finding
DFCTRL2	0x914	Start offset for Direction finding
SWITCHPATTERN	0x928	GPIO patterns to be used for each antenna

Register	Offset	Description
CLEARPATTERN	0x92C	Clear the GPIO pattern array for antenna control
PSEL.DFEGPIO[0]	0x930	Pin select for DFE pin 0
PSEL.DFEGPIO[1]	0x934	Pin select for DFE pin 1
PSEL.DFEGPIO[2]	0x938	Pin select for DFE pin 2
PSEL.DFEGPIO[3]	0x93C	Pin select for DFE pin 3
PSEL.DFEGPIO[4]	0x940	Pin select for DFE pin 4
PSEL.DFEGPIO[5]	0x944	Pin select for DFE pin 5
PSEL.DFEGPIO[6]	0x948	Pin select for DFE pin 6
PSEL.DFEGPIO[7]	0x94C	Pin select for DFE pin 7
DFEPACKET.PTR	0x950	Data pointer
DFEPACKET.MAXCNT	0x954	Maximum number of buffer words to transfer
DFEPACKET.AMOUNT	0x958	Number of samples transferred in the last transaction
POWER	0xFFC	Peripheral power control

Table 63: Register overview

### 6.12.15.1 TASKS\_TXEN

Address offset: 0x000

Enable RADIO in TX mode

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_TXEN	Trigger	1	Enable RADIO in TX mode Trigger task																											

### 6.12.15.2 TASKS\_RXEN

Address offset: 0x004

Enable RADIO in RX mode

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_RXEN	Trigger	1	Enable RADIO in RX mode Trigger task																											

### 6.12.15.3 TASKS\_START

Address offset: 0x008

Start RADIO

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_START	Trigger	1	Start RADIO Trigger task																											

### 6.12.15.4 TASKS\_STOP

Address offset: 0x00C

Stop RADIO

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_STOP			Stop RADIO																											
		Trigger	1	Trigger task																											

### 6.12.15.5 TASKS\_DISABLE

Address offset: 0x010

Disable RADIO

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_DISABLE			Disable RADIO																											
		Trigger	1	Trigger task																											

### 6.12.15.6 TASKS\_RSSISTART

Address offset: 0x014

Start the RSSI and take one single sample of the receive signal strength

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_RSSISTART			Start the RSSI and take one single sample of the receive signal strength																											
		Trigger	1	Trigger task																											

### 6.12.15.7 TASKS\_RSSISTOP

Address offset: 0x018

Stop the RSSI measurement

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_RSSISTOP			Stop the RSSI measurement																											
		Trigger	1	Trigger task																											

### 6.12.15.8 TASKS\_BCSTART

Address offset: 0x01C

Start the bit counter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_BCSTART			Start the bit counter																												
		Trigger	1	Trigger task																												

### 6.12.15.9 TASKS\_BCSTOP

Address offset: 0x020

Stop the bit counter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_BCSTOP			Stop the bit counter																												
		Trigger	1	Trigger task																												

### 6.12.15.10 TASKS\_EDSTART

Address offset: 0x024

Start the energy detect measurement used in IEEE 802.15.4 mode

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_EDSTART			Start the energy detect measurement used in IEEE 802.15.4 mode																												
		Trigger	1	Trigger task																												

### 6.12.15.11 TASKS\_EDSTOP

Address offset: 0x028

Stop the energy detect measurement

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_EDSTOP			Stop the energy detect measurement																												
		Trigger	1	Trigger task																												

### 6.12.15.12 TASKS\_CCSTART

Address offset: 0x02C

Start the clear channel assessment used in IEEE 802.15.4 mode

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_CCSTART		Start the clear channel assessment used in IEEE 802.15.4 mode																												
		Trigger	1	Trigger task																												

### 6.12.15.13 TASKS\_CCSTOP

Address offset: 0x030

Stop the clear channel assessment

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	TASKS_CCSTOP		Stop the clear channel assessment																												
		Trigger	1	Trigger task																												

### 6.12.15.14 EVENTS\_READY

Address offset: 0x100

RADIO has ramped up and is ready to be started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_READY		RADIO has ramped up and is ready to be started																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.15 EVENTS\_ADDRESS

Address offset: 0x104

Address sent or received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ADDRESS		Address sent or received																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.16 EVENTS\_PAYLOAD

Address offset: 0x108

Packet payload sent or received

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_PAYLOAD			Packet payload sent or received																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.17 EVENTS\_END

Address offset: 0x10C

Packet sent or received

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_END			Packet sent or received																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.18 EVENTS\_DISABLED

Address offset: 0x110

RADIO has been disabled

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_DISABLED			RADIO has been disabled																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.19 EVENTS\_DEVMATCH

Address offset: 0x114

A device address match occurred on the last received packet



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_DEVMATCH		A device address match occurred on the last received packet																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.20 EVENTS\_DEVMISS

Address offset: 0x118

No device address match occurred on the last received packet

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_DEVMISS		No device address match occurred on the last received packet																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.21 EVENTS\_RSSIEND

Address offset: 0x11C

Sampling of receive signal strength complete

A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_RSSIEND		Sampling of receive signal strength complete																												
				A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.22 EVENTS\_BCMATCH

Address offset: 0x128

Bit counter reached bit count value

Bit counter value is specified in the RADIO.BCC register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_BCMATCH		Bit counter reached bit count value																											
				Bit counter value is specified in the RADIO.BCC register																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.23 EVENTS\_CRCOK

Address offset: 0x130

Packet received with CRC ok

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_CRCOK		Packet received with CRC ok																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.24 EVENTS\_CRCERROR

Address offset: 0x134

Packet received with CRC error

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_CRCERROR		Packet received with CRC error																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.25 EVENTS\_FRAMESTART

Address offset: 0x138

IEEE 802.15.4 length field received

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_FRAMESTART		IEEE 802.15.4 length field received																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.26 EVENTS\_EDEND

Address offset: 0x13C

Sampling of energy detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_EDEND		Sampling of energy detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.27 EVENTS\_EDSTOPPED

Address offset: 0x140

The sampling of energy detection has stopped

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_EDSTOPPED		The sampling of energy detection has stopped																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.28 EVENTS\_CCAIDLE

Address offset: 0x144

Wireless medium in idle - clear to send

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_CCAIDLE		Wireless medium in idle - clear to send																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.29 EVENTS\_CCABUSY

Address offset: 0x148

Wireless medium busy - do not send

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_CCABUSY		Wireless medium busy - do not send																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.30 EVENTS\_CCSTOPPED

Address offset: 0x14C

The CCA has stopped

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_CCSTOPPED		The CCA has stopped																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.31 EVENTS\_RATEBOOST

Address offset: 0x150

Ble\_LR CI field received, receive mode is changed from Ble\_LR125Kbit to Ble\_LR500Kbit.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_RATEBOOST		Ble_LR CI field received, receive mode is changed from Ble_LR125Kbit to Ble_LR500Kbit.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.32 EVENTS\_TXREADY

Address offset: 0x154

RADIO has ramped up and is ready to be started TX path

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_TXREADY		RADIO has ramped up and is ready to be started TX path																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.12.15.33 EVENTS\_RXREADY

Address offset: 0x158

RADIO has ramped up and is ready to be started RX path

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_RXREADY		RADIO has ramped up and is ready to be started RX path																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.34 EVENTS\_MHRMATCH

Address offset: 0x15C

MAC header match found

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_MHRMATCH		MAC header match found																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.35 EVENTS\_SYNC

Address offset: 0x168

Preamble indicator

A possible preamble has been received in Ble\_LR125Kbit, Ble\_LR500Kbit, or leee802154\_250Kbit modes during an RX transaction. False triggering of the event is possible.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_SYNC		Preamble indicator																												
				A possible preamble has been received in Ble_LR125Kbit, Ble_LR500Kbit, or leee802154_250Kbit modes during an RX transaction. False triggering of the event is possible.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.36 EVENTS\_PHYEND

Address offset: 0x16C

Generated when last bit is sent on air, or received from air

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_PHYEND			Generated when last bit is sent on air, or received from air																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.37 EVENTS\_CTEPRESENT

Address offset: 0x170

CTE is present (early warning right after receiving CTEInfo byte)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_CTEPRESENT			CTE is present (early warning right after receiving CTEInfo byte)																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.12.15.38 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
ID																U	T	S	R	Q	P	O	N	M	L	K											
Reset 0x00000000	0 0																																				
ID	Acce Field	Value ID	Value	Description																																	
A	RW READY_START			Shortcut between event <a href="#">READY</a> and task <a href="#">START</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
B	RW END_DISABLE			Shortcut between event <a href="#">END</a> and task <a href="#">DISABLE</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
C	RW DISABLED_TXEN			Shortcut between event <a href="#">DISABLED</a> and task <a href="#">TXEN</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
D	RW DISABLED_RXEN			Shortcut between event <a href="#">DISABLED</a> and task <a href="#">RXEN</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
E	RW ADDRESS_RSSISTART			Shortcut between event <a href="#">ADDRESS</a> and task <a href="#">RSSISTART</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
F	RW END_START			Shortcut between event <a href="#">END</a> and task <a href="#">START</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
G	RW ADDRESS_BCSTART			Shortcut between event <a href="#">ADDRESS</a> and task <a href="#">BCSTART</a>																																	
		Disabled	0	Disable shortcut																																	
		Enabled	1	Enable shortcut																																	
H	RW DISABLED_RSSISTOP			Shortcut between event <a href="#">DISABLED</a> and task <a href="#">RSSISTOP</a>																																	

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		U T S R Q P O N M L K H G F E D C B A																											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
K	RW RXREADY_CCASTART			Shortcut between event <b>RXREADY</b> and task <b>CCASTART</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
L	RW CCAIDLE_TXEN			Shortcut between event <b>CCAIDLE</b> and task <b>TXEN</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
M	RW CCABUSY_DISABLE			Shortcut between event <b>CCABUSY</b> and task <b>DISABLE</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
N	RW FRAMESTART_BCSTART			Shortcut between event <b>FRAMESTART</b> and task <b>BCSTART</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
O	RW READY_EDSTART			Shortcut between event <b>READY</b> and task <b>EDSTART</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
P	RW EDEND_DISABLE			Shortcut between event <b>EDEND</b> and task <b>DISABLE</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
Q	RW CCAIDLE_STOP			Shortcut between event <b>CCAIDLE</b> and task <b>STOP</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
R	RW TXREADY_START			Shortcut between event <b>TXREADY</b> and task <b>START</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
S	RW RXREADY_START			Shortcut between event <b>RXREADY</b> and task <b>START</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
T	RW PHYEND_DISABLE			Shortcut between event <b>PHYEND</b> and task <b>DISABLE</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									
U	RW PHYEND_START			Shortcut between event <b>PHYEND</b> and task <b>START</b>																									
		Disabled	0	Disable shortcut																									
		Enabled	1	Enable shortcut																									

### 6.12.15.39 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		a Z Y V U T S R Q P O N M L K I H G F E D C B A																											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
A	RW READY			Write '1' to enable interrupt for event <b>READY</b>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		a Z Y V				U T S R Q P				O N M L K I				H G F E D C B A															
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
B	RW ADDRESS			Write '1' to enable interrupt for event <a href="#">ADDRESS</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
C	RW PAYLOAD			Write '1' to enable interrupt for event <a href="#">PAYLOAD</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
D	RW END			Write '1' to enable interrupt for event <a href="#">END</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
E	RW DISABLED			Write '1' to enable interrupt for event <a href="#">DISABLED</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
F	RW DEVMATCH			Write '1' to enable interrupt for event <a href="#">DEVMATCH</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
G	RW DEVMISS			Write '1' to enable interrupt for event <a href="#">DEVMISS</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
H	RW RSSIEND			Write '1' to enable interrupt for event <a href="#">RSSIEND</a>																									
				A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
I	RW BCMATCH			Write '1' to enable interrupt for event <a href="#">BCMATCH</a>																									
				Bit counter value is specified in the RADIO.BCC register																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
K	RW CRCOK			Write '1' to enable interrupt for event <a href="#">CRCOK</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
L	RW CRCERROR			Write '1' to enable interrupt for event <a href="#">CRCERROR</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
M	RW FRAMESTART			Write '1' to enable interrupt for event <a href="#">FRAMESTART</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
N	RW EDEND			Write '1' to enable interrupt for event <a href="#">EDEND</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		a Z Y				V U T S R Q P O N M L K												I H G F E D C B A											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
O	RW EDSTOPPED	Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">EDSTOPPED</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
P	RW CCAIDLE	Set	1	Write '1' to enable interrupt for event <a href="#">CCAIDLE</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">CCAIDLE</a> Enable																									
Q	RW CCABUSY	Set	1	Write '1' to enable interrupt for event <a href="#">CCABUSY</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">CCABUSY</a> Enable																									
R	RW CCASTOPPED	Set	1	Write '1' to enable interrupt for event <a href="#">CCASTOPPED</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">CCASTOPPED</a> Enable																									
S	RW RATEBOOST	Set	1	Write '1' to enable interrupt for event <a href="#">RATEBOOST</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">RATEBOOST</a> Enable																									
T	RW TXREADY	Set	1	Write '1' to enable interrupt for event <a href="#">TXREADY</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">TXREADY</a> Enable																									
U	RW RXREADY	Set	1	Write '1' to enable interrupt for event <a href="#">RXREADY</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">RXREADY</a> Enable																									
V	RW MHRMATCH	Set	1	Write '1' to enable interrupt for event <a href="#">MHRMATCH</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">MHRMATCH</a> Enable																									
Y	RW SYNC	Set	1	Write '1' to enable interrupt for event <a href="#">SYNC</a> Enable A possible preamble has been received in Ble_LR125Kbit, Ble_LR500Kbit, or leee802154_250Kbit modes during an RX transaction. False triggering of the event is possible.																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">SYNC</a> Enable A possible preamble has been received in Ble_LR125Kbit, Ble_LR500Kbit, or leee802154_250Kbit modes during an RX transaction. False triggering of the event is possible.																									
Z	RW PHYEND	Set	1	Write '1' to enable interrupt for event <a href="#">PHYEND</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">PHYEND</a> Enable																									
a	RW CTYPRESENT	Set	1	Write '1' to enable interrupt for event <a href="#">CTYPRESENT</a> Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
		Set	1	Write '1' to enable interrupt for event <a href="#">CTYPRESENT</a> Enable																									

## 6.12.15.40 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	a Z Y V U T S R Q P O N M L K I H G F E D C B A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value	ID	Value	Description																									
A	RW	READY				Write '1' to disable interrupt for event <a href="#">READY</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
B	RW	ADDRESS				Write '1' to disable interrupt for event <a href="#">ADDRESS</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
C	RW	PAYLOAD				Write '1' to disable interrupt for event <a href="#">PAYLOAD</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
D	RW	END				Write '1' to disable interrupt for event <a href="#">END</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
E	RW	DISABLED				Write '1' to disable interrupt for event <a href="#">DISABLED</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
F	RW	DEVMATCH				Write '1' to disable interrupt for event <a href="#">DEVMATCH</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
G	RW	DEVMISS				Write '1' to disable interrupt for event <a href="#">DEVMISS</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
H	RW	RSSIEND				Write '1' to disable interrupt for event <a href="#">RSSIEND</a>																									
						A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register																									
			Clear	1	Disable																										
Disabled	0	Read: Disabled																													
Enabled	1	Read: Enabled																													
I	RW	BCMATCH				Write '1' to disable interrupt for event <a href="#">BCMATCH</a>																									
						Bit counter value is specified in the RADIO.BCC register																									
			Clear	1	Disable																										
Disabled	0	Read: Disabled																													
Enabled	1	Read: Enabled																													
K	RW	CRCOK				Write '1' to disable interrupt for event <a href="#">CRCOK</a>																									
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
Enabled	1	Read: Enabled																													
L	RW	CRCERROR				Write '1' to disable interrupt for event <a href="#">CRCERROR</a>																									

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		a Z Y				V U T S R Q P O N M L K												I H G F E D C B A											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
M	RW FRAMESTART			Write '1' to disable interrupt for event <a href="#">FRAMESTART</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
N	RW EDEND			Write '1' to disable interrupt for event <a href="#">EDEND</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
O	RW EDSTOPPED			Write '1' to disable interrupt for event <a href="#">EDSTOPPED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
P	RW CCAIDLE			Write '1' to disable interrupt for event <a href="#">CCAIDLE</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
Q	RW CCABUSY			Write '1' to disable interrupt for event <a href="#">CCABUSY</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
R	RW CCASTOPPED			Write '1' to disable interrupt for event <a href="#">CCASTOPPED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
S	RW RATEBOOST			Write '1' to disable interrupt for event <a href="#">RATEBOOST</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
T	RW TXREADY			Write '1' to disable interrupt for event <a href="#">TXREADY</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
U	RW RXREADY			Write '1' to disable interrupt for event <a href="#">RXREADY</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
V	RW MHRMATCH			Write '1' to disable interrupt for event <a href="#">MHRMATCH</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
Y	RW SYNC			Write '1' to disable interrupt for event <a href="#">SYNC</a>																									
				A possible preamble has been received in Ble_LR125Kbit, Ble_LR500Kbit, or leee802154_250Kbit modes during an RX transaction. False triggering of the event is possible.																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	a Z Y V U T S R Q P O N M L K I H G F E D C B A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
Z	RW PHYEND			Write '1' to disable interrupt for event PHYEND																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
a	RW CTEPRESENT			Write '1' to disable interrupt for event CTEPRESENT																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.12.15.41 CRCSTATUS

Address offset: 0x400

CRC status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	R CRCSTATUS			CRC status of packet received																											
		CRCError	0	Packet received with CRC error																											
		CRCOK	1	Packet received with CRC ok																											

### 6.12.15.42 RXMATCH

Address offset: 0x408

Received address

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	R RXMATCH			Received address																											
				Logical address of which previous packet was received																											

### 6.12.15.43 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	R RXCRC			CRC field of previously received packet																											
				CRC field of previously received packet																											

### 6.12.15.44 DAI

Address offset: 0x410

Device address match index

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	DAI		Device address match index																												
				Index (n) of device address, see DAB[n] and DAP[n], that got an address match																												

### 6.12.15.45 PDUSTAT

Address offset: 0x414

Payload status

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													B	B	A	
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	PDUSTAT		Status on payload length vs. PCNF1.MAXLEN																												
		LessThan	0	Payload less than PCNF1.MAXLEN																												
		GreaterThan	1	Payload greater than PCNF1.MAXLEN																												
B	R	CISTAT		Status on what rate packet is received with in Long Range																												
		LR125kbit	0	Frame is received at 125 kbps																												
		LR500kbit	1	Frame is received at 500 kbps																												

### 6.12.15.46 CTESTATUS

Address offset: 0x44C

CTEInfo parsed from received packet

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID																													C	C	B	A	A	A	A
<b>Reset 0x00000000</b>	0 0																																		
ID	Acce Field	Value ID	Value	Description																															
A	R	CTETIME		CTETime parsed from packet																															
B	R	RFU		RFU parsed from packet																															
C	R	CTETYPE		CTEType parsed from packet																															

### 6.12.15.47 DFESTATUS

Address offset: 0x458

DFE status information

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															B	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce	Field	Value ID	Value	Description																													
A	R	SWITCHINGSTATE			Internal state of switching state machine																													
			Idle	0	Switching state Idle																													
			Offset	1	Switching state Offset																													
			Guard	2	Switching state Guard																													
			Ref	3	Switching state Ref																													
			Switching	4	Switching state Switching																													
			Ending	5	Switching state Ending																													
B	R	SAMPLINGSTATE			Internal state of sampling state machine																													
			Idle	0	Sampling state Idle																													
			Sampling	1	Sampling state Sampling																													

### 6.12.15.48 PACKETPTR

Address offset: 0x504

Packet pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PACKETPTR			Packet pointer																										
					Packet address to be used for the next transmission or reception. When transmitting, the packet pointed to by this address will be transmitted and when receiving, the received packet will be written to this address. This address is a byte aligned RAM address. See the memory chapter for details about which memories are available for EasyDMA.																										

### 6.12.15.49 FREQUENCY

Address offset: 0x508

Frequency

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																															B	A	A	A	A	A
<b>Reset 0x00000002</b>	<b>0 1 0</b>																																			
ID	Acce	Field	Value ID	Value	Description																															
A	RW	FREQUENCY		[0..100]	Radio channel frequency																															
					Frequency = 2400 + FREQUENCY (MHz)																															
B	RW	MAP			Channel map selection																															
			Default	0	Channel map between 2400 MHz .. 2500 MHz																															
					Frequency = 2400 + FREQUENCY (MHz)																															
			Low	1	Channel map between 2360 MHz .. 2460 MHz																															
					Frequency = 2360 + FREQUENCY (MHz)																															

### 6.12.15.50 TXPOWER

Address offset: 0x50C



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																								
ID	J J										I H H G G										F E E E E										C	A A A A									
<b>Reset 0x00000000</b>	<b>0 0</b>																																								
ID	Acce	Field	Value ID	Value	Description																																				
A	RW	LFLEN			Length on air of LENGTH field in number of bits																																				
C	RW	SOLEN			Length on air of S0 field in number of bytes																																				
E	RW	S1LEN			Length on air of S1 field in number of bits																																				
F	RW	S1INCL			Include or exclude S1 field in RAM																																				
			Automatic	0	Include S1 field in RAM only if S1LEN > 0																																				
			Include	1	Always include S1 field in RAM independent of S1LEN																																				
G	RW	CILEN			Length of code indicator - long range																																				
H	RW	PLEN			Length of preamble on air. Decision point: TASKS_START task																																				
			8bit	0	8-bit preamble																																				
			16bit	1	16-bit preamble																																				
			32bitZero	2	32-bit zero preamble - used for IEEE 802.15.4																																				
			LongRange	3	Preamble - used for BLE long range																																				
I	RW	CRCINC			Indicates if LENGTH field contains CRC or not																																				
			Exclude	0	LENGTH does not contain CRC																																				
			Include	1	LENGTH includes CRC																																				
J	RW	TERMLEN			Length of TERM field in Long Range operation																																				

### 6.12.15.53 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID											E D										C C C B B B B B B A A A A A A A A A A										
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	MAXLEN		[0..255]	Maximum length of packet payload. If the packet payload is larger than MAXLEN, the radio will truncate the payload to MAXLEN.																										
B	RW	STATLEN		[0..255]	Static length in number of bytes																										
					The static length parameter is added to the total length of the payload when sending and receiving packets, e.g. if the static length is set to N the radio will receive or send N bytes more than what is defined in the LENGTH field of the packet.																										
C	RW	BALEN		[2..4]	Base address length in number of bytes																										
					The address field is composed of the base address and the one byte long address prefix, e.g. set BALEN=2 to get a total address of 3 bytes.																										
D	RW	ENDIAN			On-air endianness of packet, this applies to the S0, LENGTH, S1, and the PAYLOAD fields.																										
			Little	0	Least significant bit on air first																										
			Big	1	Most significant bit on air first																										
E	RW	WHITEEN			Enable or disable packet whitening																										
			Disabled	0	Disable																										
			Enabled	1	Enable																										



### 6.12.15.54 BASE0

Address offset: 0x51C

Base address 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	BASE0			Base address 0																											

### 6.12.15.55 BASE1

Address offset: 0x520

Base address 1

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	BASE1			Base address 1																											

### 6.12.15.56 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A-D	RW	AP[i] (i=0..3)			Address prefix i.																											

### 6.12.15.57 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	D	D	D	D	D	D	D	D	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A-D	RW	AP[i] (i=4..7)			Address prefix i.																											

### 6.12.15.58 TXADDRESS

Address offset: 0x52C

Transmit address select

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A			
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	TXADDRESS		Transmit address select																												
				Logical address to be used when transmitting a packet																												

### 6.12.15.59 RXADDRESSES

Address offset: 0x530

Receive address select

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID																											H	G	F	E	D	C	B	A
Reset	0x00000000																																	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID	Acce Field	Value ID	Value	Description																														
A-H	RW	ADDR[i] (i=0..7)		Enable or disable reception on logical address i.																														
		Disabled	0	Disable																														
		Enabled	1	Enable																														

### 6.12.15.60 CRCCNF

Address offset: 0x534

CRC configuration

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											B	B			A	A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	LEN	[1..3]	CRC length in number of bytes																												
				For MODE Ble_LR125Kbit and Ble_LR500Kbit, only LEN set to 3 is supported																												
		Disabled	0	CRC length is zero and CRC calculation is disabled																												
		One	1	CRC length is one byte and CRC calculation is enabled																												
		Two	2	CRC length is two bytes and CRC calculation is enabled																												
		Three	3	CRC length is three bytes and CRC calculation is enabled																												
B	RW	SKIPADDR		Include or exclude packet address field out of CRC calculation.																												
		Include	0	CRC calculation includes address field																												
		Skip	1	CRC calculation does not include address field. The CRC calculation will start at the first byte after the address.																												
		ieee802154	2	CRC calculation as per 802.15.4 standard. Starting at first byte after length field.																												

### 6.12.15.61 CRCPOLY

Address offset: 0x538

CRC polynomial

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
Reset	0x00000000																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	CRCPOLY		CRC polynomial

Each term in the CRC polynomial is mapped to a bit in this register which index corresponds to the term's exponent. The least significant term/bit is hardwired internally to 1, and bit number 0 of the register content is ignored by the hardware. The following example is for an 8 bit CRC polynomial:  $x^8 + x^7 + x^3 + x^2 + 1 = 1\ 1000\ 1101$ .

### 6.12.15.62 CRCINIT

Address offset: 0x53C

CRC initial value

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
Reset	0x00000000																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	CRCINIT		CRC initial value

Initial value for CRC calculation

### 6.12.15.63 TIFS

Address offset: 0x544

Interframe spacing in  $\mu$ s

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																				
ID																	A																																			
Reset	0x00000000																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	TIFS		Interframe spacing in $\mu$ s.

Interframe space is the time interval between two consecutive packets. It is defined as the time, in microseconds, from the end of the last bit of the previous packet to the start of the first bit of the subsequent packet.

### 6.12.15.64 RSSISAMPLE

Address offset: 0x548

RSSI sample

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A	A	A	A
Reset	0x00000000																															
	0 0																															

ID	Acce Field	Value ID	Value	Description
A	R	RSSISAMPLE	[0..127]	RSSI sample.

RSSI sample result. The value of this register is read as a positive value while the actual received signal strength is a negative value. Actual received signal strength is therefore as follows: received signal strength = -A dBm.

## 6.12.15.65 STATE

Address offset: 0x550

Current radio state

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A	A		
Reset	0x00000000																															
	0 0																															

ID	Acce Field	Value ID	Value	Description
A	R	STATE		Current radio state
		Disabled	0	RADIO is in the Disabled state
		RxRu	1	RADIO is in the RXRU state
		RxIdle	2	RADIO is in the RXIDLE state
		Rx	3	RADIO is in the RX state
		RxDisable	4	RADIO is in the RXDISABLED state
		TxRu	9	RADIO is in the TXRU state
		TxIdle	10	RADIO is in the TXIDLE state
		Tx	11	RADIO is in the TX state
		TxDisable	12	RADIO is in the TXDISABLED state

## 6.12.15.66 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A	A	A	A
Reset	0x00000040																															
	0 1 0 0 0 0 0 0 0																															

ID	Acce Field	Value ID	Value	Description
A	RW	DATAWHITEIV		Data whitening initial value. Bit 6 is hardwired to '1', writing '0' to it has no effect, and it will always be read back and used by the device as '1'.

Bit 0 corresponds to Position 6 of the LSFR, Bit 1 to Position 5, etc.

## 6.12.15.67 BCC

Address offset: 0x560

Bit counter compare



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	MHRMATCHCONF		Search pattern configuration																												

### 6.12.15.72 MHRMATCHMAS

Address offset: 0x648

Pattern mask

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	MHRMATCHMAS		Pattern mask																												

### 6.12.15.73 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									C	C						A
Reset 0x00000200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	RU		Radio ramp-up time																												
		Default	0	Default ramp-up time (tRXEN and tTXEN), compatible with firmware written for nRF51																												
		Fast	1	Fast ramp-up (tRXEN,FAST and tTXEN,FAST), see electrical specifications for more information																												
				When enabled, TIFS is not enforced by hardware and software needs to control when to turn on the Radio																												
C	RW	DTX		Default TX value																												
				Specifies what the RADIO will transmit when it is not started, i.e. between:																												
				RADIO.EVENTS_READY and RADIO.TASKS_START																												
				RADIO.EVENTS_END and RADIO.TASKS_START																												
				RADIO.EVENTS_END and RADIO.EVENTS_DISABLED																												
				For IEEE 802.15.4 250 kbps mode only Center is a valid setting																												
				For Bluetooth Low Energy Long Range mode only Center is a valid setting																												
		B1	0	Transmit '1'																												
		B0	1	Transmit '0'																												
		Center	2	Transmit center frequency																												
				When tuning the crystal for center frequency, the RADIO must be set in DTX = Center mode to be able to achieve the expected accuracy																												

### 6.12.15.74 SFD

Address offset: 0x660

IEEE 802.15.4 start of frame delimiter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x000000A7</b>																									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	SFD		IEEE 802.15.4 start of frame delimiter																																																					

### 6.12.15.75 EDCNT

Address offset: 0x664

IEEE 802.15.4 energy detect loop count

Number of iterations to perform an ED scan. If set to 0 one scan is performed, otherwise the specified number + 1 of ED scans will be performed and the max ED value tracked in EDSAMPLE.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>																									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																			
A	RW	EDCNT		IEEE 802.15.4 energy detect loop count																																																			

### 6.12.15.76 EDSAMPLE

Address offset: 0x668

IEEE 802.15.4 energy detect level

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																									A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>																									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																			
A	R	EDLVL	[0..127]	IEEE 802.15.4 energy detect level																																																			

Register value must be converted to IEEE 802.15.4 range by an 8-bit saturating multiplication by factor ED\_RSSISCALE, as shown in the code example for ED sampling

### 6.12.15.77 CCACTRL

Address offset: 0x66C

IEEE 802.15.4 clear channel assessment control

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	D D D D D D D D C C C C C C C C B B B B B B B B A A A																														
<b>Reset 0x052D0000</b>	<b>0 0 0 0 0 1 0 1 0 0 1 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW CCAMODE			CCA mode of operation																											
		EdMode	0	Energy above threshold																											
				Will report busy whenever energy is detected above CCAEDTHRES																											
		CarrierMode	1	Carrier seen																											
				Will report busy whenever compliant IEEE 802.15.4 signal is seen																											
		CarrierAndEdMode	2	Energy above threshold AND carrier seen																											
		CarrierOrEdMode	3	Energy above threshold OR carrier seen																											
		EdModeTest1	4	Energy above threshold test mode that will abort when first ED measurement over threshold is seen. No averaging.																											
B	RW CCAEDTHRES			CCA energy busy threshold. Used in all the CCA modes except CarrierMode.																											
				Must be converted from IEEE 802.15.4 range by dividing by factor ED_RSSISCALE - similar to EDSAMPLE register																											
C	RW CCACORRTHRES			CCA correlator busy threshold. Only relevant to CarrierMode, CarrierAndEdMode, and CarrierOrEdMode.																											
D	RW CCACORRCNT			Limit for occurrences above CCACORRTHRES. When not equal to zero the correlator based signal detect is enabled.																											

### 6.12.15.78 DFEMODE

Address offset: 0x900

Whether to use Angle-of-Arrival (AOA) or Angle-of-Departure (AOD)

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW DFEOPMODE			Direction finding operation mode																											
		Disabled	0	Direction finding mode disabled																											
		AoD	2	Direction finding mode set to AoD																											
		AoA	3	Direction finding mode set to AoA																											

### 6.12.15.79 CTEINLINECONF

Address offset: 0x904

Configuration for CTE inline mode

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	I I I I I I I I H H H H H H H H G G F F F F E E C B A																														
<b>Reset 0x00002800</b>	<b>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW CTEINLINECTRLLEN			Enable parsing of CTEInfo from received packet in BLE modes																											
		Enabled	1	Parsing of CTEInfo is enabled																											
		Disabled	0	Parsing of CTEInfo is disabled																											
B	RW CTEINFOINS1			CTEInfo is S1 byte or not																											



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	I I I I I I I I H H H H H H H H G G G F F F E E C B A																														
Reset 0x00002800	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0																														
ID	Acce Field	Value ID	Value	Description																											
		InS1	1	CTEInfo is in S1 byte (data PDU)																											
		NotInS1	0	CTEInfo is NOT in S1 byte (advertising PDU)																											
C	RW	CTEERRORHANDLING		Sampling/switching if CRC is not OK																											
		Yes	1	Sampling and antenna switching also when CRC is not OK																											
		No	0	No sampling and antenna switching when CRC is not OK																											
E	RW	CTETIMEVALIDRANGE		Max range of CTETime																											
		20	0	Valid range is 2-20 in BLE core spec. If larger than 20, it can be an indication of an error in the received packet. 20 in 8 $\mu$ s unit (default)																											
		31	1	Set to 20 if parsed CTETime is larger than 20 31 in 8 $\mu$ s unit																											
		63	2	63 in 8 $\mu$ s unit																											
F	RW	CTEINLINERXMODE1US		Spacing between samples for the samples in the SWITCHING period when CTEINLINEMODE is set.																											
		4us	1	When the device is in AoD mode, this is used when the received CTEType is "AoD 1 $\mu$ s". When in AoA mode, this is used when TSWITCHSPACING is 2 $\mu$ s. 4 $\mu$ s																											
		2us	2	2 $\mu$ s																											
		1us	3	1 $\mu$ s																											
		500ns	4	0.5 $\mu$ s																											
		250ns	5	0.25 $\mu$ s																											
		125ns	6	0.125 $\mu$ s																											
G	RW	CTEINLINERXMODE2US		Spacing between samples for the samples in the SWITCHING period when CTEINLINEMODE is set.																											
		4us	1	When the device is in AoD mode, this is used when the received CTEType is "AoD 2 $\mu$ s". When in AoA mode, this is used when TSWITCHSPACING is 4 $\mu$ s. 4 $\mu$ s																											
		2us	2	2 $\mu$ s																											
		1us	3	1 $\mu$ s																											
		500ns	4	0.5 $\mu$ s																											
		250ns	5	0.25 $\mu$ s																											
		125ns	6	0.125 $\mu$ s																											
H	RW	SOCONF		S0 bit pattern to match																											
				The least significant bit always corresponds to the first bit of S0 received.																											
I	RW	SOMASK		S0 bit mask to set which bit to match																											
				The least significant bit always corresponds to the first bit of S0 received.																											

### 6.12.15.80 DFCTRL1

Address offset: 0x910

Various configuration for Direction finding

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	I I I I H H H H G G G F E E E C C C B A A A A A A																														
Reset 0x00023282	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 0 0 0 0 1 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	NUMBEROF8US		Length of the AoA/AoD procedure in number of 8 $\mu$ s units  Always used in TX mode, but in RX mode only when CTEINLINECTRLLEN is 0																											
B	RW	DFEINEXTENSION		Add CTE extension and do antenna switching/sampling in this extension																											
			CRC	1	AoA/AoD procedure triggered at end of CRC																										
			Payload	0	Antenna switching/sampling is done in the packet payload																										
C	RW	TSWITCHSPACING		Interval between every time the antenna is changed in the SWITCHING state																											
			4us	1	4 $\mu$ s																										
			2us	2	2 $\mu$ s																										
			1us	3	1 $\mu$ s																										
E	RW	TSAMPLESPACINGREF		Interval between samples in the REFERENCE period																											
			4us	1	4 $\mu$ s																										
			2us	2	2 $\mu$ s																										
			1us	3	1 $\mu$ s																										
			500ns	4	0.5 $\mu$ s																										
			250ns	5	0.25 $\mu$ s																										
			125ns	6	0.125 $\mu$ s																										
F	RW	SAMPLETYPE		Whether to sample I/Q or magnitude/phase																											
			IQ	0	Complex samples in I and Q																										
			MagPhase	1	Complex samples as magnitude and phase																										
G	RW	TSAMPLESPACING		Interval between samples in the SWITCHING period when CTEINLINECTRLLEN is 0  Not used when CTEINLINECTRLLEN is set. Then either CTEINLINERXMODE1US or CTEINLINERXMODE2US are used.																											
			4us	1	4 $\mu$ s																										
			2us	2	2 $\mu$ s																										
			1us	3	1 $\mu$ s																										
			500ns	4	0.5 $\mu$ s																										
			250ns	5	0.25 $\mu$ s																										
			125ns	6	0.125 $\mu$ s																										
			H	RW	REPEATPATTERN		Repeat each individual antenna pattern N times sequentially, i.e. P0, P0, P1, P1, P2, P2, P3, P3, etc.																								
NoRepeat	0	Do not repeat (1 time in total)																													
I	RW	AGCBACKOFFGAIN		Gain will be lowered by the specified number of gain steps at the start of CTE  First LNAGAIN gain drops, then MIXGAIN, then AAFGAIN																											

### 6.12.15.81 DFCTRL2

Address offset: 0x914

Start offset for Direction finding

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B B B B B B B B B B B B B																A A A A A A A A A A A A A															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	TSWITCHOFFSET		Signed value offset after the end of the CRC before starting switching in number of 16M cycles  Decreasing TSWITCHOFFSET beyond the trigger of the AoA/AoD procedure will have no effect																												
B	RW	TSAMPLEOFFSET		Signed value offset before starting sampling in number of 16M cycles relative to the beginning of the REFERENCE state - 12 $\mu$ s after switching start  Decreasing TSAMPLEOFFSET beyond the trigger of the AoA/AoD procedure will have no effect																												

### 6.12.15.82 SWITCHPATTERN

Address offset: 0x928

GPIO patterns to be used for each antenna

Maximum 8 GPIOs can be controlled. To secure correct signal levels on the pins, the pins must be configured in the GPIO peripheral as described in Pin configuration.

If, during switching, the total number of antenna slots is bigger than the number of written patterns, the RADIO loops back to the pattern used after the reference pattern.

A minimum number of three patterns must be written.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
ID																											A A A A A A A A									
Reset 0x00000000	0 0																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW	SWITCHPATTERN		Fill array of GPIO patterns for antenna control.  The GPIO pattern array size is 40 entries.  When written, bit n corresponds to the GPIO configured in PSEL.DFEGPIO[n].  When read, returns the number of GPIO patterns written since the last time the array was cleared. Use <a href="#">CLEARPATTERN</a> to clear the array.																																

### 6.12.15.83 CLEARPATTERN

Address offset: 0x92C

Clear the GPIO pattern array for antenna control

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	CLEARPATTERN	Clear	Clears GPIO pattern array for antenna control Clear the GPIO pattern																												

### 6.12.15.84 PSEL.DFEGPIO[n] (n=0..7)

Address offset:  $0x930 + (n \times 0x4)$

Pin select for DFE pin n

Must be set before enabling the radio

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	PIN	[0..31]	Pin number																											
C	RW	CONNECT		Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

### 6.12.15.85 DFEPACKET.PTR

Address offset: 0x950

Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	PTR		Data pointer																											

See the memory chapter for details about which memories are available for EasyDMA.

### 6.12.15.86 DFEPACKET.MAXCNT

Address offset: 0x954

Maximum number of buffer words to transfer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																												A A A A A A A A A A A A			
Reset 0x00001000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	MAXCNT		Maximum number of buffer words to transfer																											

### 6.12.15.87 DFEPACKET.AMOUNT

Address offset: 0x958

Number of samples transferred in the last transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																												A A A A A A A A A A A A A A A A A A			
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	R	AMOUNT		Number of samples transferred in the last transaction																											

## 6.12.15.88 POWER

Address offset: 0xFFC

Peripheral power control

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000001	0 1																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	POWER			Peripheral power control. The peripheral and its registers will be reset to its initial state by switching the peripheral off and then back on again.																											
			Disabled	0	Peripheral is powered off																											
			Enabled	1	Peripheral is powered on																											

## 6.12.16 Electrical specification

### 6.12.16.1 General radio characteristics

Symbol	Description	Min.	Typ.	Max.	Units
$f_{OP}$	Operating frequencies	2360		2500	MHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,1M}$	Frequency deviation @ 1 Mbps		±170		kHz
$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1 Mbps		±250		kHz
$f_{DELTA,2M}$	Frequency deviation @ 2 Mbps		±320		kHz
$f_{DELTA,BLE,2M}$	Frequency deviation @ BLE 2 Mbps		±500		kHz
$f_{skBPS}$	On-the-air data rate	125		2000	kbps
$f_{chip, IEEE 802.15.4}$	Chip rate in IEEE 802.15.4 mode		2000		kchip/s

### 6.12.16.2 Radio current consumption (transmitter)

Symbol	Description	Min.	Typ.	Max.	Units
$I_{TX,PLUS8dBm,DCDC}$	TX only run current (DC/DC, 3 V) $P_{RF} = +8$ dBm		14.0		mA
$I_{TX,PLUS8dBm}$	TX only run current $P_{RF} = +8$ dBm		30.0		mA
$I_{TX,PLUS4dBm,DCDC}$	TX only run current (DC/DC, 3 V) $P_{RF} = +4$ dBm		9.4		mA
$I_{TX,PLUS4dBm}$	TX only run current $P_{RF} = +4$ dBm		20.4		mA
$I_{TX,0dBm,DCDC}$	TX only run current (DC/DC, 3 V) $P_{RF} = 0$ dBm		4.9		mA
$I_{TX,0dBm}$	TX only run current $P_{RF} = 0$ dBm		10.4		mA
$I_{TX,MINUS4dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -4$ dBm		3.8		mA
$I_{TX,MINUS4dBm}$	TX only run current $P_{RF} = -4$ dBm		8.1		mA
$I_{TX,MINUS8dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -8$ dBm		3.4		mA
$I_{TX,MINUS8dBm}$	TX only run current $P_{RF} = -8$ dBm		7.1		mA
$I_{TX,MINUS12dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -12$ dBm		3.1		mA
$I_{TX,MINUS12dBm}$	TX only run current $P_{RF} = -12$ dBm		6.4		mA
$I_{TX,MINUS16dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -16$ dBm		2.9		mA
$I_{TX,MINUS16dBm}$	TX only run current $P_{RF} = -16$ dBm		6.0		mA
$I_{TX,MINUS20dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -20$ dBm		2.7		mA
$I_{TX,MINUS20dBm}$	TX only run current $P_{RF} = -20$ dBm		5.6		mA
$I_{TX,MINUS40dBm,DCDC}$	TX only run current DC/DC, 3 V $P_{RF} = -40$ dBm		2.3		mA
$I_{TX,MINUS40dBm}$	TX only run current $P_{RF} = -40$ dBm		4.6		mA
$I_{START,TX,DCDC}$	TX start-up current DC/DC, 3 V, $P_{RF} = 4$ dBm		4.2		mA

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>START,TX</sub>	TX start-up current, P <sub>RF</sub> = 4 dBm		8.8		mA

### 6.12.16.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Typ.	Max.	Units
I <sub>RX,1M,DCDC</sub>	RX only run current (DC/DC, 3 V) 1 Mbps/1 Mbps BLE		4.7		mA
I <sub>RX,1M</sub>	RX only run current (LDO, 3 V) 1 Mbps/1 Mbps BLE		9.8		mA
I <sub>RX,2M,DCDC</sub>	RX only run current (DC/DC, 3 V) 2 Mbps/2 Mbps BLE		5.2		mA
I <sub>RX,2M</sub>	RX only run current (LDO, 3 V) 2 Mbps/2 Mbps BLE		10.9		mA
I <sub>START,RX,1M,DCDC</sub>	RX start-up current (DC/DC, 3 V) 1 Mbps/1 Mbps BLE		3.4		mA
I <sub>START,RX,1M</sub>	RX start-up current 1 Mbps/1 Mbps BLE		6.8		mA

### 6.12.16.4 Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units
P <sub>RF</sub>	Maximum output power		8		dBm
P <sub>RFC</sub>	RF power control range		28		dB
P <sub>RF,CR</sub>	RF power accuracy			±4	dB
P <sub>RF1,1</sub>	1st Adjacent Channel Transmit Power 1 MHz (1 Mbps)		-25		dBc
P <sub>RF2,1</sub>	2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)		-54		dBc
P <sub>RF1,2</sub>	1st Adjacent Channel Transmit Power 2 MHz (2 Mbps)		-26		dBc
P <sub>RF2,2</sub>	2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)		-54		dBc
E <sub>VM</sub>	Error vector magnitude in IEEE 802.15.4 mode (Offset EVM)		2		%rms
P <sub>harm2nd, IEEE 802.15.4</sub>	2nd harmonics in IEEE 802.15.4 mode		-49		dBm
P <sub>harm3rd, IEEE 802.15.4</sub>	3rd harmonics in IEEE 802.15.4 mode		-54		dBm

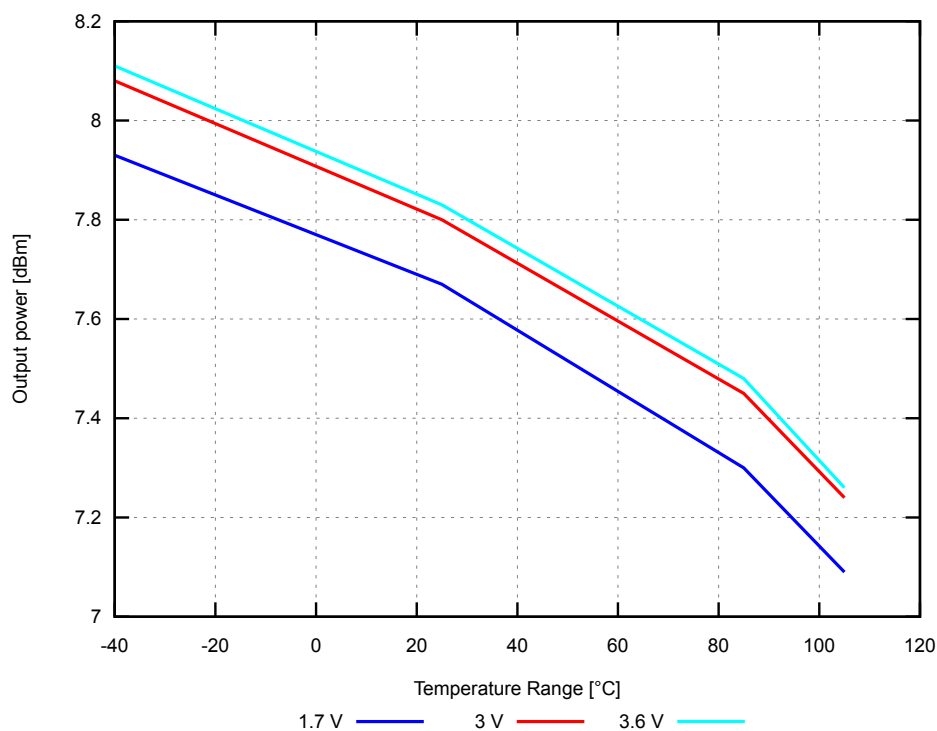


Figure 76: Output power, 1 Mbps Bluetooth low energy mode, at maximum TXPOWER setting (typical values)

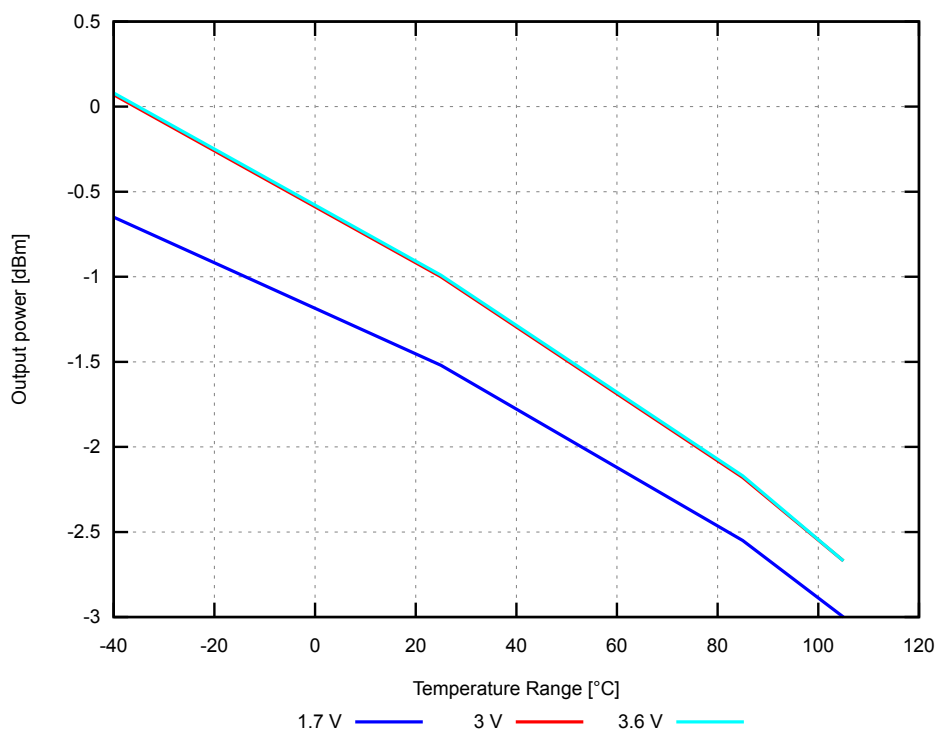


Figure 77: Output power, 1 Mbps Bluetooth low energy mode, at 0 dBm TXPOWER setting (typical values)

### 6.12.16.5 Receiver operation

Symbol	Description	Min.	Typ.	Max.	Units
P <sub>RX,MAX</sub>	Maximum received signal strength at < 0.1% PER		0		dBm
P <sub>SENS,IT,1M</sub>	Sensitivity, 1 Mbps nRF mode ideal transmitter <sup>13</sup>		-92		dBm
P <sub>SENS,IT,2M</sub>	Sensitivity, 2 Mbps nRF mode ideal transmitter <sup>13</sup>		-89		dBm
P <sub>SENS,IT,SP,1M,BLE</sub>	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≤ 37 bytes BER=1E-3 <sup>14</sup>		-95		dBm
P <sub>SENS,IT,LP,1M,BLE</sub>	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≥ 128 bytes BER=1E-4 <sup>15</sup>		-94		dBm
P <sub>SENS,IT,SP,2M,BLE</sub>	Sensitivity, 2 Mbps BLE ideal transmitter, packet length ≤ 37 bytes		-92		dBm
P <sub>SENS,IT,BLE LE125k</sub>	Sensitivity, 125 kbps BLE mode		-103		dBm
P <sub>SENS,IT,BLE LE500k</sub>	Sensitivity, 500 kbps BLE mode		-98		dBm
P <sub>SENS,IEEE 802.15.4</sub>	Sensitivity in IEEE 802.15.4 mode		-99		dBm

<sup>13</sup> Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB.

<sup>14</sup> As defined in the *Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)*.

<sup>15</sup> Equivalent BER limit < 10E-04.

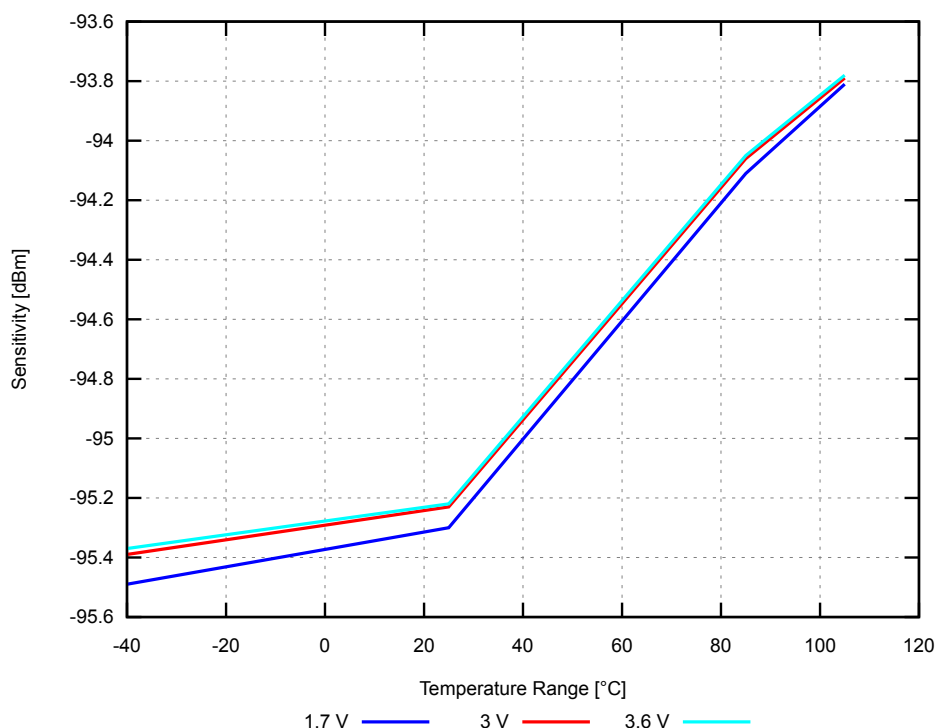


Figure 78: Sensitivity, 1 Mbps Bluetooth low energy mode, Regulator = LDO (typical values)

### 6.12.16.6 RX selectivity

RX selectivity with equal modulation on interfering signal<sup>16</sup>

Symbol	Description	Min.	Typ.	Max.	Units
C/l <sub>1M</sub> ,co-channel	1Mbps mode, co-channel interference		10		dB
C/l <sub>1M</sub> ,-1MHz	1 Mbps mode, Adjacent (-1 MHz) interference		-5		dB
C/l <sub>1M</sub> ,+1MHz	1 Mbps mode, Adjacent (+1 MHz) interference		-14		dB
C/l <sub>1M</sub> ,-2MHz	1 Mbps mode, Adjacent (-2 MHz) interference		-25		dB
C/l <sub>1M</sub> ,+2MHz	1 Mbps mode, Adjacent (+2 MHz) interference		-45		dB
C/l <sub>1M</sub> ,-3MHz	1 Mbps mode, Adjacent (-3 MHz) interference		-40		dB
C/l <sub>1M</sub> ,+3MHz	1 Mbps mode, Adjacent (+3 MHz) interference		-46		dB
C/l <sub>1M</sub> ,≥6MHz	1 Mbps mode, Adjacent (≥6 MHz) interference		-52		dB
C/l <sub>1M</sub> BLE,co-channel	1 Mbps BLE mode, co-channel interference		6		dB
C/l <sub>1M</sub> BLE,-1MHz	1 Mbps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/l <sub>1M</sub> BLE,+1MHz	1 Mbps BLE mode, Adjacent (+1 MHz) interference		-10		dB
C/l <sub>1M</sub> BLE,-2MHz	1 Mbps BLE mode, Adjacent (-2 MHz) interference		-28		dB
C/l <sub>1M</sub> BLE,+2MHz	1 Mbps BLE mode, Adjacent (+2 MHz) interference		-45		dB
C/l <sub>1M</sub> BLE,>3MHz	1 Mbps BLE mode, Adjacent (≥3 MHz) interference		-54		dB
C/l <sub>1M</sub> BLE,image	Image frequency interference		-28		dB
C/l <sub>1M</sub> BLE,image,1MHz	Adjacent (1 MHz) interference to in-band image frequency		-37		dB
C/l <sub>2M</sub> ,co-channel	2 Mbps mode, co-channel interference		10		dB
C/l <sub>2M</sub> ,-2MHz	2 Mbps mode, Adjacent (-2 MHz) interference		-4		dB
C/l <sub>2M</sub> ,+2MHz	2 Mbps mode, Adjacent (+2 MHz) interference		-16		dB
C/l <sub>2M</sub> ,-4MHz	2 Mbps mode, Adjacent (-4 MHz) interference		-22		dB
C/l <sub>2M</sub> ,+4MHz	2 Mbps mode, Adjacent (+4 MHz) interference		-46		dB

<sup>16</sup> Desired signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the desired signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented.



Symbol	Description	Min.	Typ.	Max.	Units
C/l <sub>2M,-6MHz</sub>	2 Mbps mode, Adjacent (-6 MHz) interference		-39		dB
C/l <sub>2M,+6MHz</sub>	2 Mbps mode, Adjacent (+6 MHz) interference		-48		dB
C/l <sub>2M,≥12MHz</sub>	2 Mbps mode, Adjacent (≥12 MHz) interference		-52		dB
C/l <sub>2M BLE,co-channel</sub>	2 Mbps BLE mode, co-channel interference		7		dB
C/l <sub>2M BLE,-2MHz</sub>	2 Mbps BLE mode, Adjacent (-2 MHz) interference		-2		dB
C/l <sub>2M BLE,+2MHz</sub>	2 Mbps BLE mode, Adjacent (+2 MHz) interference		-12		dB
C/l <sub>2M BLE,-4MHz</sub>	2 Mbps BLE mode, Adjacent (-4 MHz) interference		-25		dB
C/l <sub>2M BLE,+4MHz</sub>	2 Mbps BLE mode, Adjacent (+4 MHz) interference		-46		dB
C/l <sub>2M BLE,≥6MHz</sub>	2 Mbps BLE mode, Adjacent (≥6 MHz) interference		-54		dB
C/l <sub>2M BLE,image</sub>	Image frequency interference		-25		dB
C/l <sub>2M BLE,image, 2MHz</sub>	Adjacent (2 MHz) interference to in-band image frequency		-37		dB
C/l <sub>125k BLE LR,co-channel</sub>	125 kbps BLE LR mode, co-channel interference		3		dB
C/l <sub>125k BLE LR,-1MHz</sub>	125 kbps BLE LR mode, Adjacent (-1 MHz) interference		-9		dB
C/l <sub>125k BLE LR,+1MHz</sub>	125 kbps BLE LR mode, Adjacent (+1 MHz) interference		-16		dB
C/l <sub>125k BLE LR,-2MHz</sub>	125 kbps BLE LR mode, Adjacent (-2 MHz) interference		-28		dB
C/l <sub>125k BLE LR,+2MHz</sub>	125 kbps BLE LR mode, Adjacent (+2 MHz) interference		-54		dB
C/l <sub>125k BLE LR,&gt;3MHz</sub>	125 kbps BLE LR mode, Adjacent (≥3 MHz) interference		-60		dB
C/l <sub>125k BLE LR,image</sub>	Image frequency interference		-28		dB
C/l <sub>IEEE 802.15.4,-5MHz</sub>	IEEE 802.15.4 mode, Adjacent (-5 MHz) rejection		-33		dB
C/l <sub>IEEE 802.15.4,+5MHz</sub>	IEEE 802.15.4 mode, Adjacent (+5 MHz) rejection		-38		dB
C/l <sub>IEEE 802.15.4,±10MHz</sub>	IEEE 802.15.4 mode, Alternate (±10 MHz) rejection		-49		dB

### 6.12.16.7 RX intermodulation

RX intermodulation. Desired signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the desired signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

Symbol	Description	Min.	Typ.	Max.	Units
P <sub>IMD,5TH,1M</sub>	IMD performance, 1 Mbps, 5th offset channel, packet length ≤ 37 bytes		-34		dBm
P <sub>IMD,5TH,1M,BLE</sub>	IMD performance, BLE 1 Mbps, 5th offset channel, packet length ≤ 37 bytes		-32		dBm
P <sub>IMD,5TH,2M</sub>	IMD performance, 2 Mbps, 5th offset channel, packet length ≤ 37 bytes		-33		dBm
P <sub>IMD,5TH,2M,BLE</sub>	IMD performance, BLE 2 Mbps, 5th offset channel, packet length ≤ 37 bytes		-32		dBm

### 6.12.16.8 Radio timing

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>TXEN,BLE,1M</sub>	Time between TXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE and 150 μs TIFS)		140		μs
t <sub>TXEN,FAST,BLE,1M</sub>	Time between TXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE with fast ramp-up and 150 μs TIFS)		40		μs
t <sub>TXDIS,BLE,1M</sub>	When in TX, delay between DISABLE task and DISABLED event for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		6		μs
t <sub>RXEN,BLE,1M</sub>	Time between the RXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE)		140		μs
t <sub>RXEN,FAST,BLE,1M</sub>	Time between the RXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE with fast ramp-up)		40		μs

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>RXDIS,BLE,1M</sub>	When in RX, delay between DISABLE task and DISABLED event for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		0		µs
t <sub>TXDIS,BLE,2M</sub>	When in TX, delay between DISABLE task and DISABLED event for MODE = Nrf_2Mbit and MODE = Ble_2Mbit		4		µs
t <sub>RXDIS,BLE,2M</sub>	When in RX, delay between DISABLE task and DISABLED event for MODE = Nrf_2Mbit and MODE = Ble_2Mbit		0		µs
t <sub>TXEN,IEEE 802.15.4</sub>	Time between TXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 mode)		130		µs
t <sub>TXEN,FAST,IEEE 802.15.4</sub>	Time between TXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 mode with fast ramp-up)		40		µs
t <sub>TXDIS,IEEE 802.15.4</sub>	When in TX, delay between DISABLE task and DISABLED event (IEEE 802.15.4 mode)		21		µs
t <sub>RXEN,IEEE 802.15.4</sub>	Time between the RXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 mode)		130		µs
t <sub>RXEN,FAST,IEEE 802.15.4</sub>	Time between the RXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 mode with fast ramp-up)		40		µs
t <sub>RXDIS,IEEE 802.15.4</sub>	When in RX, delay between DISABLE task and DISABLED event (IEEE 802.15.4 mode)		0.5		µs
t <sub>RX-to-TX turnaround</sub>	Maximum TX-to-RX or RX-to-TX turnaround time in IEEE 802.15.4 mode		40		µs

### 6.12.16.9 Received signal strength indicator (RSSI) specifications

Symbol	Description	Min.	Typ.	Max.	Units
RSSI <sub>ACC</sub>	RSSI accuracy <sup>17</sup>		±2		dB
RSSI <sub>RESOLUTION</sub>	RSSI resolution		1		dB
RSSI <sub>PERIOD</sub>	RSSI sampling time from RSSI_START task		0.25		µs
RSSI <sub>SETTLE</sub>	RSSI settling time after signal level change		15		µs

#### 6.12.16.10 Jitter

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>DISABLEDJITTER</sub>	Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled		0.25		µs
t <sub>READYJITTER</sub>	Jitter on READY event relative to TXEN and RXEN task		0.25		µs

### 6.12.16.11 IEEE 802.15.4 mode energy detection constants

Symbol	Description	Min.	Typ.	Max.	Units
ED_RSSISCALE	Scaling value when converting between hardware-reported value and dBm		5		
ED_RSSIOFFS	Offset value when converting between hardware-reported value and dBm		-93		

<sup>17</sup> Valid range -90 to -30 dBm

## 6.13 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

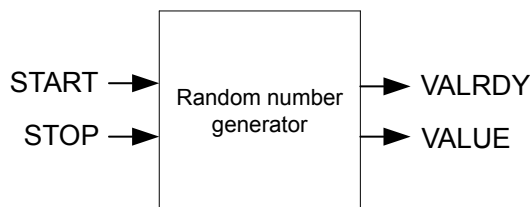


Figure 79: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated, the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

### 6.13.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward 1 or 0. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

### 6.13.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

### 6.13.3 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random number generator	

Table 64: Instances

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

Table 65: Register overview

#### 6.13.3.1 TASKS\_START

Address offset: 0x000

## Task starting the random number generator

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_START			Task starting the random number generator																											
		Trigger	1	Trigger task																											

## 6.13.3.2 TASKS\_STOP

Address offset: 0x004

## Task stopping the random number generator

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_STOP			Task stopping the random number generator																											
		Trigger	1	Trigger task																											

## 6.13.3.3 EVENTS\_VALRDY

Address offset: 0x100

## Event being generated for every new random number written to the VALUE register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_VALRDY			Event being generated for every new random number written to the VALUE register																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

## 6.13.3.4 SHORTS

Address offset: 0x200

## Shortcuts between local events and tasks

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW VALRDY_STOP			Shortcut between event VALRDY and task STOP																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											

## 6.13.3.5 INTENSET

Address offset: 0x304

## Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW VALRDY			Write '1' to enable interrupt for event VALRDY																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

## 6.13.3.6 INTENCLR

Address offset: 0x308

## Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW VALRDY			Write '1' to disable interrupt for event VALRDY																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

## 6.13.3.7 CONFIG

Address offset: 0x504

## Configuration register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW DERCEN			Bias correction																												
		Disabled	0	Disabled																												
		Enabled	1	Enabled																												

## 6.13.3.8 VALUE

Address offset: 0x508

## Output random number

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A A A A A A A A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	R VALUE		[0..255]	Generated random number																												

## 6.13.4 Electrical specification

### 6.13.4.1 RNG Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{RNG,START}}$	Time from setting the START task to generation begins. This is a one-time delay on START signal and does not apply between samples.		128		$\mu\text{s}$
$t_{\text{RNG,RAW}}$	Run time per byte without bias correction. Uniform distribution of 0 and 1 is not guaranteed.		30		$\mu\text{s}$
$t_{\text{RNG,BC}}$	Run time per byte with bias correction. Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed.		120		$\mu\text{s}$

## 6.14 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

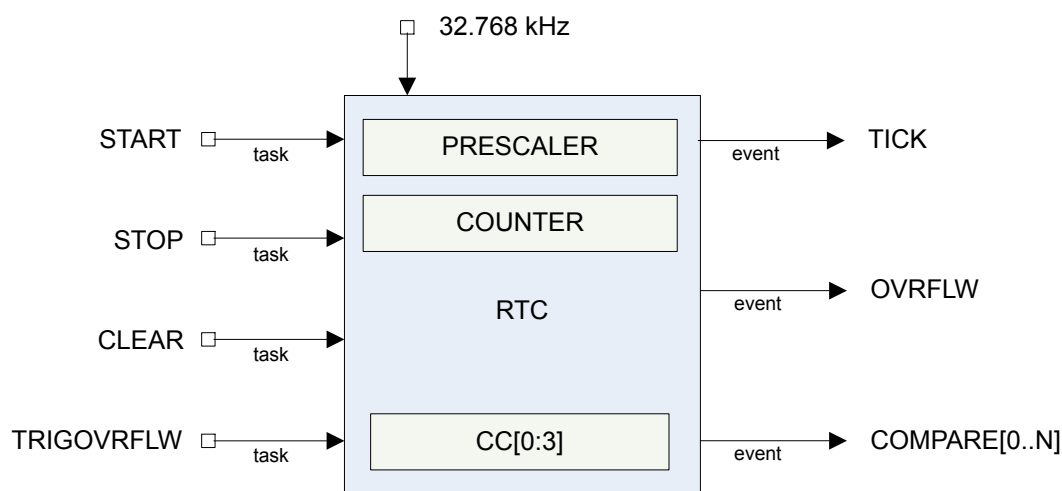


Figure 80: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

### 6.14.1 Clock source

The RTC runs off the LFCLK.

The COUNTER resolution is 30.517  $\mu\text{s}$ . Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitly start LFCLK before using the RTC.

See [CLOCK — Clock control](#) on page 69 for more information about clock sources.

### 6.14.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

$$f_{\text{RTC}} [\text{kHz}] = 32.768 / (\text{PRESCALER} + 1)$$

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR, and TRIGOVFLW, meaning the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples of different frequency configurations are as following:

- Desired COUNTER frequency 100 Hz (10 ms counter period)

$$\text{PRESCALER} = \text{round}(32.768 \text{ kHz} / 100 \text{ Hz}) - 1 = 327$$

$$f_{\text{RTC}} = 99.9 \text{ Hz}$$

$$10009.576 \mu\text{s counter period}$$

- Desired COUNTER frequency 8 Hz (125 ms counter period)

$$\text{PRESCALER} = \text{round}(32.768 \text{ kHz} / 8 \text{ Hz}) - 1 = 4095$$

$$f_{\text{RTC}} = 8 \text{ Hz}$$

$$125 \text{ ms counter period}$$

Prescaler	Counter resolution	Overflow
0	30.517 $\mu\text{s}$	512 seconds
$2^8-1$	7812.5 $\mu\text{s}$	131072 seconds
$2^{12}-1$	125 ms	582.542 hours

Table 66: RTC resolution versus overflow

### 6.14.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

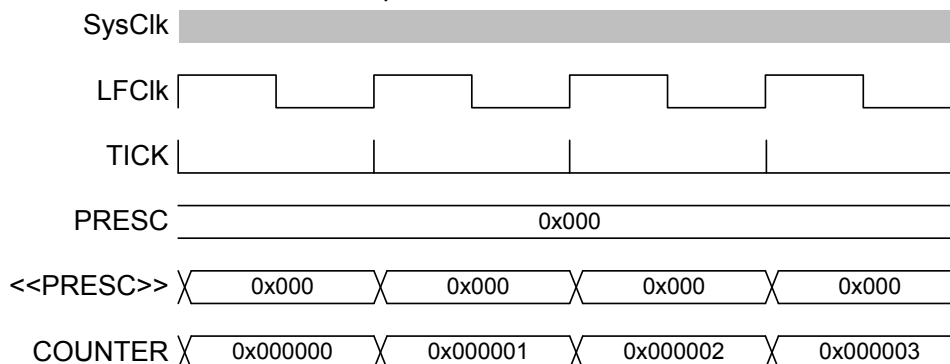


Figure 81: Timing diagram - COUNTER\_PRESCALER\_0

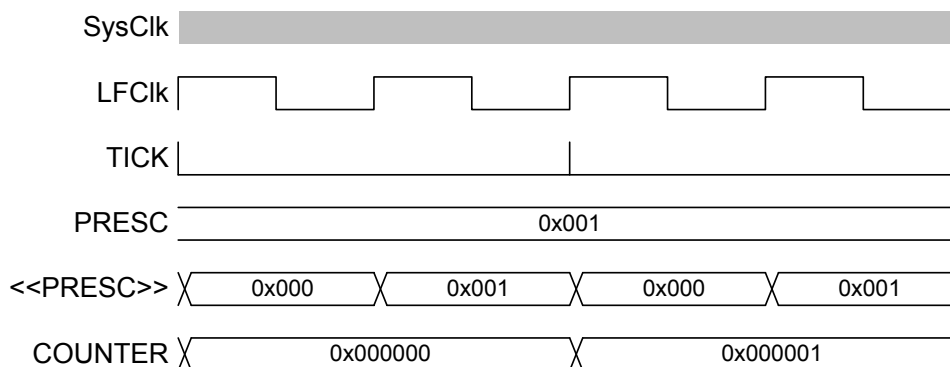


Figure 82: Timing diagram - COUNTER\_PRESCALER\_1

#### 6.14.4 Overflow features

The TRIGOVFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition. OVRFLW occurs when COUNTER overflows from 0xFFFFF to 0.

**Note:** The OVRFLW event is disabled by default.

#### 6.14.5 TICK event

The TICK event enables low power tickless RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM<sup>®</sup> SysTick feature.

Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

**Note:** The TICK event is disabled by default.

#### 6.14.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in [Peripheral interface](#) on page 85. The RTC task and event system is illustrated in [Tasks, events, and interrupts in the RTC](#) on page 233.



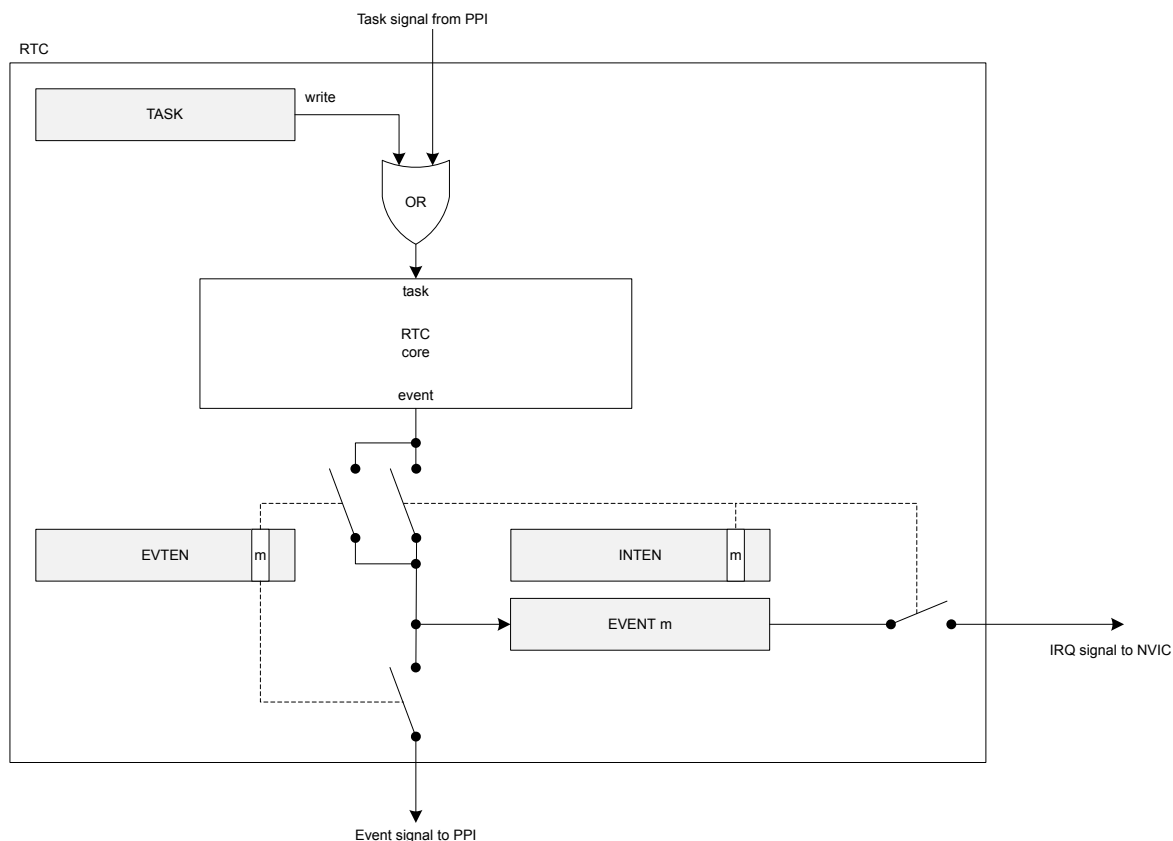


Figure 83: Tasks, events, and interrupts in the RTC

### 6.14.7 Compare feature

There are a number of Compare registers.

For more information, see [Registers](#) on page 238.

When setting a compare register, the following behavior of the RTC compare event should be noted:

- If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.

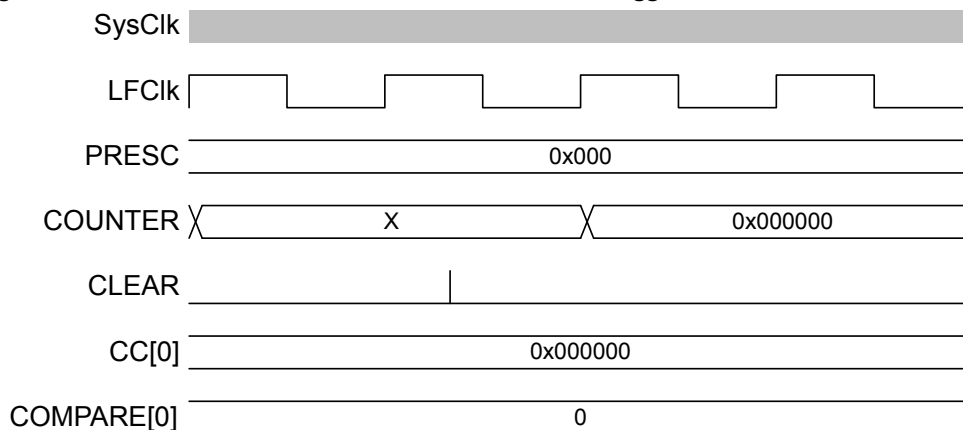


Figure 84: Timing diagram - COMPARE\_CLEAR

- If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

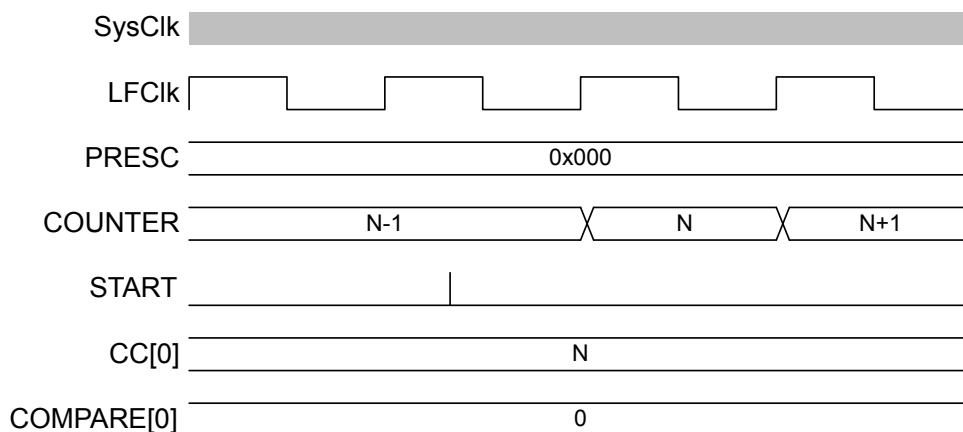


Figure 85: Timing diagram - COMPARE\_START

- COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

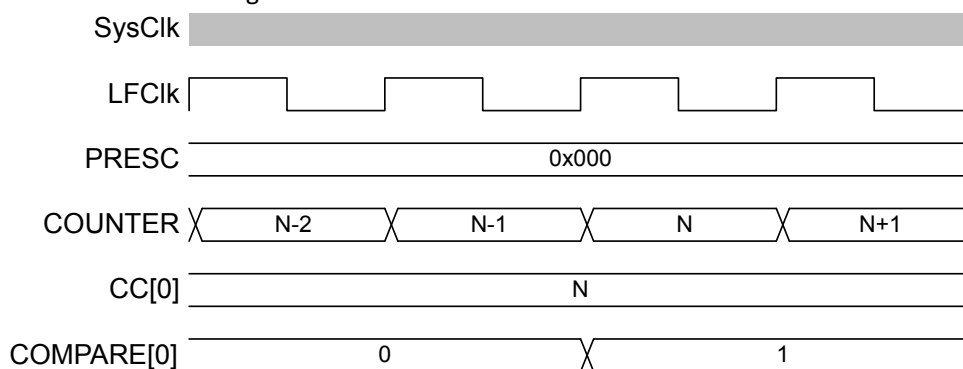


Figure 86: Timing diagram - COMPARE

- If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.

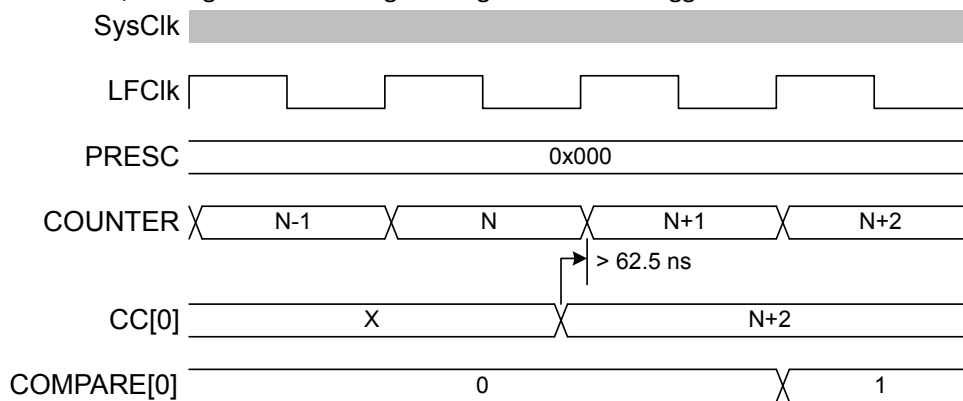


Figure 87: Timing diagram - COMPARE\_N+2

- If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

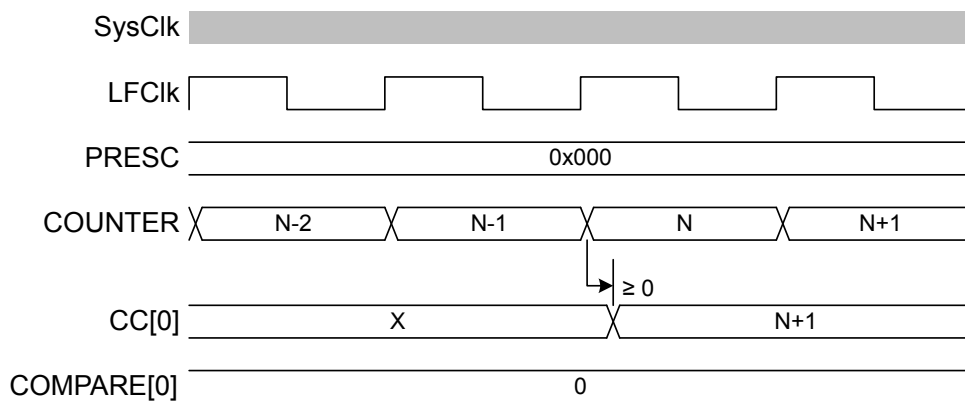


Figure 88: Timing diagram - COMPARE\_N+1

- If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value is greater than N+2 when the new value is written, there will be no event due to the old value.

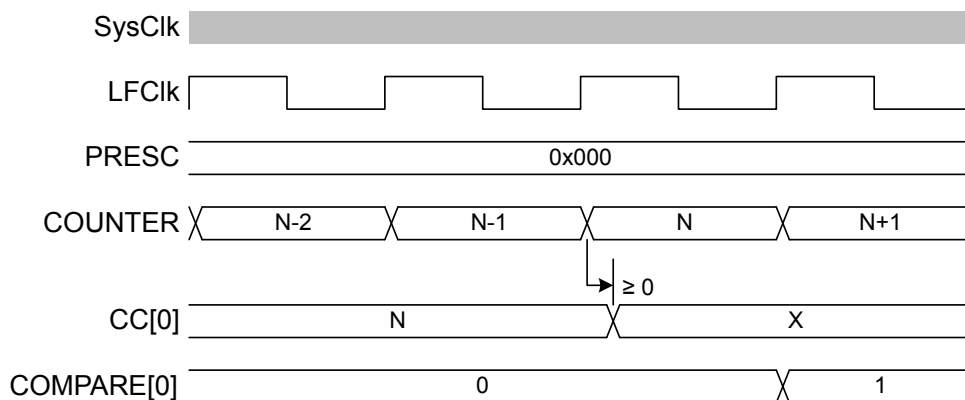


Figure 89: Timing diagram - COMPARE\_N-1

### 6.14.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events.

Task	Delay
CLEAR, STOP, START, TRIGOVRFLOW	+15 to 46 μs

Table 67: RTC jitter magnitudes on tasks

Operation/Function	Jitter
START to COUNTER increment	+/- 15 $\mu$ s
COMPARE to COMPARE <sup>18</sup>	+/- 62.5 ns

Table 68: RTC jitter magnitudes on events

**Note:** 32.768 kHz clock jitter is additional to the numbers provided above.

CLEAR and STOP (and TRIGOVFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585  $\mu$ s and 45.7755  $\mu$ s – rounded to 15  $\mu$ s and 46  $\mu$ s for the remainder of the section.

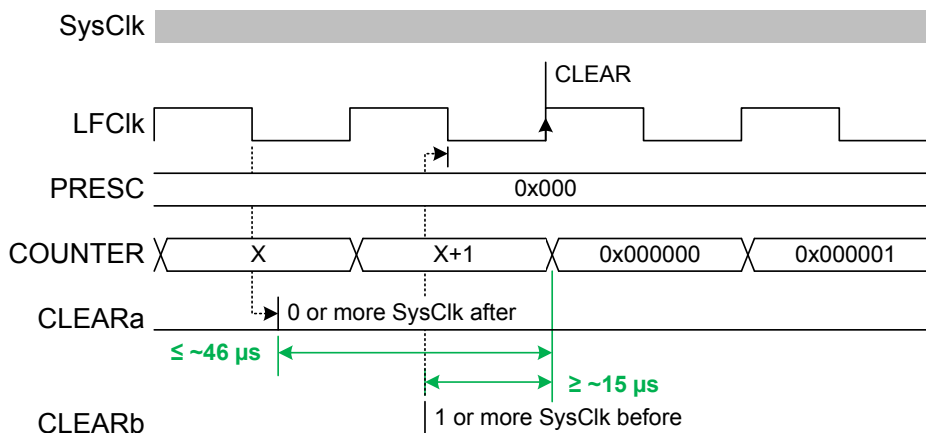


Figure 90: Timing diagram - DELAY\_CLEAR

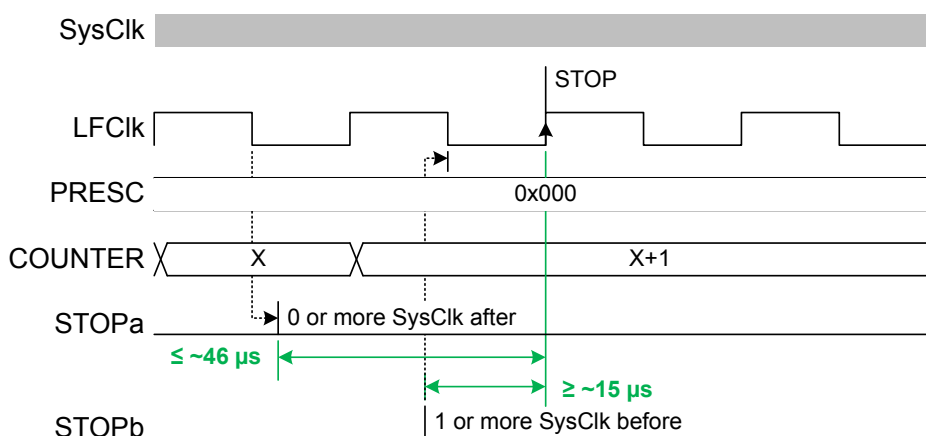


Figure 91: Timing diagram - DELAY\_STOP

The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5  $\mu$ s +/- 15  $\mu$ s. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250  $\mu$ s. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250  $\mu$ s. The figures show the shortest and longest delays on the START task which appears as a +/-15  $\mu$ s jitter on the first COUNTER increment.

<sup>18</sup> Assumes RTC runs continuously between these events.

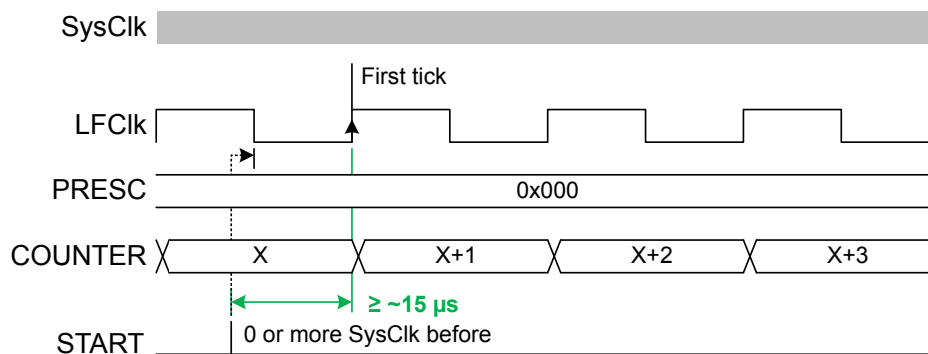


Figure 92: Timing diagram - JITTER\_START-

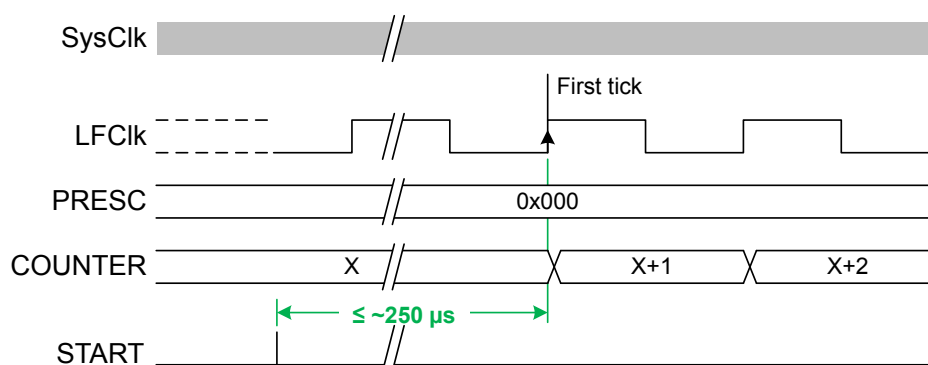


Figure 93: Timing diagram - JITTER\_START+

### 6.14.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

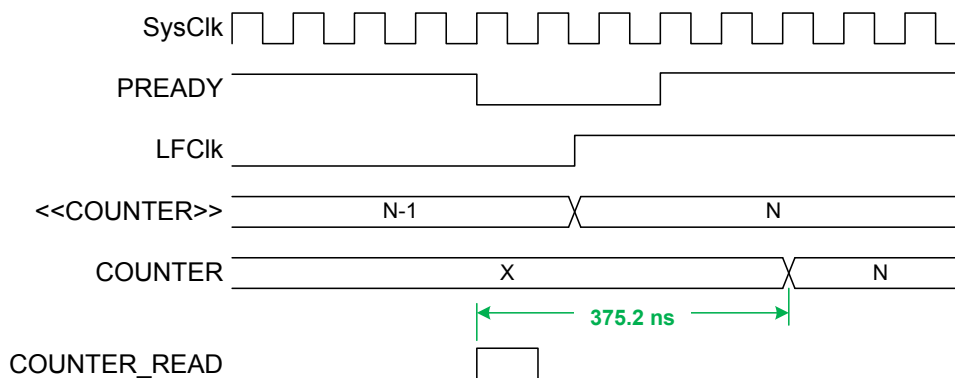


Figure 94: Timing diagram - COUNTER\_READ

## 6.14.10 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[0..2] implemented, CC[3] not implemented
0x40011000	RTC	RTC1	Real-time counter 1	CC[0..3] implemented

Table 69: Instances

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped.
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

Table 70: Register overview

### 6.14.10.1 TASKS\_START

Address offset: 0x000

Start RTC COUNTER

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value	ID	Value	Description																									
A	W	TASKS_START				Start RTC COUNTER																									
			Trigger	1		Trigger task																									

### 6.14.10.2 TASKS\_STOP

Address offset: 0x004

Stop RTC COUNTER

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOP	Trigger	1	Stop RTC COUNTER Trigger task																												

### 6.14.10.3 TASKS\_CLEAR

Address offset: 0x008

Clear RTC COUNTER

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CLEAR	Trigger	1	Clear RTC COUNTER Trigger task																												

### 6.14.10.4 TASKS\_TRIGOVFLW

Address offset: 0x00C

Set COUNTER to 0xFFFFF0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_TRIGOVFLW	Trigger	1	Set COUNTER to 0xFFFFF0 Trigger task																												

### 6.14.10.5 EVENTS\_TICK

Address offset: 0x100

Event on COUNTER increment

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_TICK	NotGenerated	0	Event on COUNTER increment Event not generated																												
		Generated	1	Event generated																												

### 6.14.10.6 EVENTS\_OVRFLW

Address offset: 0x104

Event on COUNTER overflow

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	RW	EVENTS_OVRFLW		Event on COUNTER overflow																													
		NotGenerated	0	Event not generated																													
		Generated	1	Event generated																													

### 6.14.10.7 EVENTS\_COMPARE[n] (n=0..3)

Address offset: 0x140 + (n × 0x4)

Compare event on CC[n] match

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_COMPARE		Compare event on CC[n] match																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.14.10.8 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID														F	E	D	C														B	A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	TICK		Write '1' to enable interrupt for event TICK																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW	OVRFLW		Write '1' to enable interrupt for event OVRFLW																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C-F	RW	COMPARE[i] (i=0..3)		Write '1' to enable interrupt for event COMPARE[i]																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.14.10.9 INTENCLR

Address offset: 0x308

Disable interrupt



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C																												B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW TICK			Write '1' to disable interrupt for event <b>TICK</b>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
B	RW OVRFLW			Write '1' to disable interrupt for event <b>OVRFLW</b>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
C-F	RW COMPARE[i] (i=0..3)			Write '1' to disable interrupt for event <b>COMPARE[i]</b>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.14.10.10 EVTEN

Address offset: 0x340

Enable or disable event routing

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C																												B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW TICK			Enable or disable event routing for event <b>TICK</b>																											
		Disabled	0	Disable																											
		Enabled	1	Disable																											
B	RW OVRFLW			Enable or disable event routing for event <b>OVRFLW</b>																											
		Disabled	0	Disable																											
		Enabled	1	Disable																											
C-F	RW COMPARE[i] (i=0..3)			Enable or disable event routing for event <b>COMPARE[i]</b>																											
		Disabled	0	Disable																											
		Enabled	1	Disable																											

### 6.14.10.11 EVTENSET

Address offset: 0x344

Enable event routing

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C																												B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW TICK			Write '1' to enable event routing for event <b>TICK</b>																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Set	1	Enable																											
B	RW OVRFLW			Write '1' to enable event routing for event <b>OVRFLW</b>																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Set	1	Enable																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C																												B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
C-F	RW COMPARE[i] (i=0..3)			Write '1' to enable event routing for event COMPARE[i]																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Set	1	Enable																											

### 6.14.10.12 EVTENCLR

Address offset: 0x348

Disable event routing

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C																												B A		
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW TICK			Write '1' to disable event routing for event TICK																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Clear	1	Disable																											
B	RW OVRFLW			Write '1' to disable event routing for event OVRFLW																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Clear	1	Disable																											
C-F	RW COMPARE[i] (i=0..3)			Write '1' to disable event routing for event COMPARE[i]																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
		Clear	1	Disable																											

### 6.14.10.13 COUNTER

Address offset: 0x504

Current COUNTER value

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	R	COUNTER		Counter value																											

### 6.14.10.14 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency ( $32768 / (\text{PRESCALER} + 1)$ ). Must be written when RTC is stopped.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	PRESCALER		Prescaler value																											

### 6.14.10.15 CC[n] (n=0..3)

Address offset:  $0x540 + (n \times 0x4)$

Compare register n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value	ID	Value	Description																											
A	RW	COMPARE				Compare value																											

### 6.14.11 Electrical specification

## 6.15 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

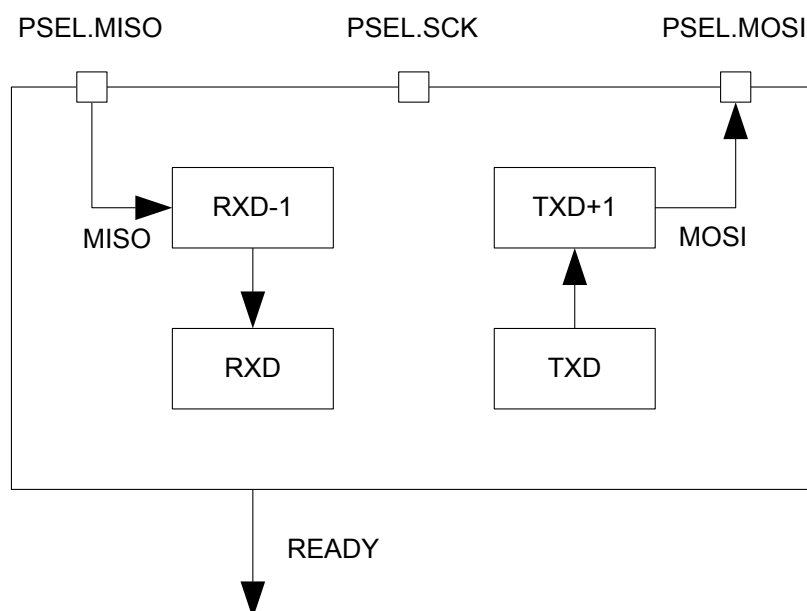


Figure 95: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

### 6.15.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Mode	Clock polarity	Clock phase
	CPOL	CPHA
SPI_MODE0	0 (Leading)	0 (Active high)
SPI_MODE1	0 (Leading)	1 (Active low)
SPI_MODE2	1 (Trailing)	0 (Active high)
SPI_MODE3	1 (Trailing)	1 (Active low)

Table 71: SPI modes

### 6.15.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated SPI master signal is not connected to any physical pin. The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in [GPIO configuration](#) on page 244 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSEL.MOSI	Output	0
MISO	As specified in PSEL.MISO	Input	Not applicable

Table 72: GPIO configuration

### 6.15.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in [Instantiation](#) on page 18 for details on peripherals and their IDs.

### 6.15.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time. This is illustrated in [SPI master transaction](#) on page 245. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the

same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.

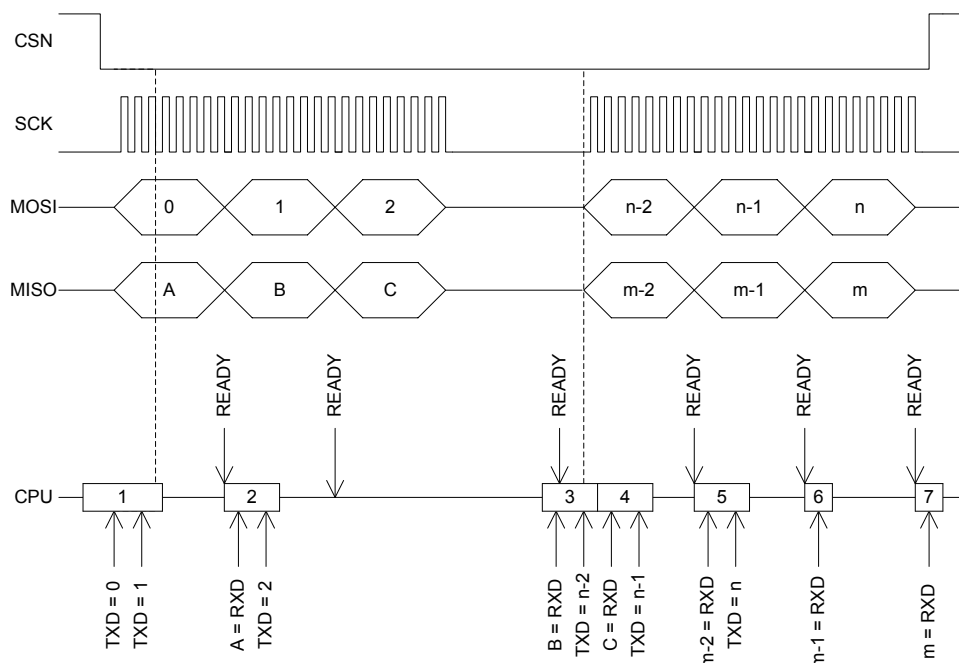


Figure 96: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see [SPI master transaction](#) on page 246. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

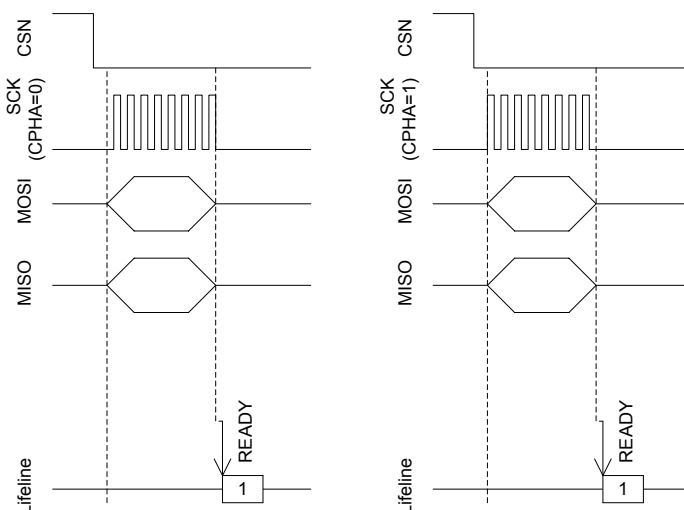


Figure 97: SPI master transaction

## 6.15.2 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPI	SPI0	SPI master 0	Deprecated
0x40004000	SPI	SPI1	SPI master 1	Deprecated

Table 73: Instances

Register	Offset	Description
EVENTS_READY	0x108	TXD byte sent and RXD byte received
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPI
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
CONFIG	0x554	Configuration register

Table 74: Register overview

### 6.15.2.1 EVENTS\_READY

Address offset: 0x108

TXD byte sent and RXD byte received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_READY			TXD byte sent and RXD byte received																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.15.2.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW READY			Write '1' to enable interrupt for event <b>READY</b>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.15.2.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW READY			Write '1' to disable interrupt for event <b>READY</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.15.2.4 ENABLE

Address offset: 0x500

Enable SPI

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A A A A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ENABLE			Enable or disable SPI																												
		Disabled	0	Disable SPI																												
		Enabled	1	Enable SPI																												

### 6.15.2.5 PSEL.SCK

Address offset: 0x508

## Pin select for SCK

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																														
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

## 6.15.2.6 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																														
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

## 6.15.2.7 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																														
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

## 6.15.2.8 RXD

Address offset: 0x518

RXD register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	R			RX data received. Double buffered																											



### 6.15.2.9 TXD

Address offset: 0x51C

TXD register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																											A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0																										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																																																		
A	RW	TXD			TX data to send. Double buffered.																																																		

### 6.15.2.10 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A																							
Reset 0x04000000	0																										0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																																																		
A	RW	FREQUENCY			SPI master data rate																																																		
			K125	0x02000000	125 kbps																																																		
			K250	0x04000000	250 kbps																																																		
			K500	0x08000000	500 kbps																																																		
			M1	0x10000000	1 Mbps																																																		
			M2	0x20000000	2 Mbps																																																		
			M4	0x40000000	4 Mbps																																																		
			M8	0x80000000	8 Mbps																																																		

### 6.15.2.11 CONFIG

Address offset: 0x554

Configuration register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																											C	B	A																										
Reset 0x00000000	0																										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																																																		
A	RW	ORDER			Bit order																																																		
			MsbFirst	0	Most significant bit shifted out first																																																		
			LsbFirst	1	Least significant bit shifted out first																																																		
B	RW	CPHA			Serial clock (SCK) phase																																																		
			Leading	0	Sample on leading edge of clock, shift serial data on trailing edge																																																		
			Trailing	1	Sample on trailing edge of clock, shift serial data on leading edge																																																		
C	RW	CPOL			Serial clock (SCK) polarity																																																		
			ActiveHigh	0	Active high																																																		
			ActiveLow	1	Active low																																																		

## 6.15.3 Electrical specification

### 6.15.3.1 SPI master interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{SPI}}$	Bit rates for SPI <sup>19</sup>			8 <sup>20</sup>	Mbps
$t_{\text{SPI,START}}$	Time from writing TXD register to transmission started		1		$\mu\text{s}$

### 6.15.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{SPI,CSCK}}$	SCK period	125			ns
$t_{\text{SPI,RSCK,LD}}$	SCK rise time, standard drive <sup>21</sup>			$t_{\text{RF},25\text{pF}}$	
$t_{\text{SPI,RSCK,HD}}$	SCK rise time, high drive <sup>21</sup>			$t_{\text{HRF},25\text{pF}}$	
$t_{\text{SPI,FSCK,LD}}$	SCK fall time, standard drive <sup>21</sup>			$t_{\text{RF},25\text{pF}}$	
$t_{\text{SPI,FSCK,HD}}$	SCK fall time, high drive <sup>21</sup>			$t_{\text{HRF},25\text{pF}}$	
$t_{\text{SPI,WHSCK}}$	SCK high time <sup>21</sup>	$(t_{\text{CSCK}}/2)$ $- t_{\text{RSCK}}$			
$t_{\text{SPI,WLSCK}}$	SCK low time <sup>21</sup>	$(t_{\text{CSCK}}/2)$ $- t_{\text{FSCK}}$			
$t_{\text{SPI,SUMI}}$	MISO to CLK edge setup time	19			ns
$t_{\text{SPI,HMI}}$	CLK edge to MISO hold time	18			ns
$t_{\text{SPI,VMO}}$	CLK edge to MOSI valid			59	ns
$t_{\text{SPI,HMO}}$	MOSI hold time after CLK edge	20			ns

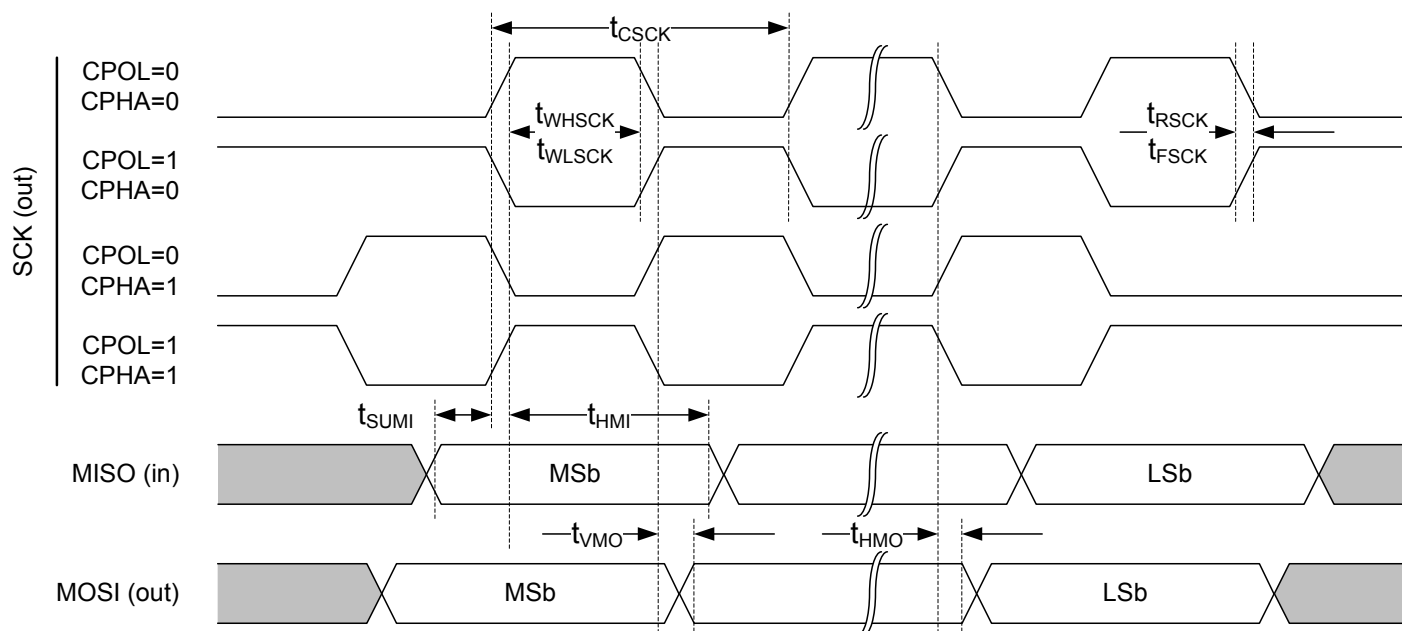


Figure 98: SPI master timing diagram

<sup>19</sup> High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

<sup>20</sup> The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

<sup>21</sup> At 25 pF load, including GPIO capacitance, see [GPIO electrical specification](#).

## 6.16 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple SPI slaves using individual chip select signals for each slave.

Listed here are the main features for the SPIM:

- EasyDMA direct transfer to/from RAM
- SPI mode 0-3
- Individual selection of I/O pins

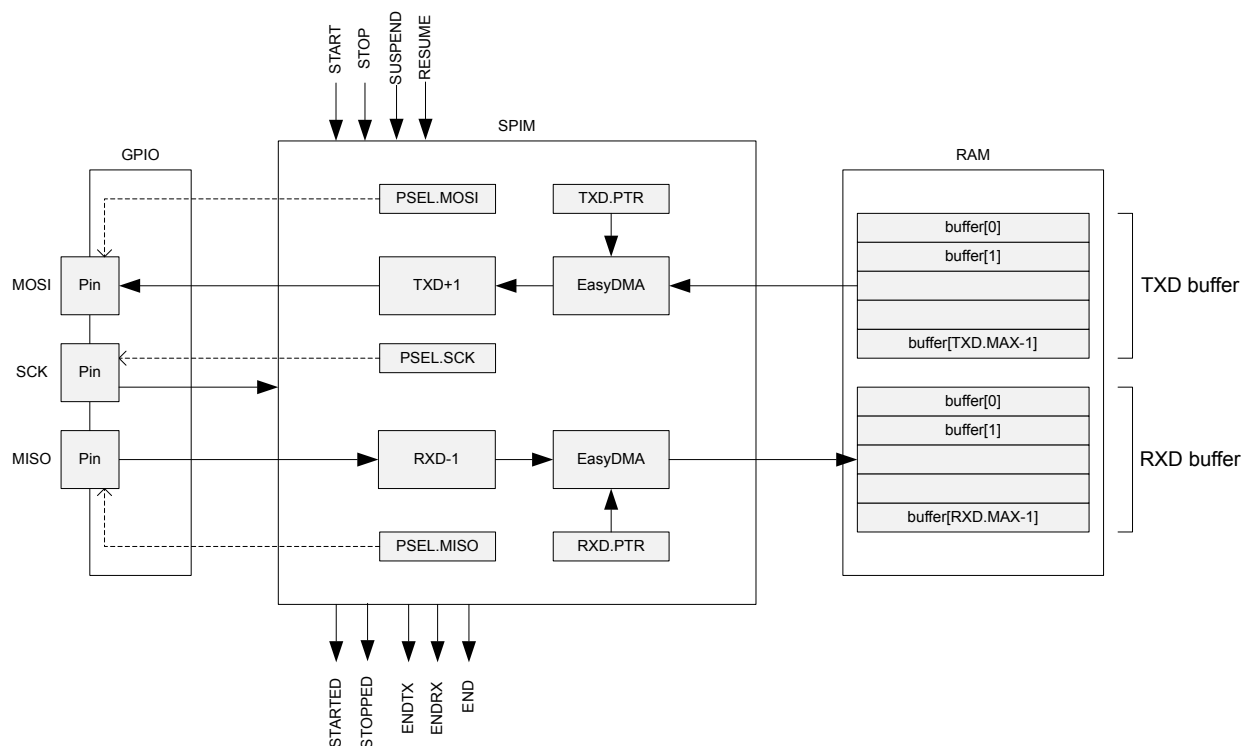


Figure 99: SPIM — SPI master with EasyDMA

### 6.16.1 SPI master transaction sequence

An SPI master transaction is started by triggering the START task. When started, a number of bytes will be transmitted/received on MOSI/MISO.

The following figure illustrates an SPI master transaction.

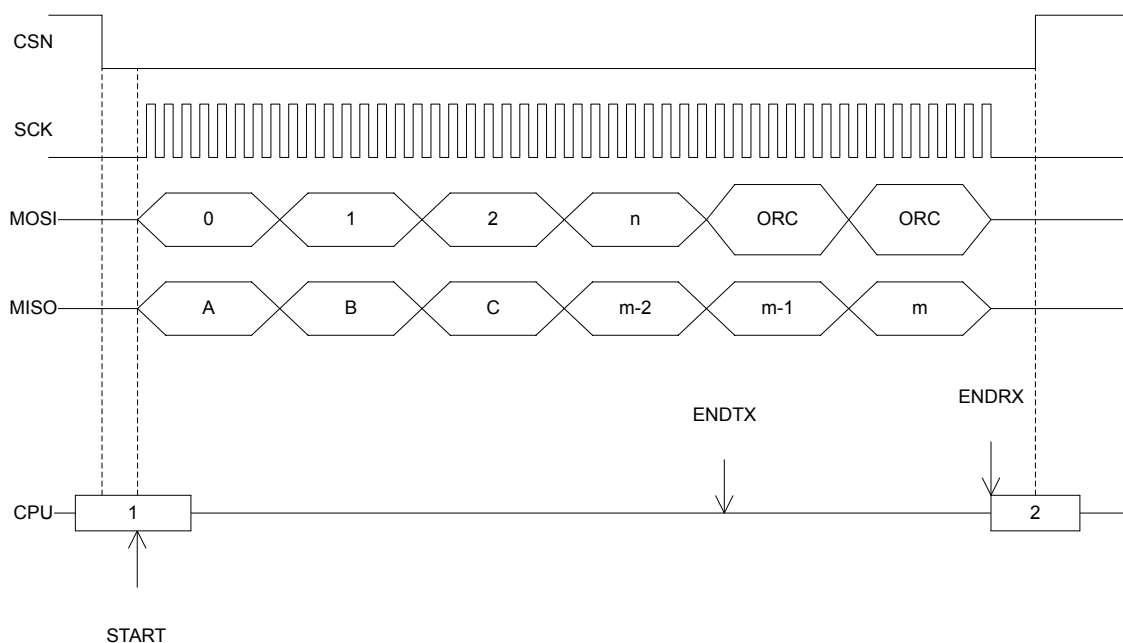


Figure 100: SPI master transaction

The ENDTX is generated when all bytes in buffer `TXD.PTR` on page 261 are transmitted. The number of bytes in the transmit buffer is specified in register `TXD.MAXCNT` on page 261. The ENDRX event will be generated when buffer `RXD.PTR` on page 260 is full, meaning the number of bytes specified in register `RXD.MAXCNT` on page 260 have been received. The transaction stops automatically after all bytes have been transmitted/received. When the maximum number of bytes in the receive buffer is larger than the number of bytes in the transmit buffer, the contents of register `ORC` on page 262 will be transmitted after the last byte in the transmit buffer has been transmitted.

The END event will be generated after both the ENDRX and ENDTX events have been generated.

The SPI master can be stopped in the middle of a transaction by triggering the STOP task. When triggering the STOP task, SPIM will complete the transmission/reception of the current byte before stopping. A STOPPED event is generated when the SPI master has stopped.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the ENDTX event will be generated even if all bytes in the buffer `TXD.PTR` on page 261 have not been transmitted.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the ENDRX event will be generated even if the buffer `RXD.PTR` on page 260 is not full.

A transaction can be suspended and resumed using the SUSPEND and RESUME tasks. When the SUSPEND task is triggered, the SPI master will complete transmitting and receiving the current ongoing byte before it is suspended.

### 6.16.2 Pin configuration

The SCK, MOSI, and MISO signals associated with SPIM are mapped to physical pins according to the configuration specified in the `PSEL.n` registers.

The contents of registers `PSEL.SCK` on page 258, `PSEL.MOSI` on page 259, and `PSEL.MISO` on page 259 are only used when SPIM is enabled, and retained only as long as the device is in System ON mode. The `PSEL.n` registers can only be configured when SPIM is disabled. Enabling/disabling is done using register `ENABLE` on page 258.

To ensure correct behavior, the pins used by SPIM must be configured in the GPIO peripheral as described in [GPIO configuration](#) on page 253 before SPIM is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in <a href="#">PSEL.SCK</a> on page 258	Output	Same as CONFIG.CPOL	
MOSI	As specified in <a href="#">PSEL.MOSI</a> on page 259	Output	0	
MISO	As specified in <a href="#">PSEL.MISO</a> on page 259	Input	Not applicable	

Table 75: GPIO configuration

SPIM does not support automatic control of CSN. The available GPIO pins need to be used to control CSN directly.

SPIM supports SPI modes 0 through 3. The clock polarity (CPOL) and the clock phase (CPHA) are configured in register [CONFIG](#) on page 262.

Mode	Clock polarity	Clock phase
	CPOL	CPHA
SPI_MODE0	0 (Active High)	0 (Leading)
SPI_MODE1	0 (Active High)	1 (Trailing)
SPI_MODE2	1 (Active Low)	0 (Leading)
SPI_MODE3	1 (Active Low)	1 (Trailing)

Table 76: SPI modes

### 6.16.3 EasyDMA

SPIM implements EasyDMA for accessing RAM without CPU involvement.

The SPIM peripheral implements the following EasyDMA channels.

Channel	Type	Register Cluster
TXD	READER	TXD
RXD	WRITER	RXD

Table 77: SPIM EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 37.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be discarded.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

If several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. Data loss will occur in this event.

### 6.16.4 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

### 6.16.5 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIM	SPIM0	SPI master 0	
0x40004000	SPIM	SPIM1	SPI master 1	

Table 78: Instances

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT

Table 79: Register overview

#### 6.16.5.1 TASKS\_START

Address offset: 0x010

## Start SPI transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_START			Start SPI transaction																											
		Trigger	1	Trigger task																											

## 6.16.5.2 TASKS\_STOP

Address offset: 0x014

## Stop SPI transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_STOP			Stop SPI transaction																											
		Trigger	1	Trigger task																											

## 6.16.5.3 TASKS\_SUSPEND

Address offset: 0x01C

## Suspend SPI transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_SUSPEND			Suspend SPI transaction																											
		Trigger	1	Trigger task																											

## 6.16.5.4 TASKS\_RESUME

Address offset: 0x020

## Resume SPI transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	W TASKS_RESUME			Resume SPI transaction																											
		Trigger	1	Trigger task																											

## 6.16.5.5 EVENTS\_STOPPED

Address offset: 0x104

## SPI transaction has stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_STOPPED		SPI transaction has stopped																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.16.5.6 EVENTS\_ENDRX

Address offset: 0x110

End of RXD buffer reached

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ENDRX		End of RXD buffer reached																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.16.5.7 EVENTS\_END

Address offset: 0x118

End of RXD buffer and TXD buffer reached

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_END		End of RXD buffer and TXD buffer reached																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.16.5.8 EVENTS\_ENDTX

Address offset: 0x120

End of TXD buffer reached

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ENDTX		End of TXD buffer reached																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.16.5.9 EVENTS\_STARTED

Address offset: 0x14C

Transaction started



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_STARTED			Transaction started																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.16.5.10 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW END_START			Shortcut between event <a href="#">END</a> and task <a href="#">START</a>																												
		Disabled	0	Disable shortcut																												
		Enabled	1	Enable shortcut																												

### 6.16.5.11 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	E															D			C		B		A									
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW STOPPED			Write '1' to enable interrupt for event <a href="#">STOPPED</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW ENDRX			Write '1' to enable interrupt for event <a href="#">ENDRX</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW END			Write '1' to enable interrupt for event <a href="#">END</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
D	RW ENDTX			Write '1' to enable interrupt for event <a href="#">ENDTX</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
E	RW STARTED			Write '1' to enable interrupt for event <a href="#">STARTED</a>																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.16.5.12 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																									
ID																												E			D			C			B			A		
<b>Reset 0x00000000</b>	<b>0 0</b>																																									
ID	Acce Field	Value ID	Value	Description																																						
A	RW STOPPED			Write '1' to disable interrupt for event <a href="#">STOPPED</a>																																						
		Clear	1	Disable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
B	RW ENDRX			Write '1' to disable interrupt for event <a href="#">ENDRX</a>																																						
		Clear	1	Disable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
C	RW END			Write '1' to disable interrupt for event <a href="#">END</a>																																						
		Clear	1	Disable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
D	RW ENDTX			Write '1' to disable interrupt for event <a href="#">ENDTX</a>																																						
		Clear	1	Disable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						
E	RW STARTED			Write '1' to disable interrupt for event <a href="#">STARTED</a>																																						
		Clear	1	Disable																																						
		Disabled	0	Read: Disabled																																						
		Enabled	1	Read: Enabled																																						

### 6.16.5.13 ENABLE

Address offset: 0x500

Enable SPIM

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																						
ID																												A			A			A			A		
<b>Reset 0x00000000</b>	<b>0 0</b>																																						
ID	Acce Field	Value ID	Value	Description																																			
A	RW ENABLE			Enable or disable SPIM																																			
		Disabled	0	Disable SPIM																																			
		Enabled	7	Enable SPIM																																			

### 6.16.5.14 PSEL.SCK

Address offset: 0x508

Pin select for SCK

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID	C																												A			A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																		
ID	Acce	Field	Value ID	Value	Description																														
A	RW	PIN		[0..31]	Pin number																														
C	RW	CONNECT			Connection																														
			Disconnected	1	Disconnect																														
			Connected	0	Connect																														

### 6.16.5.15 PSEL.MOSI

Address offset: 0x50C

Pin select for MOSI signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID	C																												A			A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																		
ID	Acce	Field	Value ID	Value	Description																														
A	RW	PIN		[0..31]	Pin number																														
C	RW	CONNECT			Connection																														
			Disconnected	1	Disconnect																														
			Connected	0	Connect																														

### 6.16.5.16 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID	C																												A			A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																		
ID	Acce	Field	Value ID	Value	Description																														
A	RW	PIN		[0..31]	Pin number																														
C	RW	CONNECT			Connection																														
			Disconnected	1	Disconnect																														
			Connected	0	Connect																														

### 6.16.5.17 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset	0x04000000																															
0	0 0 0 0 0 1 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	FREQUENCY		SPI master data rate																												
		K125	0x02000000	125 kbps																												
		K250	0x04000000	250 kbps																												
		K500	0x08000000	500 kbps																												
		M1	0x10000000	1 Mbps																												
		M2	0x20000000	2 Mbps																												
		M4	0x40000000	4 Mbps																												
		M8	0x80000000	8 Mbps																												

### 6.16.5.18 RXD.PTR

Address offset: 0x534

Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset	0x00000000																															
0	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	PTR		Data pointer																												
				See the memory chapter for details about which memories are available for EasyDMA.																												

### 6.16.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset	0x00000000																															
0	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[0..0x7fff]	Maximum number of bytes in receive buffer																												

### 6.16.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
Reset	0x00000000																															
0	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNT	[0..0x7fff]	Number of bytes transferred in the last transaction																												

### 6.16.5.21 RXD.LIST

Address offset: 0x540

## EasyDMA list type

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW LIST			List type																												
		Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

### 6.16.5.22 TXD.PTR

Address offset: 0x544

Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A																														A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW PTR			Data pointer																												
				See the memory chapter for details about which memories are available for EasyDMA.																												

### 6.16.5.23 TXD.MAXCNT

Address offset: 0x548

Number of bytes in transmit buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW MAXCNT		[0..0x7fff]	Maximum number of bytes in transmit buffer																												

### 6.16.5.24 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A																														A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	R AMOUNT		[0..0x7fff]	Number of bytes transferred in the last transaction																												

### 6.16.5.25 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A				
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW LIST	Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

### 6.16.5.26 CONFIG

Address offset: 0x554

Configuration register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											C	B	A			
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW ORDER	MsbFirst	0	Most significant bit shifted out first																												
		LsbFirst	1	Least significant bit shifted out first																												
B	RW CPHA	Leading	0	Sample on leading edge of clock, shift serial data on trailing edge																												
		Trailing	1	Sample on trailing edge of clock, shift serial data on leading edge																												
C	RW CPOL	ActiveHigh	0	Active high																												
		ActiveLow	1	Active low																												

### 6.16.5.27 ORC

Address offset: 0x5C0

Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																											A	A	A	A	A	A	A
Reset 0x00000000	0 0																																
ID	Acce Field	Value ID	Value	Description																													
A	RW ORC			Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT.																													

## 6.16.6 Electrical specification

### 6.16.6.1 Timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
f <sub>SPIM</sub>	Bit rates for SPIM <sup>22</sup>			8	Mbps

<sup>22</sup> High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{SPIM,START}}$	Time from START task to transmission started		1		$\mu\text{s}$
$t_{\text{SPIM,CSCK}}$	SCK period	125			ns
$t_{\text{SPIM,RSCK,LD}}$	SCK rise time, standard drive <sup>23</sup>			$t_{\text{RF},25\text{pF}}$	
$t_{\text{SPIM,RSCK,HD}}$	SCK rise time, high drive <sup>23</sup>			$t_{\text{HRF},25\text{pF}}$	
$t_{\text{SPIM,FSCK,LD}}$	SCK fall time, standard drive <sup>23</sup>			$t_{\text{RF},25\text{pF}}$	
$t_{\text{SPIM,FSCK,HD}}$	SCK fall time, high drive <sup>23</sup>			$t_{\text{HRF},25\text{pF}}$	
$t_{\text{SPIM,WHSCK}}$	SCK high time <sup>23</sup>	$(t_{\text{CSCK}}/2)$			
		$-t_{\text{RSCK}}$			
$t_{\text{SPIM,WLSCK}}$	SCK low time <sup>23</sup>	$(t_{\text{CSCK}}/2)$			
		$-t_{\text{FSCK}}$			
$t_{\text{SPIM,SUMI}}$	MISO to CLK edge setup time	19			ns
$t_{\text{SPIM,HMI}}$	CLK edge to MISO hold time	18			ns
$t_{\text{SPIM,VMO}}$	CLK edge to MOSI valid, SCK frequency $\leq 8$ MHz			59	ns
$t_{\text{SPIM,VMO,HS}}$	CLK edge to MOSI valid, SCK frequency $> 8$ MHz			8	ns
$t_{\text{SPIM,HMO}}$	MOSI hold time after CLK edge	20			ns

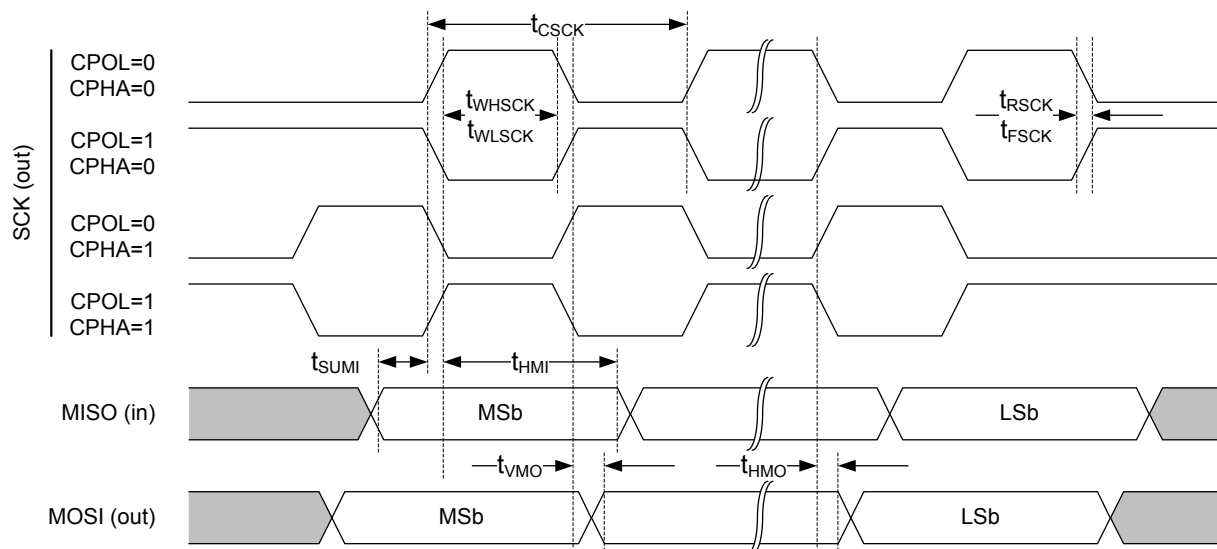


Figure 101: SPIM timing diagram

## 6.17 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra-low power serial communication from an external SPI master. EasyDMA, in conjunction with hardware-based semaphore mechanisms, removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

<sup>23</sup> At 25 pF load, including GPIO pin capacitance, see [GPIO electrical specification](#).

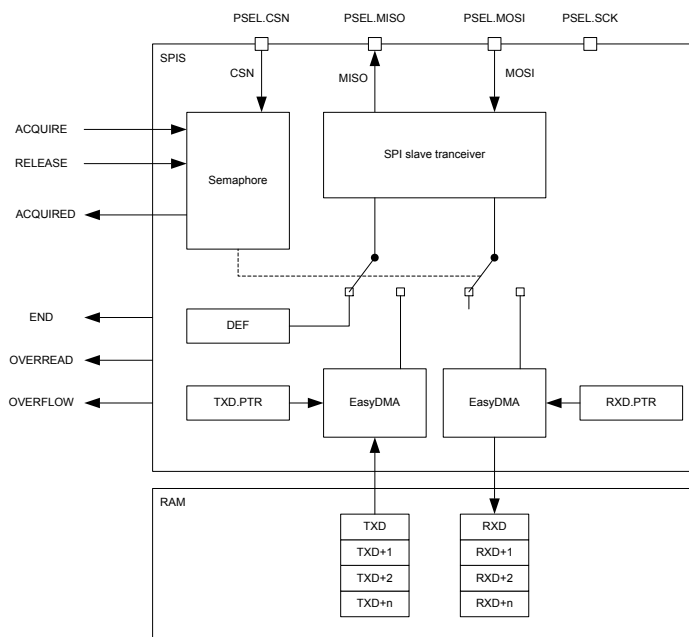


Figure 102: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Mode	Clock polarity	Clock phase
	CPOL	CPHA
SPI_MODE0	0 (Active High)	0 (Trailing Edge)
SPI_MODE1	0 (Active High)	1 (Leading Edge)
SPI_MODE2	1 (Active Low)	0 (Trailing Edge)
SPI_MODE3	1 (Active Low)	1 (Leading Edge)

Table 80: SPI modes

### 6.17.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in [Instantiation](#) on page 18 shows which peripherals have the same ID as the SPI slave.

### 6.17.2 EasyDMA

The SPIS implements EasyDMA for accessing RAM without CPU involvement.

The SPIS peripheral implements the following EasyDMA channels.



Channel	Type	Register Cluster
TXD	READER	TXD
RXD	WRITER	RXD

Table 81: SPIS EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 37.

If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

The END event indicates that EasyDMA has finished accessing the buffer in RAM.

### 6.17.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See [SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 266.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers, it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in [SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 266. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in [SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 266, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available, the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END\_ACQUIRE shortcut can be used. With this shortcut enabled, the semaphore will be handed over to the CPU automatically after the granted transaction has completed. This enables the CPU to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END\_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.

The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction. This does not include the ORC (over-read) characters. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

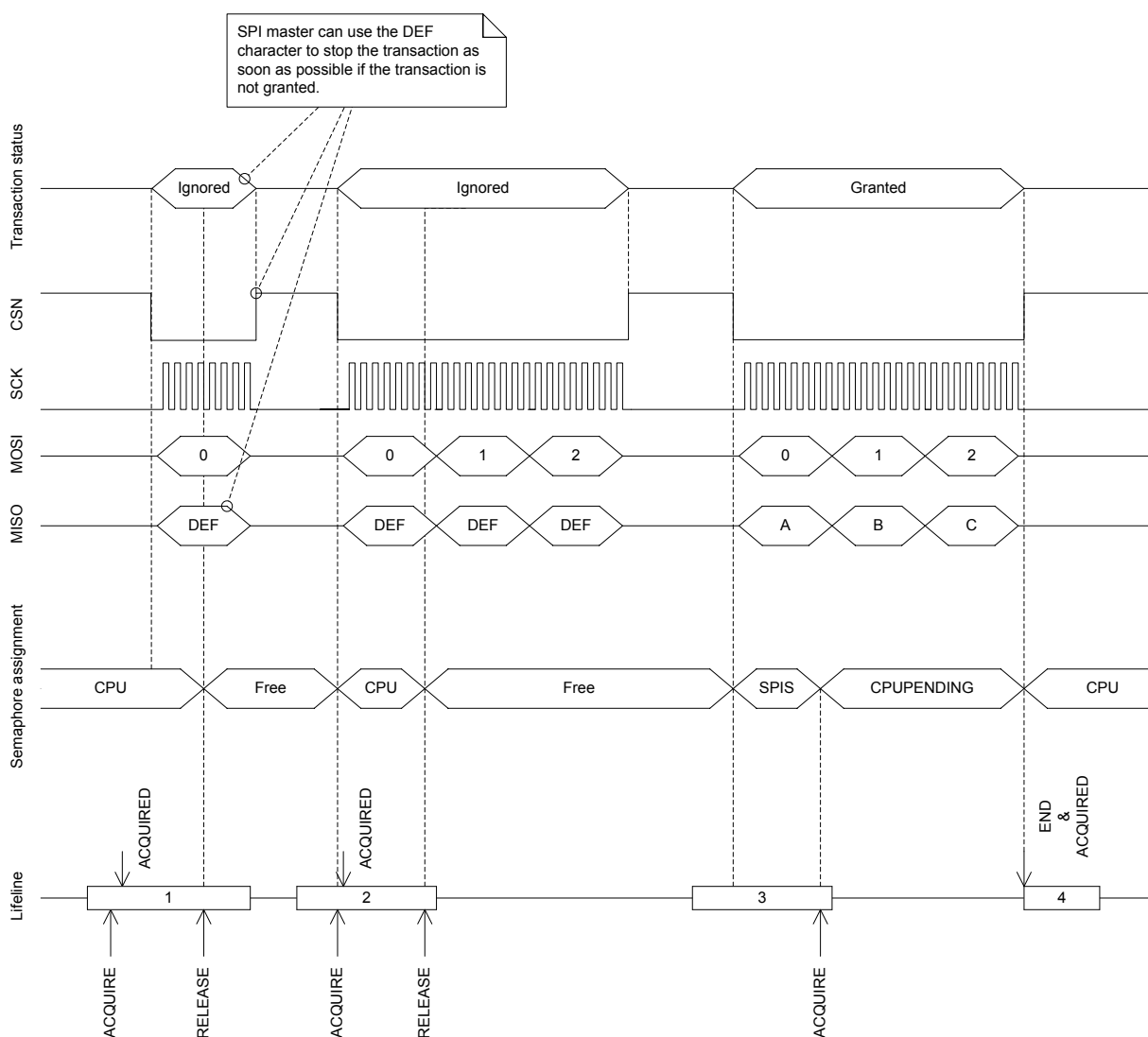


Figure 103: SPI transaction when shortcut between END and ACQUIRE is enabled

## 6.17.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode. See [POWER — Power supply](#) on page 49 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in [GPIO configuration before enabling peripheral](#) on page 267 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

Table 82: GPIO configuration before enabling peripheral

## 6.17.5 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIS	SPI0	SPI slave 0	
0x40004000	SPIS	SPI1	SPI slave 1	

Table 83: Instances

Register	Offset	Description
TASKS_ACQUIRE	0x024	Acquire SPI semaphore
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it
EVENTS_END	0x104	Granted transaction completed
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_ACQUIRED	0x128	Semaphore acquired
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
SEMSTAT	0x400	Semaphore status register
STATUS	0x440	Status from last transaction
ENABLE	0x500	Enable SPI slave
PSEL.SCK	0x508	Pin select for SCK
PSEL.MISO	0x50C	Pin select for MISO signal

Register	Offset	Description	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
RXD.LIST	0x540	EasyDMA list type	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
TXD.LIST	0x550	EasyDMA list type	
CONFIG	0x554	Configuration register	
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.	
ORC	0x5C0	Over-read character	

Table 84: Register overview

### 6.17.5.1 TASKS\_ACQUIRE

Address offset: 0x024

Acquire SPI semaphore

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_ACQUIRE		Acquire SPI semaphore																											
		Trigger	1	Trigger task																											

### 6.17.5.2 TASKS\_RELEASE

Address offset: 0x028

Release SPI semaphore, enabling the SPI slave to acquire it

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	W	TASKS_RELEASE		Release SPI semaphore, enabling the SPI slave to acquire it																											
		Trigger	1	Trigger task																											

### 6.17.5.3 EVENTS\_END

Address offset: 0x104

Granted transaction completed

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_END		Granted transaction completed																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.17.5.4 EVENTS\_ENDRX

Address offset: 0x110

End of RXD buffer reached

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDRX		End of RXD buffer reached																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.17.5.5 EVENTS\_ACQUIRED

Address offset: 0x128

Semaphore acquired

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ACQUIRED		Semaphore acquired																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.17.5.6 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	END_ACQUIRE		Shortcut between event <b>END</b> and task <b>ACQUIRE</b>																											
		Disabled	0	Disable shortcut																											
		Enabled	1	Enable shortcut																											

### 6.17.5.7 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																												C			B		A
Reset 0x00000000	0 0																																
ID	Acce Field	Value ID	Value	Description																													
A	RW END			Write '1' to enable interrupt for event <a href="#">END</a>																													
		Set	1	Enable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
B	RW ENDRX			Write '1' to enable interrupt for event <a href="#">ENDRX</a>																													
		Set	1	Enable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
C	RW ACQUIRED			Write '1' to enable interrupt for event <a href="#">ACQUIRED</a>																													
		Set	1	Enable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													

### 6.17.5.8 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																												C			B		A
Reset 0x00000000	0 0																																
ID	Acce Field	Value ID	Value	Description																													
A	RW END			Write '1' to disable interrupt for event <a href="#">END</a>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
B	RW ENDRX			Write '1' to disable interrupt for event <a href="#">ENDRX</a>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
C	RW ACQUIRED			Write '1' to disable interrupt for event <a href="#">ACQUIRED</a>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													

### 6.17.5.9 SEMSTAT

Address offset: 0x400

Semaphore status register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A				
<b>Reset 0x00000001</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ID	Acce	Field	Value ID	Value	Description																											
A	R	SEMSTAT			Semaphore status																											
			Free	0	Semaphore is free																											
			CPU	1	Semaphore is assigned to CPU																											
			SPIS	2	Semaphore is assigned to SPI slave																											
			CPUPending	3	Semaphore is assigned to SPI but a handover to the CPU is pending																											

### 6.17.5.10 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a 1 to the bits that shall be cleared

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											B	A				
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	RW	OVERREAD			TX buffer over-read detected, and prevented																											
			NotPresent	0	Read: error not present																											
			Present	1	Read: error present																											
			Clear	1	Write: clear error on writing '1'																											
B	RW	OVERFLOW			RX buffer overflow detected, and prevented																											
			NotPresent	0	Read: error not present																											
			Present	1	Read: error present																											
			Clear	1	Write: clear error on writing '1'																											

### 6.17.5.11 ENABLE

Address offset: 0x500

Enable SPI slave

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A	A		
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	RW	ENABLE			Enable or disable SPI slave																											
			Disabled	0	Disable SPI slave																											
			Enabled	2	Enable SPI slave																											

### 6.17.5.12 PSEL.SCK

Address offset: 0x508

Pin select for SCK

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

### 6.17.5.13 PSEL.MISO

Address offset: 0x50C

Pin select for MISO signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

### 6.17.5.14 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											

### 6.17.5.15 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PIN		[0..31]	Pin number																											
C	RW CONNECT			Connection																											
		Disconnected	1	Disconnect																											
		Connected	0	Connect																											



### 6.17.5.16 PSELCK ( Deprecated )

Address offset: 0x508

Pin select for SCK

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW PSELCK	Disconnected	[0..31] 0xFFFFFFFF	Pin number configuration for SPI SCK signal Disconnect																												

### 6.17.5.17 PSELMISO ( Deprecated )

Address offset: 0x50C

Pin select for MISO

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW PSELMISO	Disconnected	[0..31] 0xFFFFFFFF	Pin number configuration for SPI MISO signal Disconnect																												

### 6.17.5.18 PSELMOSI ( Deprecated )

Address offset: 0x510

Pin select for MOSI

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW PSELMOSI	Disconnected	[0..31] 0xFFFFFFFF	Pin number configuration for SPI MOSI signal Disconnect																												

### 6.17.5.19 PSELCSN ( Deprecated )

Address offset: 0x514

Pin select for CSN

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A A																															
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW PSELCSN	Disconnected	[0..31] 0xFFFFFFFF	Pin number configuration for SPI CSN signal Disconnect																												

### 6.17.5.20 RXDPTR ( Deprecated )

Address offset: 0x534

## RXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												

A RW RXDPTR

RXD data pointer

See the memory chapter for details about which memories are available for EasyDMA.

### 6.17.5.21 MAXRX ( Deprecated )

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												

A RW MAXRX

[0..0x7fff]

Maximum number of bytes in receive buffer

### 6.17.5.22 AMOUNTRX ( Deprecated )

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												

A R AMOUNTRX

[0..0x7fff]

Number of bytes received in the last granted transaction

### 6.17.5.23 RXD.PTR

Address offset: 0x534

RXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												

A RW PTR

RXD data pointer

See the memory chapter for details about which memories are available for EasyDMA.

### 6.17.5.24 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[0..0x7fff]	Maximum number of bytes in receive buffer																												

### 6.17.5.25 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNT	[0..0x7fff]	Number of bytes received in the last granted transaction																												

### 6.17.5.26 RXD.LIST

Address offset: 0x540

EasyDMA list type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	LIST		List type																												
		Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

### 6.17.5.27 TXDPTR ( Deprecated )

Address offset: 0x544

TXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	TXDPTR		TXD data pointer																												
				See the memory chapter for details about which memories are available for EasyDMA.																												

### 6.17.5.28 MAXTX ( Deprecated )

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXTX	[0..0x7fff]	Maximum number of bytes in transmit buffer																												

### 6.17.5.29 AMOUNTTX ( Deprecated )

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNTTX	[0..0x7fff]	Number of bytes transmitted in last granted transaction																												

### 6.17.5.30 TXD.PTR

Address offset: 0x544

TXD data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	PTR		TXD data pointer																												

See the memory chapter for details about which memories are available for EasyDMA.

### 6.17.5.31 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[0..0x7fff]	Maximum number of bytes in transmit buffer																												

### 6.17.5.32 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNT	[0..0x7fff]	Number of bytes transmitted in last granted transaction																												

### 6.17.5.33 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW LIST			List type																												
		Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

### 6.17.5.34 CONFIG

Address offset: 0x554

Configuration register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																															C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																
ID	Acce Field	Value ID	Value	Description																													
A	RW ORDER			Bit order																													
		MsbFirst	0	Most significant bit shifted out first																													
		LsbFirst	1	Least significant bit shifted out first																													
B	RW CPHA			Serial clock (SCK) phase																													
		Leading	0	Sample on leading edge of clock, shift serial data on trailing edge																													
		Trailing	1	Sample on trailing edge of clock, shift serial data on leading edge																													
C	RW CPOL			Serial clock (SCK) polarity																													
		ActiveHigh	0	Active high																													
		ActiveLow	1	Active low																													

### 6.17.5.35 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																															A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW DEF			Default character. Character clocked out in case of an ignored transaction.																																

### 6.17.5.36 ORC

Address offset: 0x5C0

Over-read character

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	ORC			Over-read character. Character clocked out after an over-read of the transmit buffer.																											

## 6.17.6 Electrical specification

### 6.17.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f <sub>SPIS</sub>	Bit rates for SPIS <sup>24</sup>			g <sup>25</sup>	Mbps
t <sub>SPIS,START</sub>	Time from RELEASE task to receive/transmit (CSN active)		0.125		µs

### 6.17.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>SPIS,CSCKIN</sub>	SCK input period	125			ns
t <sub>SPIS,RFSCCKIN</sub>	SCK input rise/fall time			30	ns
t <sub>SPIS,WHSCCKIN</sub>	SCK input high time	30			ns
t <sub>SPIS,WLSCCKIN</sub>	SCK input low time	30			ns
t <sub>SPIS,SUCSN</sub>	CSN to CLK setup time	1000			ns
t <sub>SPIS,HCSN</sub>	CLK to CSN hold time	1000			ns
t <sub>SPIS,ASA</sub>	CSN to MISO driven	0			ns
t <sub>SPIS,ASO</sub>	CSN to MISO valid <sup>26</sup>			1000	ns
t <sub>SPIS,DISSO</sub>	CSN to MISO disabled <sup>26</sup>			68	ns
t <sub>SPIS,CWH</sub>	CSN inactive time	300			ns
t <sub>SPIS,VSO</sub>	CLK edge to MISO valid			19	ns
t <sub>SPIS,HSO</sub>	MISO hold time after CLK edge	18 <sup>27</sup>			ns
t <sub>SPIS,SUSI</sub>	MOSI to CLK edge setup time	59			ns
t <sub>SPIS,HSI</sub>	CLK edge to MOSI hold time	20			ns

<sup>24</sup> High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

<sup>25</sup> The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

<sup>26</sup> At 25 pF load, including GPIO capacitance, see [GPIO electrical specification](#).

<sup>27</sup> This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output.

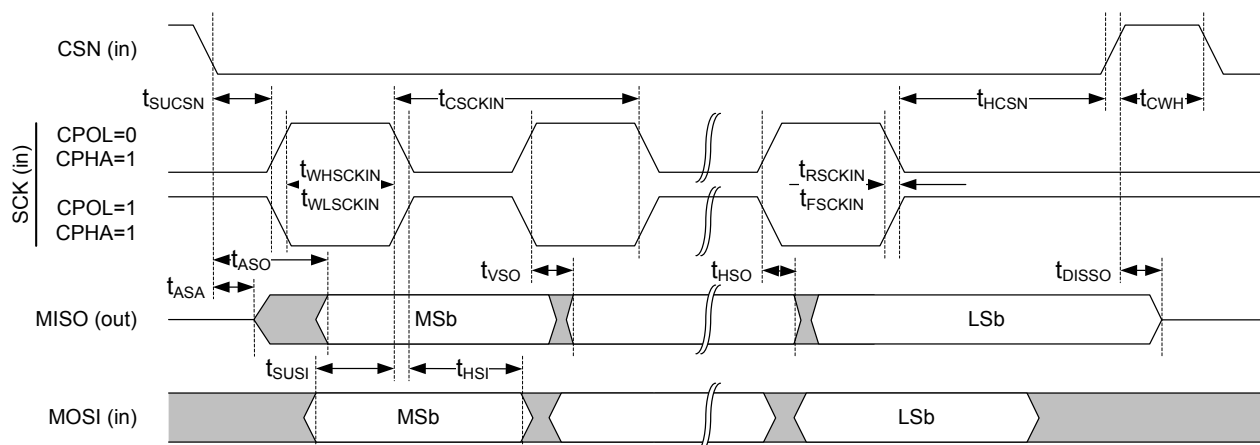
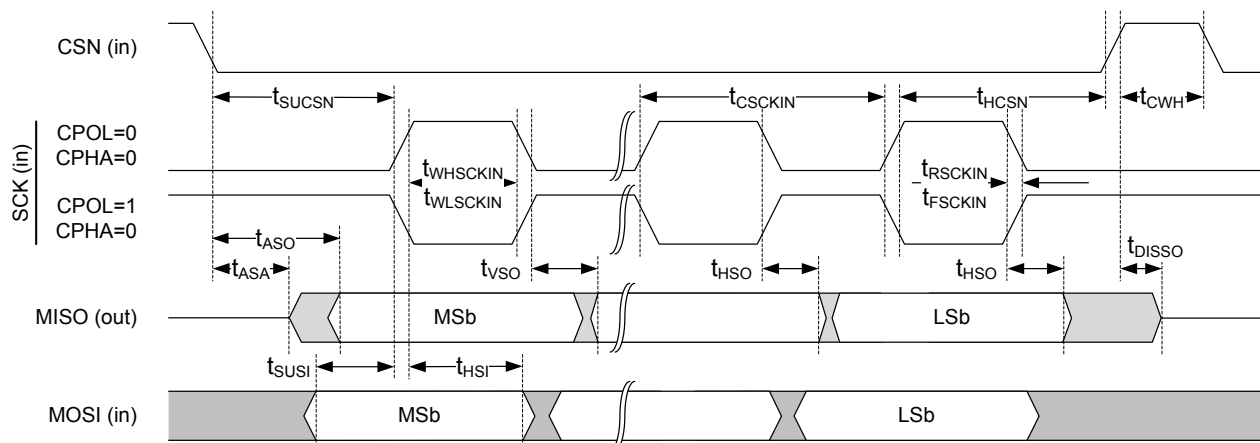


Figure 104: SPIS timing diagram

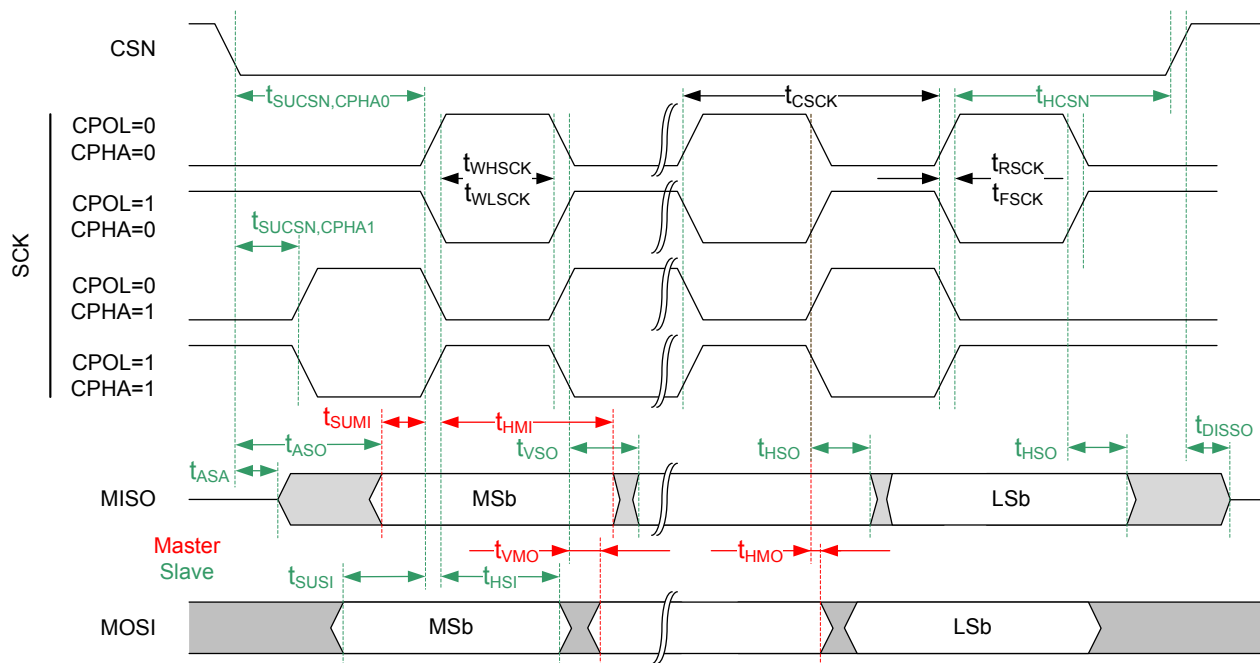


Figure 105: Common SPIM and SPIS timing diagram

## 6.18 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

### 6.18.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40014000	SWI	SWI0	Software interrupt 0	
0x40015000	SWI	SWI1	Software interrupt 1	
0x40016000	SWI	SWI2	Software interrupt 2	
0x40017000	SWI	SWI3	Software interrupt 3	
0x40018000	SWI	SWI4	Software interrupt 4	
0x40019000	SWI	SWI5	Software interrupt 5	

Table 85: Instances

## 6.19 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see [CLOCK — Clock control](#) on page 69 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

### 6.19.1 Registers

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature sensor	

Table 86: Instances

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of first piecewise linear function



Register	Offset	Description
A1	0x524	Slope of second piecewise linear function
A2	0x528	Slope of third piecewise linear function
A3	0x52C	Slope of fourth piecewise linear function
A4	0x530	Slope of fifth piecewise linear function
A5	0x534	Slope of sixth piecewise linear function
B0	0x540	y-intercept of first piecewise linear function
B1	0x544	y-intercept of second piecewise linear function
B2	0x548	y-intercept of third piecewise linear function
B3	0x54C	y-intercept of fourth piecewise linear function
B4	0x550	y-intercept of fifth piecewise linear function
B5	0x554	y-intercept of sixth piecewise linear function
T0	0x560	End point of first piecewise linear function
T1	0x564	End point of second piecewise linear function
T2	0x568	End point of third piecewise linear function
T3	0x56C	End point of fourth piecewise linear function
T4	0x570	End point of fifth piecewise linear function

Table 87: Register overview

### 6.19.1.1 TASKS\_START

Address offset: 0x000

Start temperature measurement

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_START			Start temperature measurement																												
		Trigger	1	Trigger task																												

### 6.19.1.2 TASKS\_STOP

Address offset: 0x004

Stop temperature measurement

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOP			Stop temperature measurement																												
		Trigger	1	Trigger task																												

### 6.19.1.3 EVENTS\_DATARDY

Address offset: 0x100

Temperature measurement complete, data ready

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_DATARDY		Temperature measurement complete, data ready																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.19.1.4 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	DATARDY		Write '1' to enable interrupt for event DATARDY																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.19.1.5 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	DATARDY		Write '1' to disable interrupt for event DATARDY																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.19.1.6 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	R	TEMP		Temperature in °C (0.25° steps)																											
				Result of temperature measurement. Die temperature in °C, 2's complement format, 0.25 °C steps.																											
				Decision point: DATARDY																											

### 6.19.1.7 A0

Address offset: 0x520

Slope of first piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x00000326</b>																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0
ID	Acce Field	Value ID	Value	Description																																																			
A	RW	A0		Slope of first piecewise linear function																																																			

### 6.19.1.8 A1

Address offset: 0x524

Slope of second piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x00000348</b>																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0
ID	Acce Field	Value ID	Value	Description																																																			
A	RW	A1		Slope of second piecewise linear function																																																			

### 6.19.1.9 A2

Address offset: 0x528

Slope of third piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x000003AA</b>																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1	0
ID	Acce Field	Value ID	Value	Description																																																			
A	RW	A2		Slope of third piecewise linear function																																																			

### 6.19.1.10 A3

Address offset: 0x52C

Slope of fourth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x0000040E</b>																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	A3		Slope of fourth piecewise linear function																																																				

### 6.19.1.11 A4

Address offset: 0x530

Slope of fifth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x00004BD</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	1
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	A4		Slope of fifth piecewise linear function																																																				

### 6.19.1.12 A5

Address offset: 0x534

Slope of sixth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x00005A3</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	1	1
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	A5		Slope of sixth piecewise linear function																																																				

### 6.19.1.13 B0

Address offset: 0x540

y-intercept of first piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x00003FEF</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	B0		y-intercept of first piecewise linear function																																																				

### 6.19.1.14 B1

Address offset: 0x544

y-intercept of second piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x00003FBE</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	B1		y-intercept of second piecewise linear function																																																					

### 6.19.1.15 B2

Address offset: 0x548

y-intercept of third piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x00003FBE</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	B2		y-intercept of third piecewise linear function																																																					

### 6.19.1.16 B3

Address offset: 0x54C

y-intercept of fourth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
<b>Reset 0x00000012</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	B3		y-intercept of fourth piecewise linear function																																																					

### 6.19.1.17 B4

Address offset: 0x550

y-intercept of fifth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000124</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	B4		y-intercept of fifth piecewise linear function																																																				

### 6.19.1.18 B5

Address offset: 0x554

y-intercept of sixth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x0000027C</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	0	0
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	B5		y-intercept of sixth piecewise linear function																																																				

### 6.19.1.19 T0

Address offset: 0x560

End point of first piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x000000E2</b>																								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0
ID	Acce Field	Value ID	Value	Description																																																			
A	RW	T0		End point of first piecewise linear function																																																			

### 6.19.1.20 T1

Address offset: 0x564

End point of second piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	T1		End point of second piecewise linear function																												

### 6.19.1.21 T2

Address offset: 0x568

End point of third piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000019	0 1 1 0 0 1																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	T2		End point of third piecewise linear function																												

### 6.19.1.22 T3

Address offset: 0x56C

End point of fourth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x0000003C	0 1 1 1 1 0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	T3		End point of fourth piecewise linear function																												

### 6.19.1.23 T4

Address offset: 0x570

End point of fifth piecewise linear function

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000050	0 1 0 1 0 0 0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	T4		End point of fifth piecewise linear function																												

## 6.19.2 Electrical specification

### 6.19.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>TEMP</sub>	Time required for temperature measurement		36		μs
T <sub>TEMP,RANGE</sub>	Temperature sensor range	-40		105	°C
T <sub>TEMP,ACC</sub>	Temperature sensor accuracy	-5		5	°C
T <sub>TEMP,ACC,EXT</sub>	Temperature sensor accuracy, extended temperature range	-7		7	°C
T <sub>TEMP,RES</sub>	Temperature sensor resolution		0.25		°C
T <sub>TEMP,STB</sub>	Sample to sample stability at constant device temperature		±0.25		°C
T <sub>TEMP,OFFST</sub>	Sample offset at 25°C	-2.5		2.5	°C

## 6.20 TWI — I<sup>2</sup>C compatible two-wire interface

The TWI master is compatible with I<sup>2</sup>C operating at 100 kHz and 400 kHz.

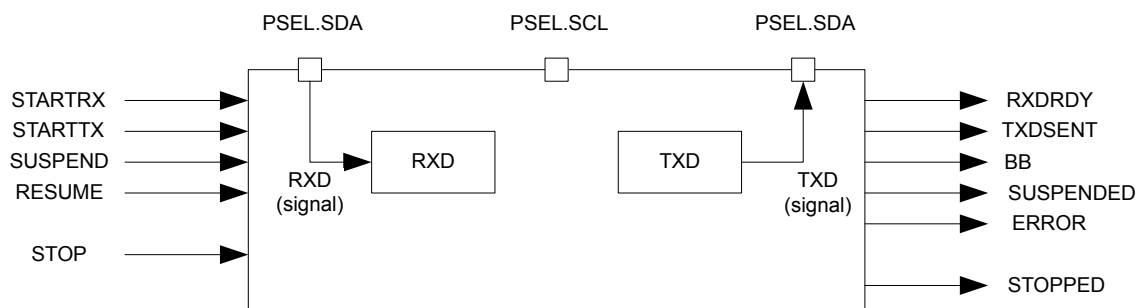


Figure 106: TWI master's main features

### 6.20.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See [TWI master's main features](#) on page 287.

A TWI setup with one master and three slaves is shown in the following figure. This TWI master is only able to operate as the only master on the TWI bus.

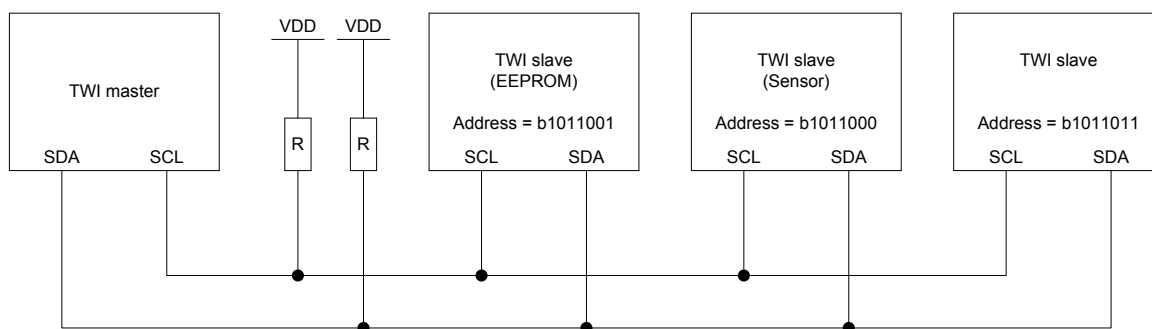


Figure 107: A typical TWI setup with one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

### 6.20.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated TWI signal is not connected to any physical pin. The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCL and PSEL.SDA must only be configured when TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in [GPIO configuration](#) on page 288.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSEL.SCL	Input	S0D1	Not applicable
SDA	As specified in PSEL.SDA	Input	S0D1	Not applicable

Table 88: GPIO configuration

### 6.20.3 Shared resources

TWI shares registers and other resources with other peripherals that have the same ID as TWI.

Therefore, you must disable all peripherals that have the same ID as TWI before TWI can be configured and used. Disabling a peripheral that has the same ID as TWI will not reset any of the registers that are shared with TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in [Instantiation](#) on page 18 shows which peripherals have the same ID as TWI.

### 6.20.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered. A second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in [The TWI master writing data to a slave](#) on page 289. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.



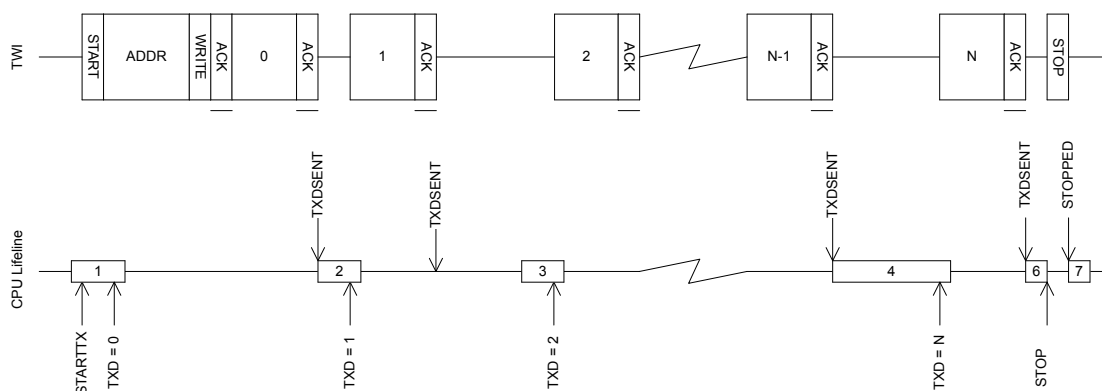


Figure 108: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered, causing the TWI master to generate a stop condition on the TWI bus.

### 6.20.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit, the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in [The TWI master reading data from a slave](#) on page 290. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.

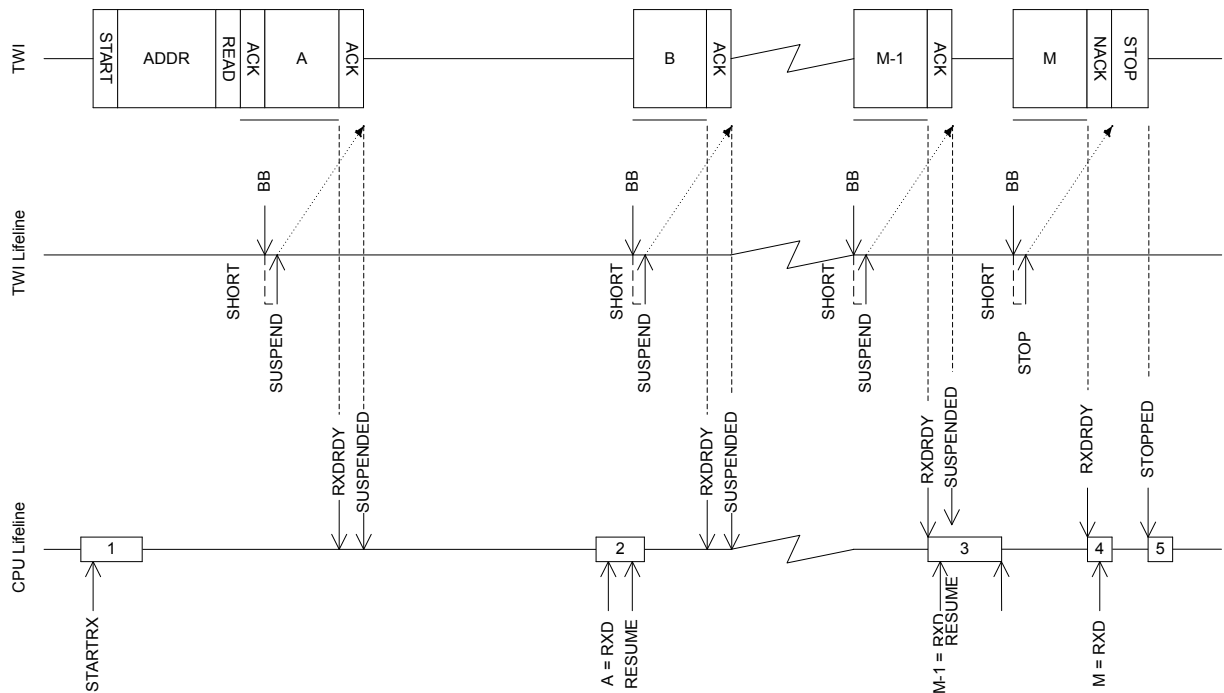


Figure 109: The TWI master reading data from a slave

### 6.20.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The following figure shows a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

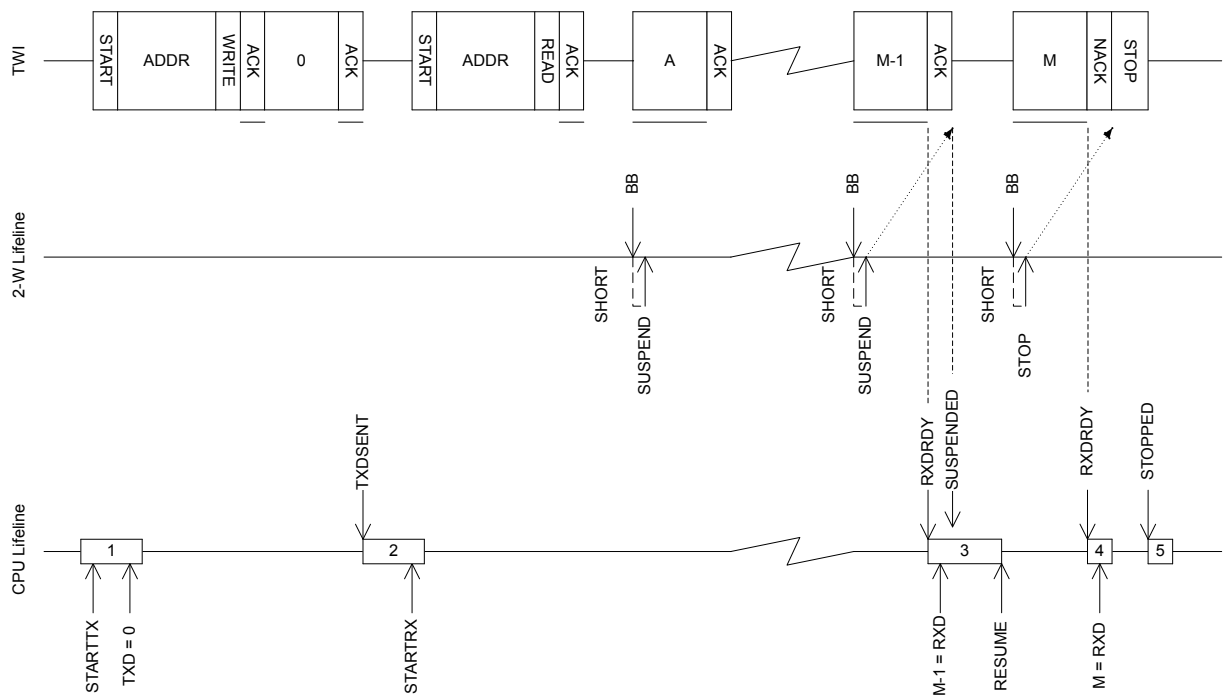


Figure 110: Repeated start sequence illustration

To generate a repeated start after a read sequence, a second start task, `STARTRX` or `STARTTX`, must be triggered instead of the `STOP` task. This start task must be triggered before the last byte is extracted from `RXD` to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

## 6.20.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The `STOP` task is not always needed, like when the peripheral is already stopped. If the `STOP` task is sent, the software shall wait until the `STOPPED` event was received as a response before disabling the peripheral through the `ENABLE` register.

## 6.20.8 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated

Table 89: Instances

Register	Offset	Description
<code>TASKS_STARTRX</code>	0x000	Start TWI receive sequence
<code>TASKS_STARTTX</code>	0x008	Start TWI transmit sequence
<code>TASKS_STOP</code>	0x014	Stop TWI transaction
<code>TASKS_SUSPEND</code>	0x01C	Suspend TWI transaction
<code>TASKS_RESUME</code>	0x020	Resume TWI transaction
<code>EVENTS_STOPPED</code>	0x104	TWI stopped
<code>EVENTS_RXDREADY</code>	0x108	TWI RXD byte received
<code>EVENTS_TXDSENT</code>	0x11C	TWI TXD byte sent
<code>EVENTS_ERROR</code>	0x124	TWI error
<code>EVENTS_BB</code>	0x138	TWI byte boundary, generated before each byte that is sent or received
<code>EVENTS_SUSPENDED</code>	0x148	TWI entered the suspended state
<code>SHORTS</code>	0x200	Shortcuts between local events and tasks
<code>INTENSET</code>	0x304	Enable interrupt
<code>INTENCLR</code>	0x308	Disable interrupt
<code>ERRORSRC</code>	0x4C4	Error source
<code>ENABLE</code>	0x500	Enable TWI
<code>PSEL_SCL</code>	0x508	Pin select for SCL
<code>PSEL_SDA</code>	0x50C	Pin select for SDA
<code>RXD</code>	0x518	RXD register
<code>TXD</code>	0x51C	TXD register
<code>FREQUENCY</code>	0x524	TWI frequency. Accuracy depends on the HFCLK source selected.
<code>ADDRESS</code>	0x588	Address used in the TWI transfer

Table 90: Register overview

### 6.20.8.1 `TASKS_STARTRX`

Address offset: 0x000

Start TWI receive sequence

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STARTRX			Start TWI receive sequence																												
		Trigger	1	Trigger task																												

### 6.20.8.2 TASKS\_STARTTX

Address offset: 0x008

Start TWI transmit sequence

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STARTTX			Start TWI transmit sequence																												
		Trigger	1	Trigger task																												

### 6.20.8.3 TASKS\_STOP

Address offset: 0x014

Stop TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOP			Stop TWI transaction																												
		Trigger	1	Trigger task																												

### 6.20.8.4 TASKS\_SUSPEND

Address offset: 0x01C

Suspend TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_SUSPEND			Suspend TWI transaction																												
		Trigger	1	Trigger task																												

### 6.20.8.5 TASKS\_RESUME

Address offset: 0x020

Resume TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_RESUME	Trigger	1	Resume TWI transaction Trigger task																												

### 6.20.8.6 EVENTS\_STOPPED

Address offset: 0x104

TWI stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_STOPPED	NotGenerated	0	TWI stopped Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.7 EVENTS\_RXDREADY

Address offset: 0x108

TWI RXD byte received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_RXDREADY	NotGenerated	0	TWI RXD byte received Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.8 EVENTS\_TXDSENT

Address offset: 0x11C

TWI TXD byte sent

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_TXDSENT	NotGenerated	0	TWI TXD byte sent Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.9 EVENTS\_ERROR

Address offset: 0x124

TWI error

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_ERROR			TWI error																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.10 EVENTS\_BB

Address offset: 0x138

TWI byte boundary, generated before each byte that is sent or received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_BB			TWI byte boundary, generated before each byte that is sent or received																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.11 EVENTS\_SUSPENDED

Address offset: 0x148

TWI entered the suspended state

Generated just after ACK bit has been transferred in a read transaction, and only if SUSPEND has been requested earlier.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_SUSPENDED			TWI entered the suspended state																												
				Generated just after ACK bit has been transferred in a read transaction, and only if SUSPEND has been requested earlier.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.20.8.12 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															B	A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value	ID	Value	Description																										
A	RW	BB_SUSPEND				Shortcut between event <b>BB</b> and task <b>SUSPEND</b>																										
			Disabled	0		Disable shortcut																										
			Enabled	1		Enable shortcut																										
B	RW	BB_STOP				Shortcut between event <b>BB</b> and task <b>STOP</b>																										
			Disabled	0		Disable shortcut																										
			Enabled	1		Enable shortcut																										

### 6.20.8.13 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																F	E	D	C											B	A	
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value	ID	Value	Description																										
A	RW	STOPPED				Write '1' to enable interrupt for event <b>STOPPED</b>																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										
B	RW	RXDREADY				Write '1' to enable interrupt for event <b>RXDREADY</b>																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										
C	RW	TXDSENT				Write '1' to enable interrupt for event <b>TXDSENT</b>																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										
D	RW	ERROR				Write '1' to enable interrupt for event <b>ERROR</b>																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										
E	RW	BB				Write '1' to enable interrupt for event <b>BB</b>																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										
F	RW	SUSPENDED				Write '1' to enable interrupt for event <b>SUSPENDED</b>																										
						Generated just after ACK bit has been transferred in a read transaction, and only if SUSPEND has been requested earlier.																										
			Set	1		Enable																										
			Disabled	0		Read: Disabled																										
			Enabled	1		Read: Enabled																										

### 6.20.8.14 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID		F							E							D							C							B		A
Reset 0x00000000		0 0																														
ID	Acce Field	Value ID	Value	Description																												
A	RW STOPPED			Write '1' to disable interrupt for event <b>STOPPED</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
B	RW RXDREADY			Write '1' to disable interrupt for event <b>RXDREADY</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
C	RW TXDSENT			Write '1' to disable interrupt for event <b>TXDSENT</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
D	RW ERROR			Write '1' to disable interrupt for event <b>ERROR</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
E	RW BB			Write '1' to disable interrupt for event <b>BB</b>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
F	RW SUSPENDED			Write '1' to disable interrupt for event <b>SUSPENDED</b>																												
				Generated just after ACK bit has been transferred in a read transaction, and only if SUSPEND has been requested earlier.																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.20.8.15 ERRORSRC

Address offset: 0x4C4

Error source

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																													
ID																							C							B	A
Reset 0x00000000		0 0																													
ID	Acce Field	Value ID	Value	Description																											
A	RW OVERRUN			Overrun error																											
				A new byte was received before previous byte got read by software from the RXD register. (Previous data is lost)																											
		NotPresent	0	Read: no overrun occurred																											
		Present	1	Read: overrun occurred																											
B	RW ANACK			NACK received after sending the address (write '1' to clear)																											
		NotPresent	0	Read: error not present																											
		Present	1	Read: error present																											
C	RW DNACK			NACK received after sending a data byte (write '1' to clear)																											
		NotPresent	0	Read: error not present																											
		Present	1	Read: error present																											



### 6.20.8.16 ENABLE

Address offset: 0x500

Enable TWI

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW ENABLE			Enable or disable TWI																														
		Disabled	0	Disable TWI																														
		Enabled	5	Enable TWI																														

### 6.20.8.17 PSEL.SCL

Address offset: 0x508

Pin select for SCL

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID	C																														A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

### 6.20.8.18 PSEL.SDA

Address offset: 0x50C

Pin select for SDA

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID	C																														A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

### 6.20.8.19 RXD

Address offset: 0x518

RXD register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																															A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																			
ID	Acce Field	Value ID	Value	Description																																
A	R	RXD		RXD register																																

## 6.20.8.20 TXD

Address offset: 0x51C

TXD register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	TXD		TXD register																												

## 6.20.8.21 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A																															
Reset 0x04000000	0 0 0 0 0 1 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	FREQUENCY		TWI master clock frequency																												
		K100	0x01980000	100 kbps																												
		K250	0x04000000	250 kbps																												
		K400	0x06680000	400 kbps (actual rate 410.256 kbps)																												

## 6.20.8.22 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	ADDRESS		Address used in the TWI transfer																												

## 6.20.9 Electrical specification

### 6.20.9.1 TWI interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{TWI,SCL}$	Bit rates for TWI <sup>28</sup>	100		400	kbps
$t_{TWI,START}$	Time from STARTRX/STARTTX task to transmission started		1.5		$\mu$ s

<sup>28</sup> High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

## 6.20.9.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{TWI,SU\_DAT}$	Data setup time before positive edge on SCL – all modes	300			ns
$t_{TWI,HD\_DAT}$	Data hold time after negative edge on SCL – all modes	500			ns
$t_{TWI,HD\_STA,100kbps}$	TWI master hold time for START and repeated START condition, 100 kbps	10000			ns
$t_{TWI,HD\_STA,250kbps}$	TWI master hold time for START and repeated START condition, 250kbps	4000			ns
$t_{TWI,HD\_STA,400kbps}$	TWI master hold time for START and repeated START condition, 400 kbps	2500			ns
$t_{TWI,SU\_STO,100kbps}$	TWI master setup time from SCL high to STOP condition, 100 kbps	5000			ns
$t_{TWI,SU\_STO,250kbps}$	TWI master setup time from SCL high to STOP condition, 250 kbps	2000			ns
$t_{TWI,SU\_STO,400kbps}$	TWI master setup time from SCL high to STOP condition, 400 kbps	1250			ns
$t_{TWI,BUF,100kbps}$	TWI master bus free time between STOP and START conditions, 100 kbps	5800			ns
$t_{TWI,BUF,250kbps}$	TWI master bus free time between STOP and START conditions, 250 kbps	2700			ns
$t_{TWI,BUF,400kbps}$	TWI master bus free time between STOP and START conditions, 400 kbps	2100			ns

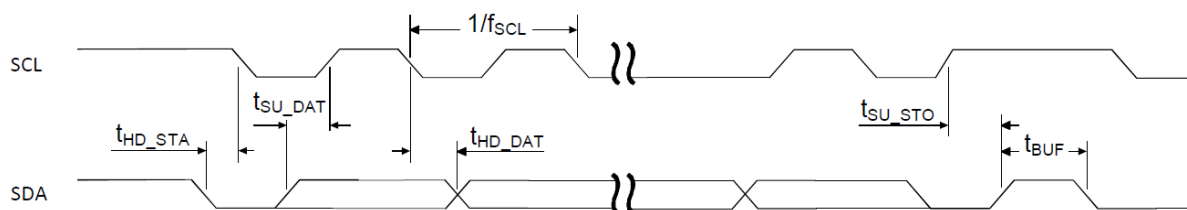


Figure 111: TWI timing diagram, 1 byte transaction

## 6.21 TIMER — Timer/counter

This peripheral is a general purpose timer designed to keep track of time in user-selective time intervals, it can operate in two modes: timer and counter.

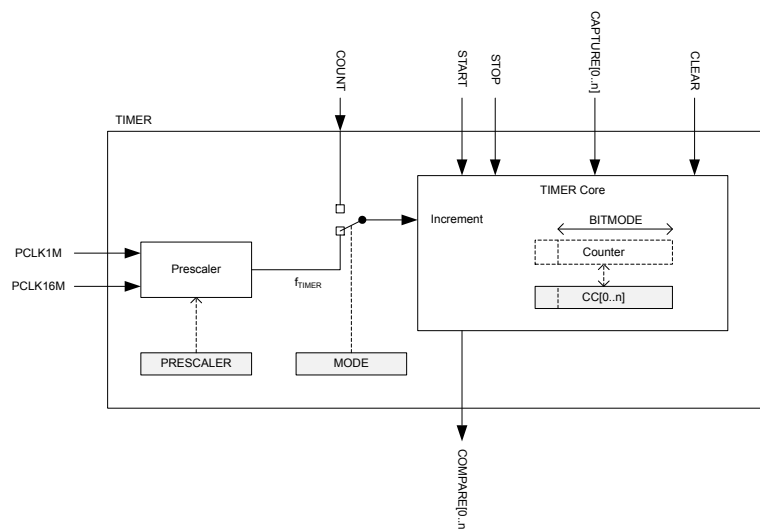


Figure 112: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

TIMER can operate in two modes: Timer mode and Counter mode. In both modes, TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency  $f_{\text{TIMER}}$  as illustrated in [Block schematic for timer/counter](#) on page 300. The timer frequency is derived from PCLK16M as shown in the following example, using the values specified in the PRESCALER register.

$$f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})$$

When  $f_{\text{TIMER}} \leq 1 \text{ MHz}$ , TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, meaning the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in register [BITMODE](#) on page 305.

[PRESCALER](#) on page 305 and [BITMODE](#) on page 305 must only be updated when the timer is stopped. If these registers are updated while the timer is started, unpredictable behavior may occur.

When the timer is incremented beyond its maximum value, the Counter register will overflow and the timer will automatically start over from zero.

The Counter register can be cleared by triggering the CLEAR task. This will explicitly set the internal value to zero.

TIMER implements multiple capture/compare registers.

Independent of prescaler setting, the accuracy of TIMER is equivalent to one tick of the timer frequency  $f_{\text{TIMER}}$  as illustrated in [Block schematic for timer/counter](#) on page 300.

### 6.21.1 Capture

TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

### 6.21.2 Compare

TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

**BITMODE** on page 305 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

### 6.21.3 Task delays

After TIMER is started, the CLEAR, COUNT, and STOP tasks are guaranteed to take effect within one clock cycle of the PCLK16M.

### 6.21.4 Task priority

If the START task and the STOP task are triggered at the same time, meaning within the same period of PCLK16M, the STOP task will be prioritized.

### 6.21.5 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers (CC[0..3])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers (CC[0..3])
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers (CC[0..3])
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers (CC[0..5])

Table 91: Instances

Register	Offset	Description	
TASKS_START	0x000	Start Timer	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register	

Register	Offset	Description
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MODE	0x504	Timer mode selection
BITMODE	0x508	Configure the number of bits used by the TIMER
PRESCALER	0x510	Timer prescaler register
CC[0]	0x540	Capture/Compare register 0
CC[1]	0x544	Capture/Compare register 1
CC[2]	0x548	Capture/Compare register 2
CC[3]	0x54C	Capture/Compare register 3
CC[4]	0x550	Capture/Compare register 4
CC[5]	0x554	Capture/Compare register 5

Table 92: Register overview

### 6.21.5.1 TASKS\_START

Address offset: 0x000

Start Timer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	W	TASKS_START	Trigger	1	Start Timer Trigger task																										

### 6.21.5.2 TASKS\_STOP

Address offset: 0x004

Stop Timer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	W	TASKS_STOP	Trigger	1	Stop Timer Trigger task																										

### 6.21.5.3 TASKS\_COUNT

Address offset: 0x008

Increment Timer (Counter mode only)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_COUNT			Increment Timer (Counter mode only)																												
		Trigger	1	Trigger task																												

### 6.21.5.4 TASKS\_CLEAR

Address offset: 0x00C

Clear time

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CLEAR			Clear time																												
		Trigger	1	Trigger task																												

### 6.21.5.5 TASKS\_SHUTDOWN ( Deprecated )

Address offset: 0x010

Shut down timer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_SHUTDOWN			Shut down timer																												
		Trigger	1	Trigger task																												
				Deprecated																												

### 6.21.5.6 TASKS\_CAPTURE[n] (n=0..5)

Address offset: 0x040 + (n × 0x4)

Capture Timer value to CC[n] register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_CAPTURE			Capture Timer value to CC[n] register																												
		Trigger	1	Trigger task																												

### 6.21.5.7 EVENTS\_COMPARE[n] (n=0..5)

Address offset: 0x140 + (n × 0x4)

## Compare event on CC[n] match

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																															A
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_COMPARE			Compare event on CC[n] match																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

## 6.21.5.8 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																							
ID																									L	K	J	I	H	G					F	E	D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																							
ID	Acce Field	Value ID	Value	Description																																				
A-F	RW COMPARE[i]_CLEAR (i=0..5)			Shortcut between event COMPARE[i] and task CLEAR																																				
		Disabled	0	Disable shortcut																																				
		Enabled	1	Enable shortcut																																				
G-L	RW COMPARE[i]_STOP (i=0..5)			Shortcut between event COMPARE[i] and task STOP																																				
		Disabled	0	Disable shortcut																																				
		Enabled	1	Enable shortcut																																				

## 6.21.5.9 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																									F	E	D	C	B	A	
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A-F	RW COMPARE[i] (i=0..5)			Write '1' to enable interrupt for event COMPARE[i]																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

## 6.21.5.10 INTENCLR

Address offset: 0x308

Disable interrupt



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	F E D C B A																														
Reset	0x00000000																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A-F	RW	COMPARE[i] (i=0..5)		Write '1' to disable interrupt for event COMPARE[i]																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.21.5.11 MODE

Address offset: 0x504

Timer mode selection

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset	0x00000000																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	MODE		Timer mode																											
		Timer	0	Select Timer mode																											
		Counter	1	Select Counter mode																											
		LowPowerCounter	2	Select Low Power Counter mode																											

Deprecated

### 6.21.5.12 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset	0x00000000																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	BITMODE		Timer bit width																											
		16Bit	0	16 bit timer bit width																											
		08Bit	1	8 bit timer bit width																											
		24Bit	2	24 bit timer bit width																											
		32Bit	3	32 bit timer bit width																											

### 6.21.5.13 PRESCALER

Address offset: 0x510

Timer prescaler register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A A A																														
Reset	0x00000004																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	PRESCALER	[0..9]	Prescaler value																											

### 6.21.5.14 CC[n] (n=0..5)

Address offset: 0x540 + (n × 0x4)

## Capture/Compare register n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

ID	Acce Field	Value ID	Value	Description
A	RW	CC		Capture/Compare value  Only the number of bits indicated by BITMODE will be used by the TIMER.

## 6.21.6 Electrical specification

# 6.22 TWIM — I<sup>2</sup>C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus.

Listed here are the main features for TWIM:

- I<sup>2</sup>C compatible
- Supported baud rates: 100, 250, 400 kbps
- Support for clock stretching (non I<sup>2</sup>C compliant)
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

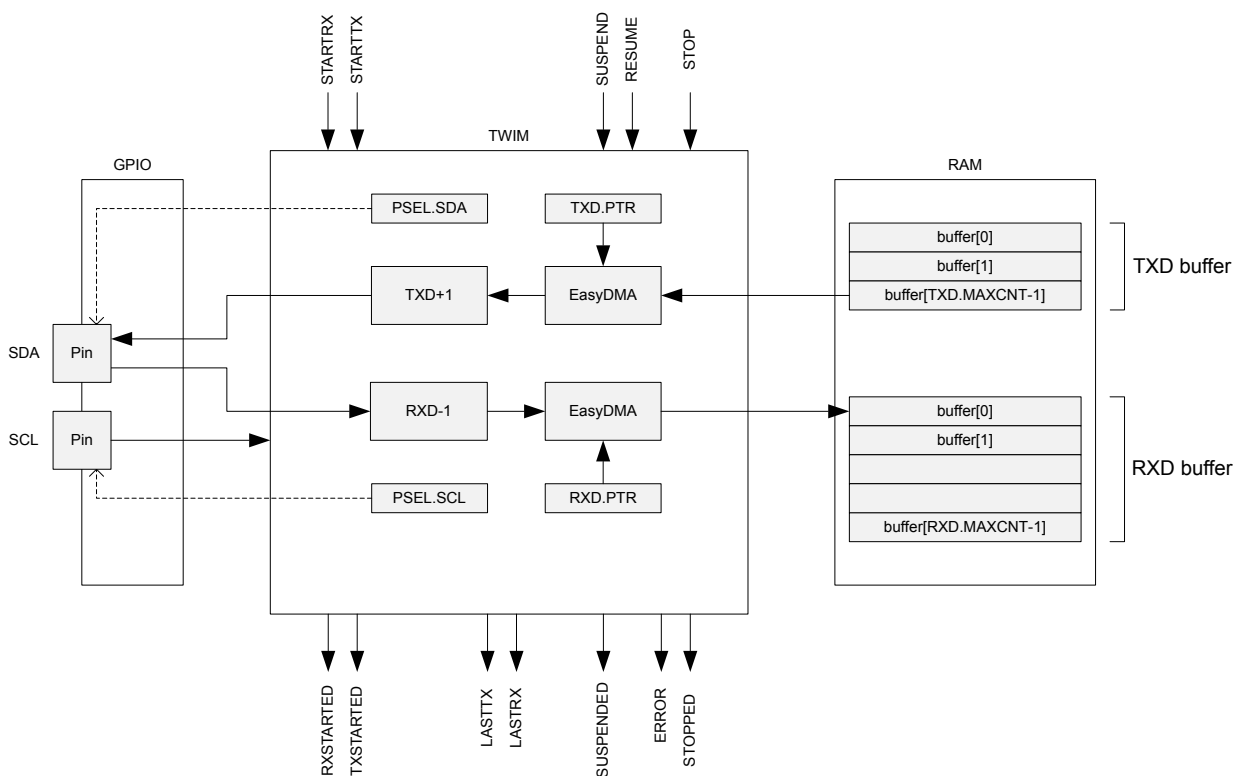


Figure 113: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see the following figure. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.

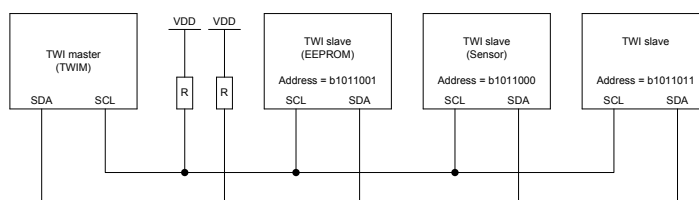


Figure 114: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The SCK pulse following a stretched clock cycle may be shorter than specified by the I2C specification.

The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

After the TWI master is started, the STARTTX or STARTRX tasks should not be triggered again until the TWI master has issued a LASTRX, LASTTX, or STOPPED event.

The TWI master can be suspended using the SUSPEND task, this can be used when using the TWI master in a low priority interrupt context. When the TWIM enters suspend state, will automatically issue a SUSPENDED event while performing a continuous clock stretching until it is instructed to resume operation via a RESUME task. The TWI master cannot be stopped while it is suspended, thus the STOP task has to be issued after the TWI master has been resumed.

**Note:** Any ongoing byte transfer will be allowed to complete before the suspend is enforced. A SUSPEND task has no effect unless the TWI master is actively involved in a transfer.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

## 6.22.1 EasyDMA

The TWIM implements EasyDMA for accessing RAM without CPU involvement.

The TWIM peripheral implements the EasyDMA channels found in the following table.

Channel	Type	Register Cluster
TXD	READER	TXD
RXD	WRITER	RXD

Table 93: TWIM EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 37.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

## 6.22.2 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is shown in the following figure. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect. This event can be used to synchronize the software.

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is shown in the following figure.

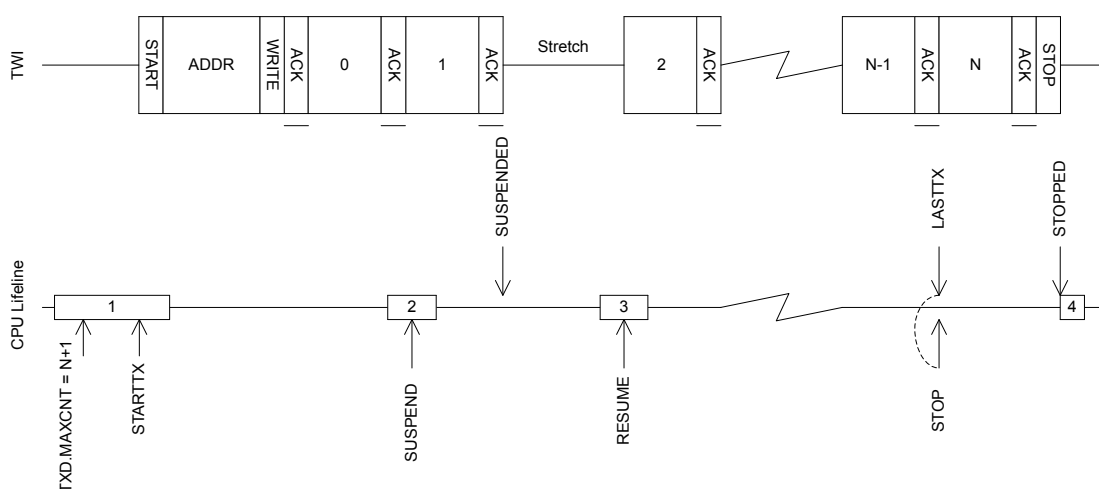


Figure 115: TWI master writing data to a slave

The TWI master is stopped by triggering the STOP task. This task should be triggered during the transmission of the last byte to secure that the TWI master will stop as fast as possible after sending the last byte. The shortcut between LASTTX and STOP can alternatively be used to accomplish this.

**Note:** The TWI master does not stop by itself when the entire RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

### 6.22.3 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After sending the ACK bit, the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte have been received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in [The TWI master reading data from a slave](#) on page 310. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect. This event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, as shown in [The TWI master reading data from a slave](#) on page 310. If RXD.MAXCNT > 1, the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1, the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task. This task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is recommended to use the shortcut between LASTRX and STOP to accomplish this.

The TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot be stopped while suspended, so the STOP task must be issued after the TWI master has been resumed.

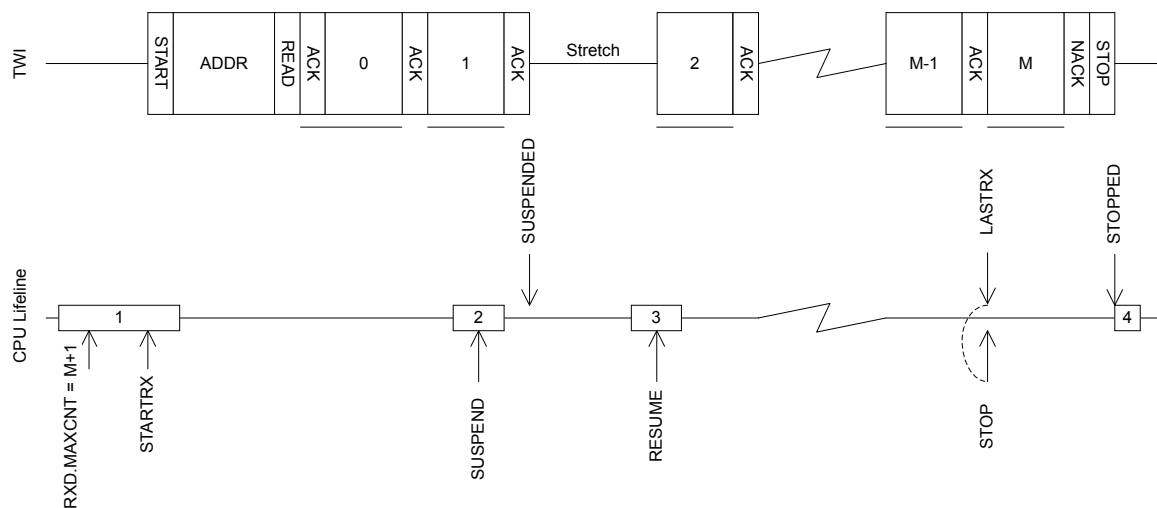


Figure 116: The TWI master reading data from a slave

### 6.22.4 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The following figure shows an example of a repeated start sequence where the TWI master writes two bytes followed by reading four bytes from the slave.

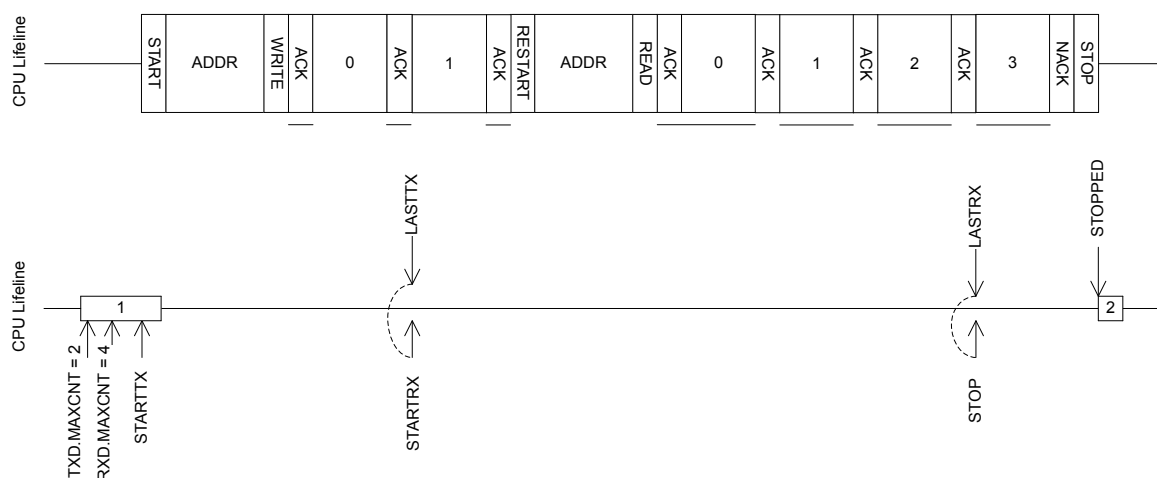


Figure 117: Master repeated start sequence

If a more complex repeated start sequence is needed, and the TWI firmware driver is serviced in a low priority interrupt, it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts is shown in the following figure.

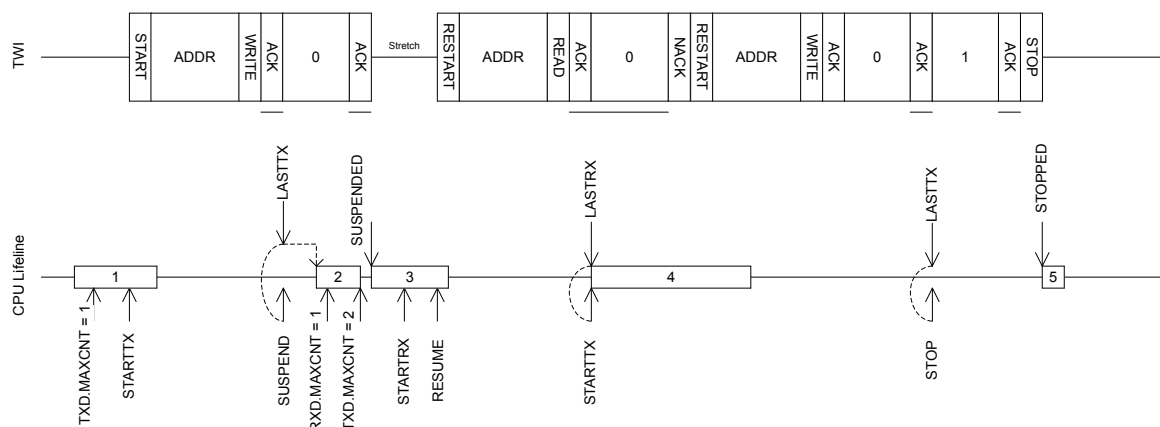


Figure 118: Double repeated start sequence

### 6.22.5 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

When the STOP task is sent, the software shall wait until the STOPPED event is received as a response before disabling the peripheral through the ENABLE register. If the peripheral is already stopped, the STOP task is not required.

### 6.22.6 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in the following table.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	S0D1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1

Table 94: GPIO configuration before enabling peripheral

### 6.22.7 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIM	TWIM0	Two-wire interface master 0	
0x40004000	TWIM	TWIM1	Two-wire interface master 1	

Table 95: Instances

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_SUSPENDED	0x148	SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcuts between local events and tasks
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS	0x588	Address used in the TWI transfer

Table 96: Register overview

### 6.22.7.1 TASKS\_STARTRX

Address offset: 0x000

Start TWI receive sequence

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value	ID	Value	Description																										
A	W	TASKS_STARTRX				Start TWI receive sequence																										
			Trigger	1		Trigger task																										

### 6.22.7.2 TASKS\_STARTTX

Address offset: 0x008

Start TWI transmit sequence



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STARTTX	Trigger	1	Start TWI transmit sequence Trigger task																												

### 6.22.7.3 TASKS\_STOP

Address offset: 0x014

Stop TWI transaction. Must be issued while the TWI master is not suspended.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOP	Trigger	1	Stop TWI transaction. Must be issued while the TWI master is not suspended. Trigger task																												

### 6.22.7.4 TASKS\_SUSPEND

Address offset: 0x01C

Suspend TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_SUSPEND	Trigger	1	Suspend TWI transaction Trigger task																												

### 6.22.7.5 TASKS\_RESUME

Address offset: 0x020

Resume TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_RESUME	Trigger	1	Resume TWI transaction Trigger task																												

### 6.22.7.6 EVENTS\_STOPPED

Address offset: 0x104

TWI stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_STOPPED			TWI stopped																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.22.7.7 EVENTS\_ERROR

Address offset: 0x124

TWI error

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_ERROR			TWI error																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.22.7.8 EVENTS\_SUSPENDED

Address offset: 0x148

SUSPEND task has been issued, TWI traffic is now suspended.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_SUSPENDED			SUSPEND task has been issued, TWI traffic is now suspended.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.22.7.9 EVENTS\_RXSTARTED

Address offset: 0x14C

Receive sequence started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_RXSTARTED			Receive sequence started																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.22.7.10 EVENTS\_TXSTARTED

Address offset: 0x150

Transmit sequence started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_TXSTARTED		Transmit sequence started																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.22.7.11 EVENTS\_LASTRX

Address offset: 0x15C

Byte boundary, starting to receive the last byte

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_LASTRX		Byte boundary, starting to receive the last byte																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.22.7.12 EVENTS\_LASTTX

Address offset: 0x160

Byte boundary, starting to transmit the last byte

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_LASTTX		Byte boundary, starting to transmit the last byte																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.22.7.13 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
ID																						F	E	D	C	B	A										
Reset	0x00000000																																				
	0 0																																				
ID	Acce Field	Value ID	Value	Description																																	
A	RW	LASTTX_STARTRX		Shortcut between event <a href="#">LASTTX</a> and task <a href="#">STARTRX</a>																																	
			Disabled	0	Disable shortcut																																
			Enabled	1	Enable shortcut																																
B	RW	LASTTX_SUSPEND		Shortcut between event <a href="#">LASTTX</a> and task <a href="#">SUSPEND</a>																																	
			Disabled	0	Disable shortcut																																
			Enabled	1	Enable shortcut																																
C	RW	LASTTX_STOP		Shortcut between event <a href="#">LASTTX</a> and task <a href="#">STOP</a>																																	
			Disabled	0	Disable shortcut																																
			Enabled	1	Enable shortcut																																

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																															F	E	D	C	B	A
<b>Reset 0x00000000</b>										0 0																										
ID	Acce	Field	Value	ID	Value	Description																														
D	RW	LASTRX_STARTTX				Shortcut between event <a href="#">LASTRX</a> and task <a href="#">STARTTX</a>																														
			Disabled	0		Disable shortcut																														
			Enabled	1		Enable shortcut																														
E	RW	LASTRX_SUSPEND				Shortcut between event <a href="#">LASTRX</a> and task <a href="#">SUSPEND</a>																														
			Disabled	0		Disable shortcut																														
			Enabled	1		Enable shortcut																														
F	RW	LASTRX_STOP				Shortcut between event <a href="#">LASTRX</a> and task <a href="#">STOP</a>																														
			Disabled	0		Disable shortcut																														
			Enabled	1		Enable shortcut																														

### 6.22.7.14 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																						
ID																													J	I	H G F			D			A		
<b>Reset 0x00000000</b>										0 0																													
ID	Acce	Field	Value	ID	Value	Description																																	
A	RW	STOPPED				Enable or disable interrupt for event <a href="#">STOPPED</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
D	RW	ERROR				Enable or disable interrupt for event <a href="#">ERROR</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
F	RW	SUSPENDED				Enable or disable interrupt for event <a href="#">SUSPENDED</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
G	RW	RXSTARTED				Enable or disable interrupt for event <a href="#">RXSTARTED</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
H	RW	TXSTARTED				Enable or disable interrupt for event <a href="#">TXSTARTED</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
I	RW	LASTRX				Enable or disable interrupt for event <a href="#">LASTRX</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	
J	RW	LASTTX				Enable or disable interrupt for event <a href="#">LASTTX</a>																																	
			Disabled	0		Disable																																	
			Enabled	1		Enable																																	

### 6.22.7.15 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		J I H G F										D										A							
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
A	RW STOPPED			Write '1' to enable interrupt for event <a href="#">STOPPED</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
D	RW ERROR			Write '1' to enable interrupt for event <a href="#">ERROR</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
F	RW SUSPENDED			Write '1' to enable interrupt for event <a href="#">SUSPENDED</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
G	RW RXSTARTED			Write '1' to enable interrupt for event <a href="#">RXSTARTED</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
H	RW TXSTARTED			Write '1' to enable interrupt for event <a href="#">TXSTARTED</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
I	RW LASTRX			Write '1' to enable interrupt for event <a href="#">LASTRX</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
J	RW LASTTX			Write '1' to enable interrupt for event <a href="#">LASTTX</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									

### 6.22.7.16 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		J I H G F										D										A							
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
A	RW STOPPED			Write '1' to disable interrupt for event <a href="#">STOPPED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
D	RW ERROR			Write '1' to disable interrupt for event <a href="#">ERROR</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
F	RW SUSPENDED			Write '1' to disable interrupt for event <a href="#">SUSPENDED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID		J I H G F																D																A
Reset 0x00000000		0 0																																
ID	Acce Field	Value ID	Value	Description																														
		Enabled	1	Read: Enabled																														
G	RW RXSTARTED			Write '1' to disable interrupt for event <a href="#">RXSTARTED</a>																														
		Clear	1	Disable																														
		Disabled	0	Read: Disabled																														
		Enabled	1	Read: Enabled																														
H	RW TXSTARTED			Write '1' to disable interrupt for event <a href="#">TXSTARTED</a>																														
		Clear	1	Disable																														
		Disabled	0	Read: Disabled																														
		Enabled	1	Read: Enabled																														
I	RW LASTRX			Write '1' to disable interrupt for event <a href="#">LASTRX</a>																														
		Clear	1	Disable																														
		Disabled	0	Read: Disabled																														
		Enabled	1	Read: Enabled																														
J	RW LASTTX			Write '1' to disable interrupt for event <a href="#">LASTTX</a>																														
		Clear	1	Disable																														
		Disabled	0	Read: Disabled																														
		Enabled	1	Read: Enabled																														

### 6.22.7.17 ERRORSRC

Address offset: 0x4C4

Error source

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																																		C B A
Reset 0x00000000		0 0																																
ID	Acce Field	Value ID	Value	Description																														
A	RW OVERRUN			Overrun error																														
				A new byte was received before previous byte got transferred into RXD buffer. (Previous data is lost)																														
		NotReceived	0	Error did not occur																														
		Received	1	Error occurred																														
B	RW ANACK			NACK received after sending the address (write '1' to clear)																														
		NotReceived	0	Error did not occur																														
		Received	1	Error occurred																														
C	RW DNACK			NACK received after sending a data byte (write '1' to clear)																														
		NotReceived	0	Error did not occur																														
		Received	1	Error occurred																														

### 6.22.7.18 ENABLE

Address offset: 0x500

Enable TWIM

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW ENABLE			Enable or disable TWIM																														
		Disabled	0	Disable TWIM																														
		Enabled	6	Enable TWIM																														

### 6.22.7.19 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID	C																														A	A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																		
ID	Acce Field	Value ID	Value	Description																															
A	RW PIN		[0..31]	Pin number																															
C	RW CONNECT			Connection																															
		Disconnected	1	Disconnect																															
		Connected	0	Connect																															

### 6.22.7.20 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID	C																														A	A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																		
ID	Acce Field	Value ID	Value	Description																															
A	RW PIN		[0..31]	Pin number																															
C	RW CONNECT			Connection																															
		Disconnected	1	Disconnect																															
		Connected	0	Connect																															

### 6.22.7.21 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x04000000</b>	<b>0 0 0 0 0 1 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW FREQUENCY			TWI master clock frequency																												
		K100	0x01980000	100 kbps																												
		K250	0x04000000	250 kbps																												
		K400	0x06400000	400 kbps																												

### 6.22.7.22 RXD.PTR

Address offset: 0x534

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																											
A	RW	PTR			Data pointer																											

See the memory chapter for details about which memories are available for EasyDMA.

### 6.22.7.23 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	RW	MAXCNT		[0..0x7FFF]	Maximum number of bytes in receive buffer																											

### 6.22.7.24 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	R	AMOUNT		[0..0x7FFF]	Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte.																											

### 6.22.7.25 RXD.LIST

Address offset: 0x540

EasyDMA list type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																															A	A	A
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																												
A	RW	LIST			List type																												
			Disabled	0	Disable EasyDMA list																												
			ArrayList	1	Use array list																												



### 6.22.7.26 TXD.PTR

Address offset: 0x544

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acces	Field	Value ID	Value	Description																											

A RW PTR

Data pointer

See the memory chapter for details about which memories are available for EasyDMA.

### 6.22.7.27 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																			
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																			
ID	Acces	Field	Value ID	Value	Description																																														

A RW MAXCNT

[0..0x7FFF]

Maximum number of bytes in transmit buffer

### 6.22.7.28 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																			
ID																							A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																			
ID	Acces	Field	Value ID	Value	Description																																														

A R AMOUNT

[0..0x7FFF]

Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte.

### 6.22.7.29 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											A	A	A			
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acces	Field	Value ID	Value	Description																											

A RW LIST

List type

Disabled

0

Disable EasyDMA list

ArrayList

1

Use array list

### 6.22.7.30 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	ADDRESS		Address used in the TWI transfer																												

## 6.22.8 Electrical specification

### 6.22.8.1 TWIM interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{TWIM,SCL}$	Bit rates for TWIM <sup>29</sup>	100		400	kbps
$t_{TWIM,START}$	Time from STARTRX/STARTTX task to transmission started		1.5		$\mu$ s

### 6.22.8.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{TWIM,SU\_DAT}$	Data setup time before positive edge on SCL – all modes	300			ns
$t_{TWIM,HD\_DAT}$	Data hold time after negative edge on SCL – 100, 250 and 400 kbps	500			ns
$t_{TWIM,HD\_STA,100kbps}$	TWIM master hold time for START and repeated START condition, 100 kbps	9937.5			ns
$t_{TWIM,HD\_STA,250kbps}$	TWIM master hold time for START and repeated START condition, 250 kbps	3937.5			ns
$t_{TWIM,HD\_STA,400kbps}$	TWIM master hold time for START and repeated START condition, 400 kbps	2437.5			ns
$t_{TWIM,SU\_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100 kbps	5000			ns
$t_{TWIM,SU\_STO,250kbps}$	TWIM master setup time from SCL high to STOP condition, 250 kbps	2000			ns
$t_{TWIM,SU\_STO,400kbps}$	TWIM master setup time from SCL high to STOP condition, 400 kbps	1250			ns
$t_{TWIM,BUF,100kbps}$	TWIM master bus free time between STOP and START conditions, 100 kbps	5800			ns
$t_{TWIM,BUF,250kbps}$	TWIM master bus free time between STOP and START conditions, 250 kbps	2700			ns
$t_{TWIM,BUF,400kbps}$	TWIM master bus free time between STOP and START conditions, 400 kbps	2100			ns

<sup>29</sup> High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see [GPIO — General purpose input/output](#) on page 127 for more details.

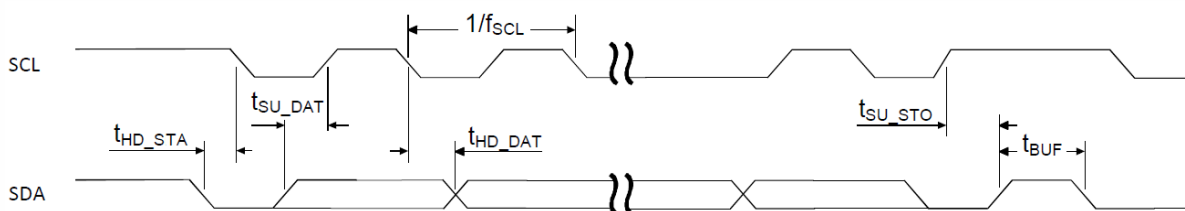


Figure 119: TWIM timing diagram, 1 byte transaction

### 6.22.9 Pullup resistor

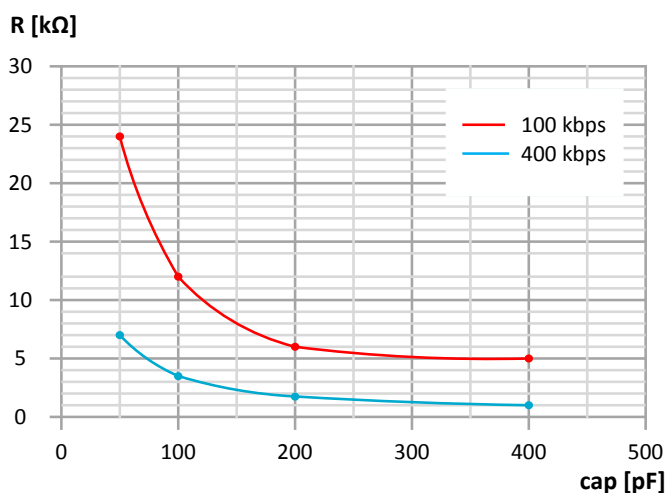


Figure 120: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The value of internal pullup resistor ( $R_{PU}$ ) for nRF52820 can be found in [GPIO — General purpose input/output](#) on page 127.

## 6.23 TWIS — I<sup>2</sup>C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I<sup>2</sup>C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

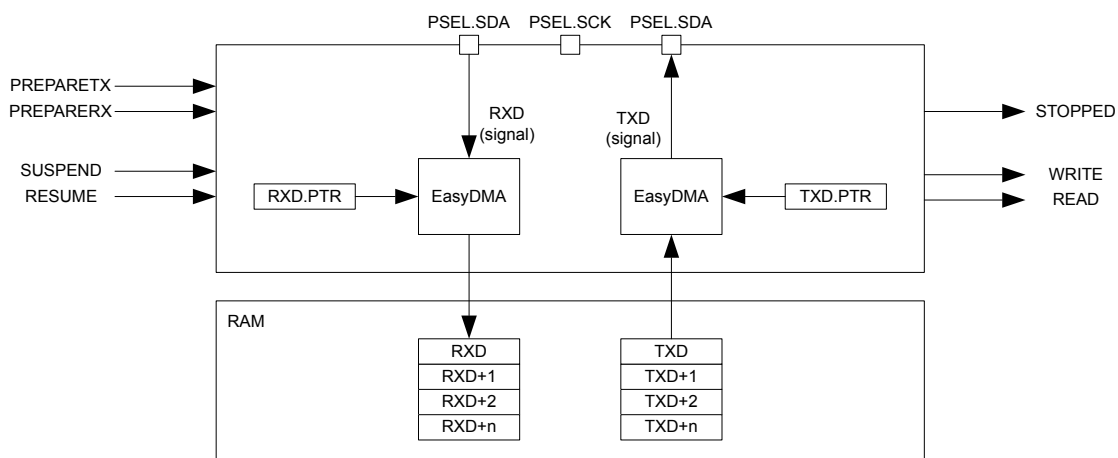


Figure 121: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see the following figure. TWI is only able to operate with a single master on the TWI bus.

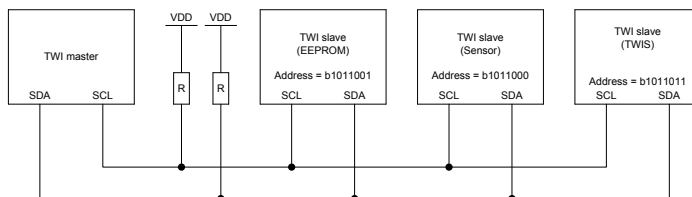


Figure 122: A typical TWI setup comprising one master and three slaves

The following figure shows the TWI slave state machine.

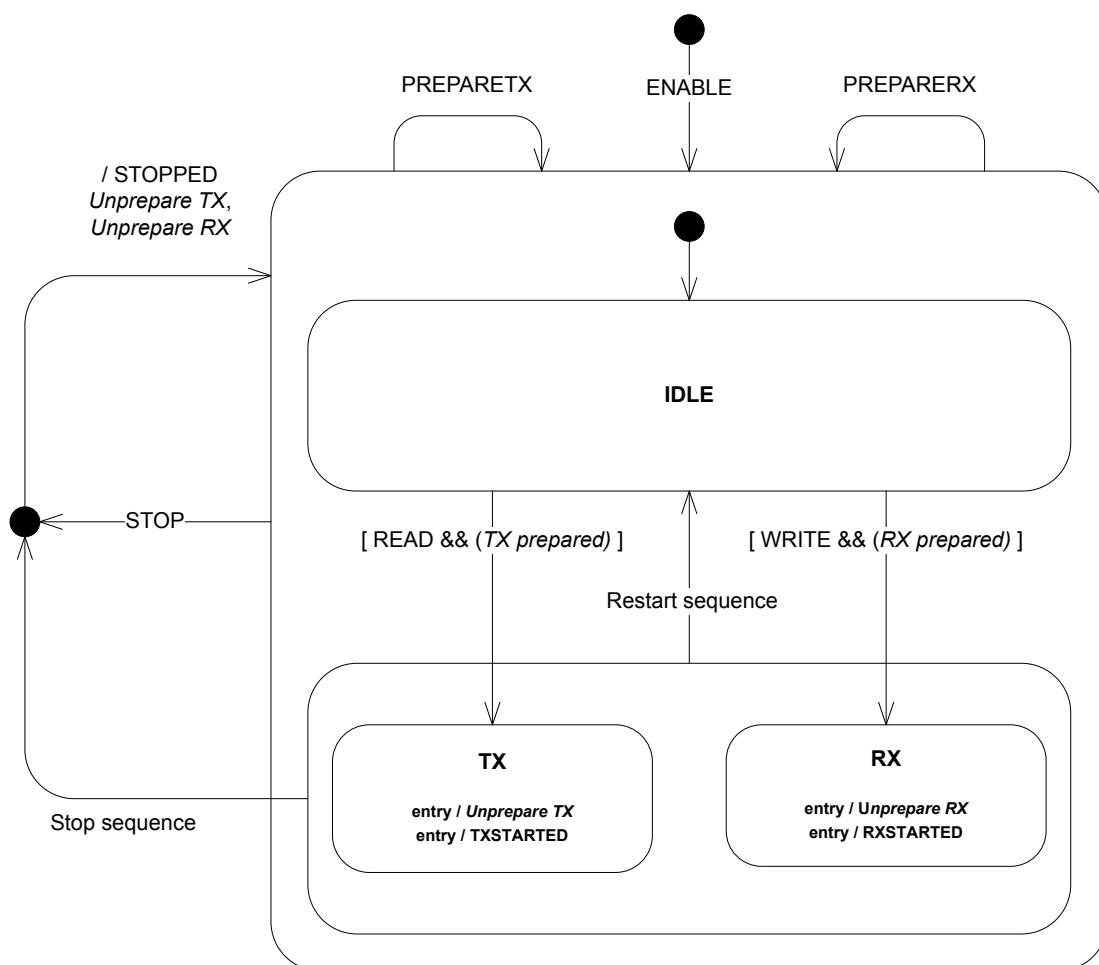


Figure 123: TWI slave state machine

The following table contains descriptions of the symbols used in the state machine.

Symbol	Type	Description
ENABLE	Register	The TWI slave has been enabled via the <code>ENABLE</code> register.
PREPARETX	Task	The <code>TASKS_PREPARETX</code> task has been triggered.
STOP	Task	The <code>TASKS_STOP</code> task has been triggered.
PREPARERX	Task	The <code>TASKS_PREPARERX</code> task has been triggered.
STOPPED	Event	The <code>EVENTS_STOPPED</code> event was generated.
RXSTARTED	Event	The <code>EVENTS_RXSTARTED</code> event was generated.
TXSTARTED	Event	The <code>EVENTS_TXSTARTED</code> event was generated.
TX prepared	Internal	Internal flag indicating that a <code>TASKS_PREPARETX</code> task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a <code>TASKS_PREPARERX</code> task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next <code>TASKS_PREPARETX</code> task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next <code>TASKS_PREPARERX</code> task.
Stop condition	TWI protocol	A TWI stop condition was detected.
Restart condition	TWI protocol	A TWI restart condition was detected.

Table 97: TWI slave state machine symbols

The TWI slave can perform clock stretching, with the premise that the master is able to support it.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behavior of the TWI slave, `PSEL.SCL`, `PSEL.SDA`, `CONFIG`, and the `ADDRESS[n]` registers must be configured prior to enabling the TWI slave through the `ENABLE` register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behavior.

### 6.23.1 EasyDMA

The TWIS implements EasyDMA for accessing RAM without CPU involvement.

The following table shows the Easy DMA channels that the TWIS peripheral implements.

Channel	Type	Register Cluster
TXD	READER	TXD
RXD	WRITER	RXD

Table 98: TWIS EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 37.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

### 6.23.2 TWI slave responding to a read command

Before the TWI slave can respond to a read command, the TWI slave must be configured correctly and enabled via the `ENABLE` register. When enabled, the TWI slave will be in its IDLE state.

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the `READ/WRITE` bit set to 1 (`WRITE=0`, `READ=1`). The `READ/WRITE` bit is followed by an `ACK/NACK` bit (`ACK=0` or `NACK=1`) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. This is configured in the `ADDRESS` registers and the `CONFIG` register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received, the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also [Terminating an ongoing TWI transaction](#) on page 328.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is shown in the following figure. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

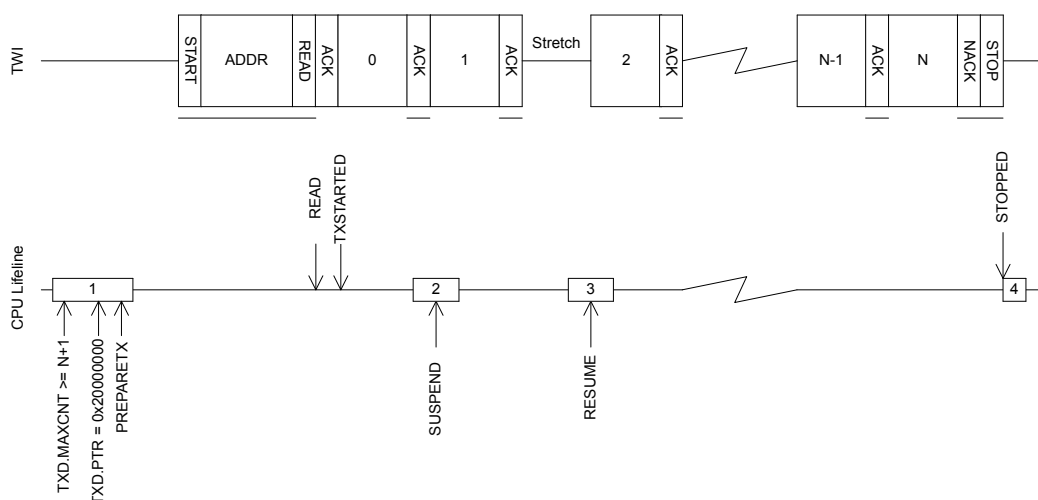


Figure 124: The TWI slave responding to a read command

### 6.23.3 TWI slave responding to a write command

Before the TWI slave can respond to a write command, the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled, the TWI slave will be in its IDLE state.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. This is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received, the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.

The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state, the TWI slave will be able to receive the bytes sent by the TWI master.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the RXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than it can receive, the extra bytes are discarded and NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also [Terminating an ongoing TWI transaction](#) on page 328.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is shown in the following figure. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

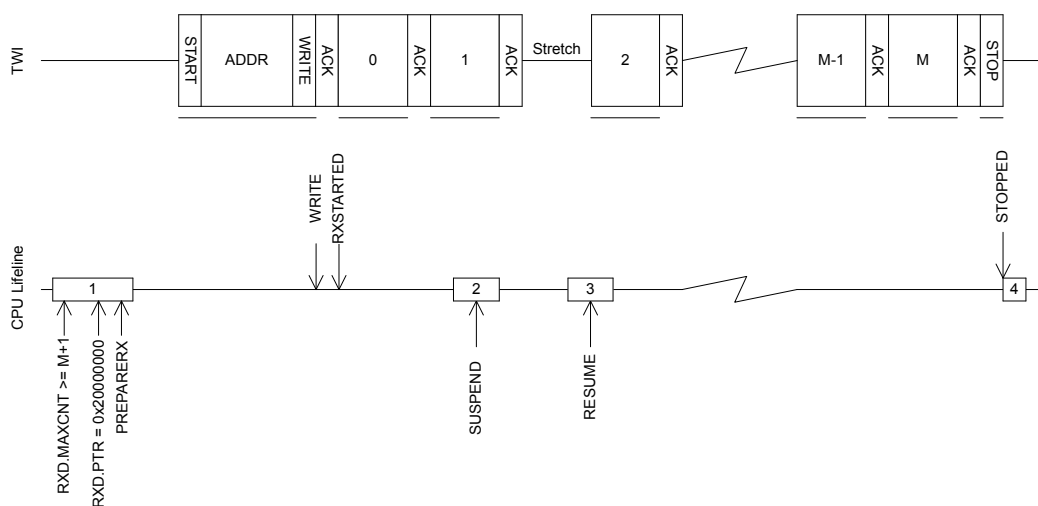


Figure 125: The TWI slave responding to a write command

### 6.23.4 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in the following figure.

In this example, the receiver does not know what the master wants to read in advance. This information is in the first two received bytes of the write in the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.

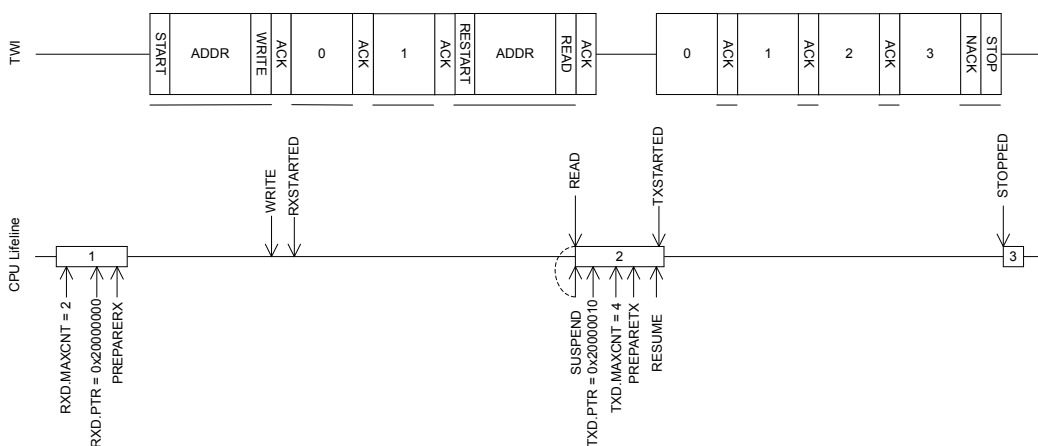


Figure 126: Repeated start sequence

### 6.23.5 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation, a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.



### 6.23.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

### 6.23.7 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in the following table.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	S0D1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1

Table 99: GPIO configuration before enabling peripheral

### 6.23.8 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 100: Instances

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcuts between local events and tasks
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

Register	Offset	Description
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

Table 101: Register overview

### 6.23.8.1 TASKS\_STOP

Address offset: 0x014

Stop TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STOP			Stop TWI transaction																											
			Trigger	1	Trigger task																											

### 6.23.8.2 TASKS\_SUSPEND

Address offset: 0x01C

Suspend TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_SUSPEND			Suspend TWI transaction																											
			Trigger	1	Trigger task																											

### 6.23.8.3 TASKS\_RESUME

Address offset: 0x020

Resume TWI transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_RESUME	Trigger	1	Resume TWI transaction Trigger task																												

### 6.23.8.4 TASKS\_PREPARERX

Address offset: 0x030

Prepare the TWI slave to respond to a write command

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_PREPARERX	Trigger	1	Prepare the TWI slave to respond to a write command Trigger task																												

### 6.23.8.5 TASKS\_PREPARETX

Address offset: 0x034

Prepare the TWI slave to respond to a read command

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_PREPARETX	Trigger	1	Prepare the TWI slave to respond to a read command Trigger task																												

### 6.23.8.6 EVENTS\_STOPPED

Address offset: 0x104

TWI stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_STOPPED	NotGenerated	0	TWI stopped Event not generated																												
		Generated	1	Event generated																												

### 6.23.8.7 EVENTS\_ERROR

Address offset: 0x124

TWI error

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_ERROR			TWI error																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.23.8.8 EVENTS\_RXSTARTED

Address offset: 0x14C

Receive sequence started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_RXSTARTED			Receive sequence started																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.23.8.9 EVENTS\_TXSTARTED

Address offset: 0x150

Transmit sequence started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_TXSTARTED			Transmit sequence started																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.23.8.10 EVENTS\_WRITE

Address offset: 0x164

Write command received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_WRITE			Write command received																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.23.8.11 EVENTS\_READ

Address offset: 0x168

Read command received

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	RW EVENTS_READ			Read command received																													
		NotGenerated	0	Event not generated																													
		Generated	1	Event generated																													

### 6.23.8.12 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																B A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW WRITE_SUSPEND			Shortcut between event <a href="#">WRITE</a> and task <a href="#">SUSPEND</a>																												
		Disabled	0	Disable shortcut																												
		Enabled	1	Enable shortcut																												
B	RW READ_SUSPEND			Shortcut between event <a href="#">READ</a> and task <a href="#">SUSPEND</a>																												
		Disabled	0	Disable shortcut																												
		Enabled	1	Enable shortcut																												

### 6.23.8.13 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																H G F E B A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW STOPPED			Enable or disable interrupt for event <a href="#">STOPPED</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												
B	RW ERROR			Enable or disable interrupt for event <a href="#">ERROR</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												
E	RW RXSTARTED			Enable or disable interrupt for event <a href="#">RXSTARTED</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												
F	RW TXSTARTED			Enable or disable interrupt for event <a href="#">TXSTARTED</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												
G	RW WRITE			Enable or disable interrupt for event <a href="#">WRITE</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												
H	RW READ			Enable or disable interrupt for event <a href="#">READ</a>																												
		Disabled	0	Disable																												
		Enabled	1	Enable																												

### 6.23.8.14 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	H G						F E						B						A												
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	STOPPED			Write '1' to enable interrupt for event <b>STOPPED</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
B	RW	ERROR			Write '1' to enable interrupt for event <b>ERROR</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
E	RW	RXSTARTED			Write '1' to enable interrupt for event <b>RXSTARTED</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
F	RW	TXSTARTED			Write '1' to enable interrupt for event <b>TXSTARTED</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
G	RW	WRITE			Write '1' to enable interrupt for event <b>WRITE</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
H	RW	READ			Write '1' to enable interrupt for event <b>READ</b>																										
			Set	1	Enable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										

### 6.23.8.15 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	H G						F E						B						A												
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	STOPPED			Write '1' to disable interrupt for event <b>STOPPED</b>																										
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
B	RW	ERROR			Write '1' to disable interrupt for event <b>ERROR</b>																										
			Clear	1	Disable																										
			Disabled	0	Read: Disabled																										
			Enabled	1	Read: Enabled																										
E	RW	RXSTARTED			Write '1' to disable interrupt for event <b>RXSTARTED</b>																										
			Clear	1	Disable																										

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID		H G								F E								B								A							
<b>Reset 0x00000000</b>		<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
F	RW TXSTARTED			Write '1' to disable interrupt for event <b>TXSTARTED</b>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
G	RW WRITE			Write '1' to disable interrupt for event <b>WRITE</b>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													
H	RW READ			Write '1' to disable interrupt for event <b>READ</b>																													
		Clear	1	Disable																													
		Disabled	0	Read: Disabled																													
		Enabled	1	Read: Enabled																													

### 6.23.8.16 ERRORSRC

Address offset: 0x4D0

Error source

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																														C B		A	
<b>Reset 0x00000000</b>		<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																													
A	RW OVERFLOW			RX buffer overflow detected, and prevented																													
		NotDetected	0	Error did not occur																													
		Detected	1	Error occurred																													
B	RW DNACK			NACK sent after receiving a data byte																													
		NotReceived	0	Error did not occur																													
		Received	1	Error occurred																													
C	RW OVERREAD			TX buffer over-read detected, and prevented																													
		NotDetected	0	Error did not occur																													
		Detected	1	Error occurred																													

### 6.23.8.17 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A	
<b>Reset 0x00000000</b>		<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																													
A	R MATCH		[0..1]	Indication of which address in {ADDRESS} that matched the incoming address																													

### 6.23.8.18 ENABLE

Address offset: 0x500

## Enable TWIS

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW ENABLE			Enable or disable TWIS																														
		Disabled	0	Disable TWIS																														
		Enabled	9	Enable TWIS																														

## 6.23.8.19 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID	C																														A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

## 6.23.8.20 PSEL.SDA

Address offset: 0x50C

Pin select for SDA signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID	C																														A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

## 6.23.8.21 RXD.PTR

Address offset: 0x534

RXD Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW PTR			RXD Data pointer																											

See the memory chapter for details about which memories are available for EasyDMA.



### 6.23.8.22 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																								
ID																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																																								
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	MAXCNT	[0..0x7FFF]	Maximum number of bytes in RXD buffer																																																					

### 6.23.8.23 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																								
ID																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																																								
ID	Acce Field	Value ID	Value	Description																																																					
A	R	AMOUNT	[0..0x7FFF]	Number of bytes transferred in the last RXD transaction																																																					

### 6.23.8.24 RXD.LIST

Address offset: 0x540

EasyDMA list type

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	LIST		List type																												
		Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

### 6.23.8.25 TXD.PTR

Address offset: 0x544

TXD Data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	PTR		TXD Data pointer																											

See the memory chapter for details about which memories are available for EasyDMA.

### 6.23.8.26 TXD.MAXCNT

Address offset: 0x548

## Maximum number of bytes in TXD buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																									
ID																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0 0																																																									
ID	Acce Field	Value ID	Value	Description																																																						
A	RW	MAXCNT	[0..0x7FFF]	Maximum number of bytes in TXD buffer																																																						

## 6.23.8.27 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																								
ID																															A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0 0																																																								
ID	Acce Field	Value ID	Value	Description																																																					
A	R	AMOUNT	[0..0x7FFF]	Number of bytes transferred in the last TXD transaction																																																					

## 6.23.8.28 TXD.LIST

Address offset: 0x550

EasyDMA list type

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																															A	A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	LIST		List type																												
		Disabled	0	Disable EasyDMA list																												
		ArrayList	1	Use array list																												

## 6.23.8.29 ADDRESS[n] (n=0..1)

Address offset: 0x588 + (n × 0x4)

TWI slave address n

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																															A	A	A	A	A	A
Reset 0x00000000	0 0																																			
ID	Acce Field	Value ID	Value	Description																																
A	RW	ADDRESS		TWI slave address																																

## 6.23.8.30 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																										
ID																															B	A																										
Reset	0x00000001																														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ID	Acce Field	Value ID	Value	Description																																																						
A-B	RW	ADDRESS[i] (i=0..1)		Enable or disable address matching on ADDRESS[i]																																																						
		Disabled	0	Disabled																																																						
		Enabled	1	Enabled																																																						

### 6.23.8.31 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																											A	A	A	A	A	A	A																								
Reset	0x00000000																														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																					
A	RW	ORC		Over-read character. Character sent out in case of an over-read of the transmit buffer.																																																					

## 6.23.9 Electrical specification

### 6.23.9.1 TWIS slave timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
f <sub>TWIS,SCL</sub>	Bit rates for TWIS <sup>30</sup>	100		400	kbps
t <sub>TWIS,START</sub>	Time from PREPARERX/PREPARETX task to ready to receive/transmit		1.5		μs
t <sub>TWIS,SU_DAT</sub>	Data setup time before positive edge on SCL – all modes	300			ns
t <sub>TWIS,HD_DAT</sub>	Data hold time after negative edge on SCL – all modes	500			ns
t <sub>TWIS,HD_STA,100kbps</sub>	TWI slave hold time from for START condition (SDA low to SCL low), 100 kbps	5200			ns
t <sub>TWIS,HD_STA,400kbps</sub>	TWI slave hold time from for START condition (SDA low to SCL low), 400 kbps	1300			ns
t <sub>TWIS,SU_STO,100kbps</sub>	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
t <sub>TWIS,SU_STO,400kbps</sub>	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
t <sub>TWIS,BUF,100kbps</sub>	TWI slave bus free time between STOP and START conditions, 100 kbps		4700		ns
t <sub>TWIS,BUF,400kbps</sub>	TWI slave bus free time between STOP and START conditions, 400 kbps		1300		ns

<sup>30</sup> High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see [GPIO](#) chapter for more details.

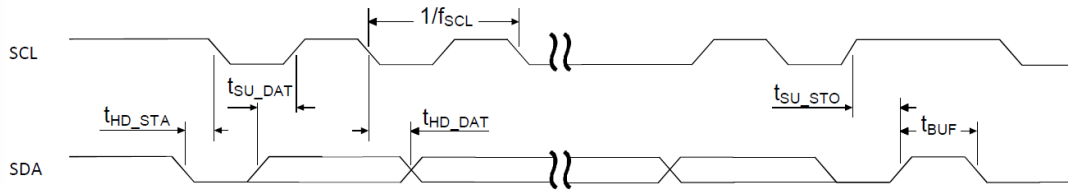


Figure 127: TWIS timing diagram, 1 byte transaction

## 6.24 UART — Universal asynchronous receiver/transmitter

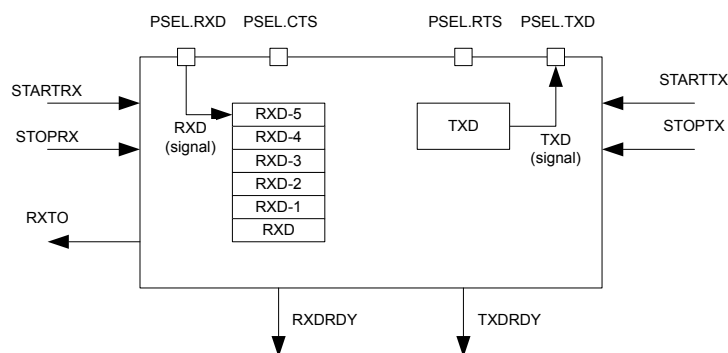


Figure 128: UART configuration

### 6.24.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- Automatic flow control
- Parity checking and generation for the 9<sup>th</sup> data bit

As illustrated in [UART configuration](#) on page 340, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

**Note:** The external crystal oscillator must be enabled to obtain sufficient clock accuracy for stable communication. See [CLOCK — Clock control](#) on page 69 for more information.

### 6.24.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated UART signal will not be connected to any physical pin. The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in [Pin configuration](#) on page 340.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

UART pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1
TXD	Output	1

Table 102: GPIO configuration

### 6.24.3 Shared resources

The UART shares registers and resources with other peripherals that have the same ID as the UART.

All peripherals with the same ID as the UART must be disabled before configuring and using the UART. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See [Instantiation](#) on page 18 for details on peripherals and their IDs.

### 6.24.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted, the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated, and resumed when CTS is activated again, as shown in the following figure. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see [Suspending the UART](#) on page 342.

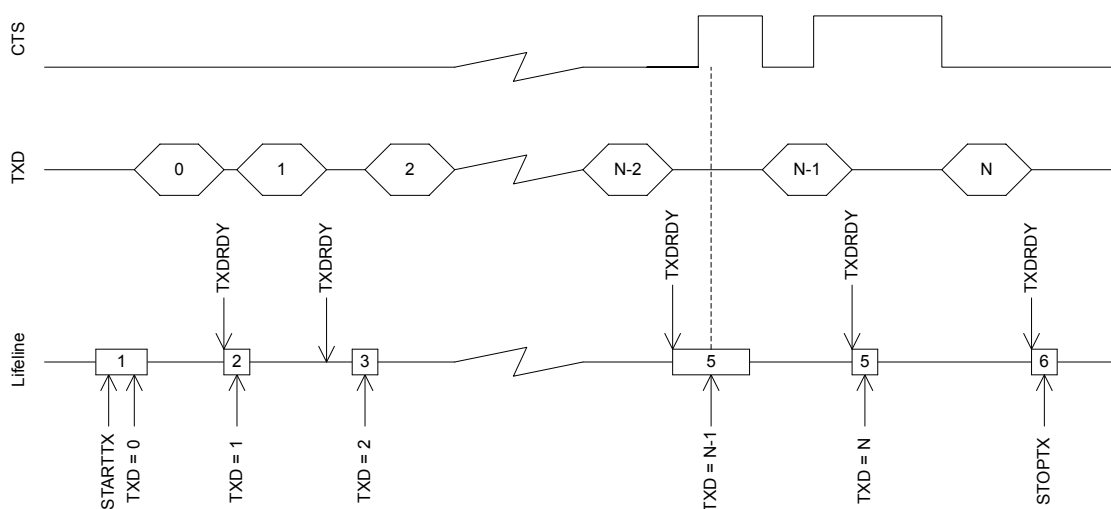


Figure 129: UART transmission

## 6.24.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO, a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.

The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see [UART reception](#) on page 342.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in [UART reception](#) on page 342. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data, the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and can generate a new event immediately after the RXD register is read (emptied) by the CPU.

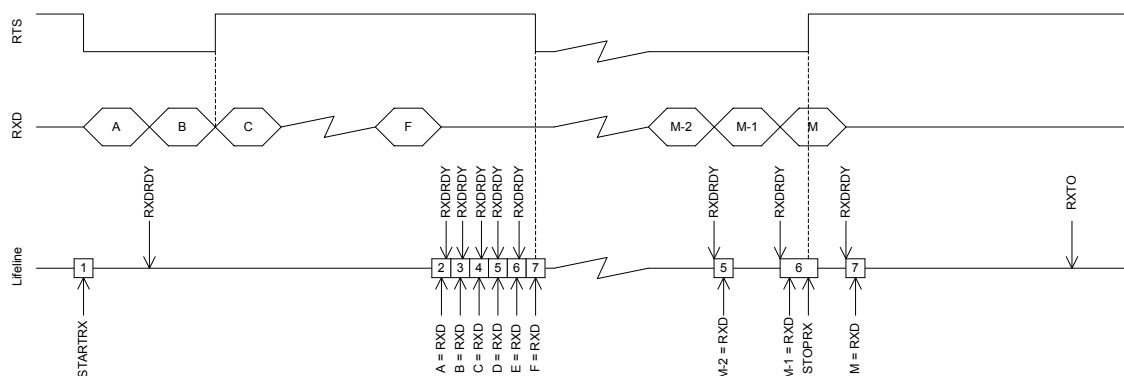


Figure 130: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

## 6.24.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

### 6.24.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

### 6.24.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

### 6.24.9 Parity and stop bit configuration

Automatic even parity generation for both transmission and reception can be configured using the register **CONFIG** on page 351. If odd parity is desired, it can be configured using the register **CONFIG** on page 351. See the register description for details.

The amount of stop bits can also be configured through the register **CONFIG** on page 351.

### 6.24.10 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UART	UART0	Universal asynchronous receiver/transmitter	Deprecated

Table 103: Instances

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXT0	0x144	Receiver timeout
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS
PSEL.TXD	0x50C	Pin select for TXD
PSEL.CTS	0x510	Pin select for CTS
PSEL.RXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.

Register	Offset	Description
CONFIG	0x56C	Configuration of parity and hardware flow control

Table 104: Register overview

### 6.24.10.1 TASKS\_STARTRX

Address offset: 0x000

Start UART receiver

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STARTRX	Trigger	1	Start UART receiver Trigger task																												

### 6.24.10.2 TASKS\_STOPRX

Address offset: 0x004

Stop UART receiver

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOPRX	Trigger	1	Stop UART receiver Trigger task																												

### 6.24.10.3 TASKS\_STARTTX

Address offset: 0x008

Start UART transmitter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STARTTX	Trigger	1	Start UART transmitter Trigger task																												

### 6.24.10.4 TASKS\_STOPTX

Address offset: 0x00C

Stop UART transmitter



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_STOPTX			Stop UART transmitter																												
		Trigger	1	Trigger task																												

### 6.24.10.5 TASKS\_SUSPEND

Address offset: 0x01C

Suspend UART

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_SUSPEND			Suspend UART																												
		Trigger	1	Trigger task																												

### 6.24.10.6 EVENTS\_CTS

Address offset: 0x100

CTS is activated (set low). Clear To Send.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_CTS			CTS is activated (set low). Clear To Send.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.7 EVENTS\_NCTS

Address offset: 0x104

CTS is deactivated (set high). Not Clear To Send.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_NCTS			CTS is deactivated (set high). Not Clear To Send.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.8 EVENTS\_RXDRDY

Address offset: 0x108

Data received in RXD

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_RXDRDY		Data received in RXD																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.9 EVENTS\_TXDRDY

Address offset: 0x11C

Data sent from TXD

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_TXDRDY		Data sent from TXD																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.10 EVENTS\_ERROR

Address offset: 0x124

Error detected

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ERROR		Error detected																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.11 EVENTS\_RXTO

Address offset: 0x144

Receiver timeout

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_RXTO		Receiver timeout																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.24.10.12 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																														B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW CTS_STARTRX	Disabled	0	Shortcut between event <a href="#">CTS</a> and task <a href="#">STARTRX</a> Disable shortcut																											
		Enabled	1	Enable shortcut																											
B	RW NCTS_STOPRX	Disabled	0	Shortcut between event <a href="#">NCTS</a> and task <a href="#">STOPRX</a> Disable shortcut																											
		Enabled	1	Enable shortcut																											

### 6.24.10.13 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID																														F	E	D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																		
ID	Acce Field	Value ID	Value	Description																															
A	RW CTS			Write '1' to enable interrupt for event <a href="#">CTS</a>																															
		Set	1	Enable																															
		Disabled	0	Read: Disabled																															
B	RW NCTS	Enabled	1	Read: Enabled																															
		Set	1	Write '1' to enable interrupt for event <a href="#">NCTS</a> Enable																															
		Disabled	0	Read: Disabled																															
C	RW RXDRDY	Enabled	1	Read: Enabled																															
		Set	1	Write '1' to enable interrupt for event <a href="#">RXDRDY</a> Enable																															
		Disabled	0	Read: Disabled																															
D	RW TXDRDY	Enabled	1	Read: Enabled																															
		Set	1	Write '1' to enable interrupt for event <a href="#">TXDRDY</a> Enable																															
		Disabled	0	Read: Disabled																															
E	RW ERROR	Enabled	1	Read: Enabled																															
		Set	1	Write '1' to enable interrupt for event <a href="#">ERROR</a> Enable																															
		Disabled	0	Read: Disabled																															
F	RW RXTO	Enabled	1	Read: Enabled																															
		Set	1	Write '1' to enable interrupt for event <a href="#">RXTO</a> Enable																															
		Disabled	0	Read: Disabled																															

### 6.24.10.14 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																					
ID		F																							E			D			C			B			A		
Reset 0x00000000		0 0																																					
ID	Acce Field	Value ID	Value	Description																																			
A	RW CTS			Write '1' to disable interrupt for event <a href="#">CTS</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
B	RW NCTS			Write '1' to disable interrupt for event <a href="#">NCTS</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
C	RW RXDRDY			Write '1' to disable interrupt for event <a href="#">RXDRDY</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
D	RW TXDRDY			Write '1' to disable interrupt for event <a href="#">TXDRDY</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
E	RW ERROR			Write '1' to disable interrupt for event <a href="#">ERROR</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			
F	RW RXTO			Write '1' to disable interrupt for event <a href="#">RXTO</a>																																			
		Clear	1	Disable																																			
		Disabled	0	Read: Disabled																																			
		Enabled	1	Read: Enabled																																			

### 6.24.10.15 ERRORSRC

Address offset: 0x480

Error source

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID																									D			C			B			A		
Reset 0x00000000		0 0																																		
ID	Acce Field	Value ID	Value	Description																																
A	RW OVERRUN			Overrun error																																
				A start bit is received while the previous data still lies in RXD. (Previous data is lost.)																																
		NotPresent	0	Read: error not present																																
		Present	1	Read: error present																																
B	RW PARITY			Parity error																																
				A character with bad parity is received, if HW parity check is enabled.																																
		NotPresent	0	Read: error not present																																
		Present	1	Read: error present																																
C	RW FRAMING			Framing error occurred																																
				A valid stop bit is not detected on the serial data input after all bits in a character have been received.																																
		NotPresent	0	Read: error not present																																

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															D	C	B	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce Field	Value ID	Value	Description																														
		Present	1	Read: error present																														
D	RW BREAK			Break condition																														
				The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.).																														
		NotPresent	0	Read: error not present																														
		Present	1	Read: error present																														

### 6.24.10.16 ENABLE

Address offset: 0x500

Enable UART

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID																															A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW ENABLE			Enable or disable UART																														
		Disabled	0	Disable UART																														
		Enabled	4	Enable UART																														

### 6.24.10.17 PSEL.RTS

Address offset: 0x508

Pin select for RTS

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID	C																														A	A	A	A
<b>Reset 0xFFFFFFFF</b>	<b>1 1</b>																																	
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

### 6.24.10.18 PSEL.TXD

Address offset: 0x50C

Pin select for TXD

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.24.10.19 PSEL.CTS

Address offset: 0x510

Pin select for CTS

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.24.10.20 PSEL.RXD

Address offset: 0x514

Pin select for RXD

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.24.10.21 RXD

Address offset: 0x518

RXD register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																												A A A A A A A A			
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	R	RXD			RX data received in previous transfers, double buffered																										

### 6.24.10.22 TXD

Address offset: 0x51C

TXD register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																									
ID																												A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0 0																																																								
ID	Acce	Field	Value ID	Value	Description																																																				
A	W	TXD			TX data to be transferred																																																				

### 6.24.10.23 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x04000000</b>	0 0 0 0 0 1 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	BAUDRATE			Baud rate																											
			Baud1200	0x0004F000	1200 baud (actual rate: 1205)																											
			Baud2400	0x0009D000	2400 baud (actual rate: 2396)																											
			Baud4800	0x0013B000	4800 baud (actual rate: 4808)																											
			Baud9600	0x00275000	9600 baud (actual rate: 9598)																											
			Baud14400	0x003B0000	14400 baud (actual rate: 14414)																											
			Baud19200	0x004EA000	19200 baud (actual rate: 19208)																											
			Baud28800	0x0075F000	28800 baud (actual rate: 28829)																											
			Baud31250	0x00800000	31250 baud																											
			Baud38400	0x009D5000	38400 baud (actual rate: 38462)																											
			Baud56000	0x00E50000	56000 baud (actual rate: 55944)																											
			Baud57600	0x00EBF000	57600 baud (actual rate: 57762)																											
			Baud76800	0x013A9000	76800 baud (actual rate: 76923)																											
			Baud115200	0x01D7E000	115200 baud (actual rate: 115942)																											
			Baud230400	0x03AFB000	230400 baud (actual rate: 231884)																											
			Baud250000	0x04000000	250000 baud																											
			Baud460800	0x075F7000	460800 baud (actual rate: 470588)																											
			Baud921600	0x0EBED000	921600 baud (actual rate: 941176)																											
			Baud1M	0x10000000	1Mega baud																											

### 6.24.10.24 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																										
ID																												D																														A
<b>Reset 0x00000000</b>	0 0																																																									
ID	Acce	Field	Value ID	Value	Description																																																					
A	RW	HWFC			Hardware flow control																																																					
			Disabled	0	Disabled																																																					
			Enabled	1	Enabled																																																					
B	RW	PARITY			Parity																																																					
			Excluded	0x0	Exclude parity bit																																																					
			Included	0x7	Include parity bit																																																					
C	RW	STOP			Stop bits																																																					
			One	0	One stop bit																																																					
			Two	1	Two stop bits																																																					

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
ID																								D				C	B	B	B	A															
Reset 0x00000000	0 0																																														
ID	Acce	Field	Value	ID	Value	Description																																									
D	RW	PARITYTYPE				Even or odd parity type																																									
			Even		0	Even parity																																									
			Odd		1	Odd parity																																									

## 6.24.11 Electrical specification

### 6.24.11.1 UART electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{UART}}$	Baud rate for UART <sup>31</sup> .			1000	kbps
$t_{\text{UART,CTSH}}$	CTS high time	1			$\mu\text{s}$
$t_{\text{UART,START}}$	Time from STARTRX/STARTTX task to transmission started		1		$\mu\text{s}$

## 6.25 UARTE — Universal asynchronous receiver/transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- Automatic hardware flow control
- Optional even parity bit checking and generation
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- One or two stop bit
- Least significant bit (LSB) first

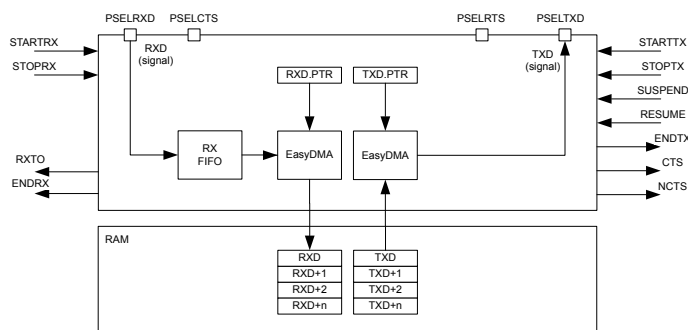


Figure 131: UARTE configuration

<sup>31</sup> High baud rates may require GPIOs to be set as High Drive, see [GPIO](#) for more details.



The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

**Note:** The external crystal oscillator must be enabled to obtain sufficient clock accuracy for stable communication. See [CLOCK — Clock control](#) on page 69 for more information.

### 6.25.1 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 15 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX and ENDTX events indicate that the EasyDMA is finished accessing the RX or TX buffer in RAM.

### 6.25.2 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task. A TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled through the HWFC field in the CONFIG register, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as shown in the following figure. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

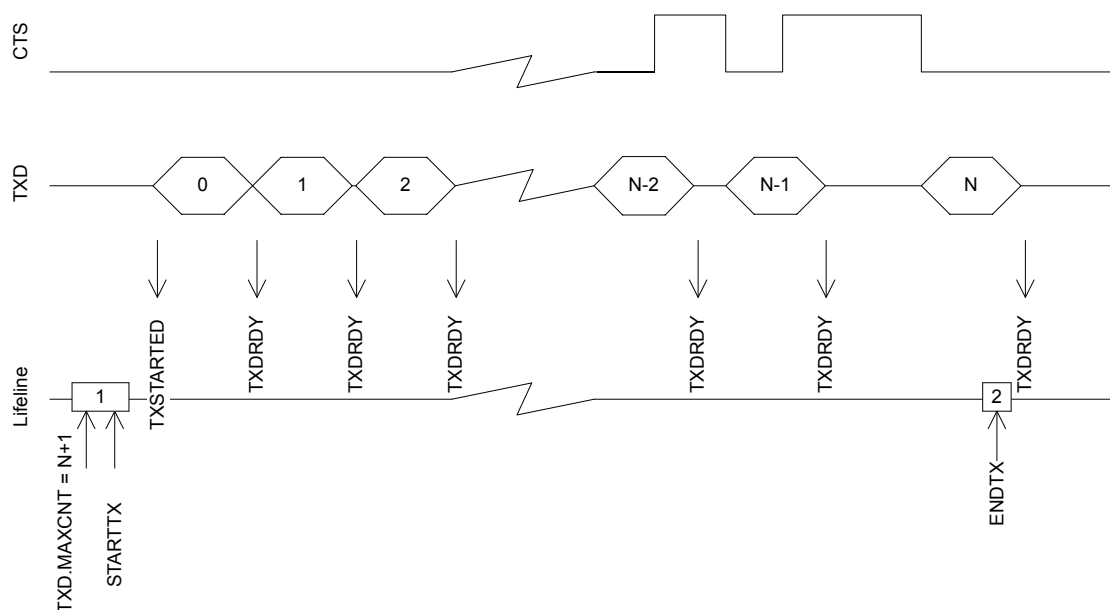


Figure 132: UART transmission

The UART transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via `STARTTX` or after it has been stopped via `STOPTX` and the `TXSTOPPED` event has been generated. See [POWER — Power supply](#) on page 49 for more information about power modes.

### 6.25.3 Reception

The UART receiver is started by triggering the `STARTRX` task. The UART receiver is using EasyDMA to store incoming data in an RX buffer in RAM.

The RX buffer is located at the address specified in the `RXD.PTR` register. The `RXD.PTR` register is double-buffered and it can be updated and prepared for the next `STARTRX` task immediately after the `RXSTARTED` event is generated. The size of the RX buffer is specified in the `RXD.MAXCNT` register. The UART generates an `ENDRX` event when it has filled up the RX buffer, as seen in the following figure.

For each byte received over the `RXD` line, an `RXDRDY` event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The `RXD.AMOUNT` register can be queried following an `ENDRX` event to see how many new bytes have been transferred to the RX buffer in RAM since the previous `ENDRX` event.

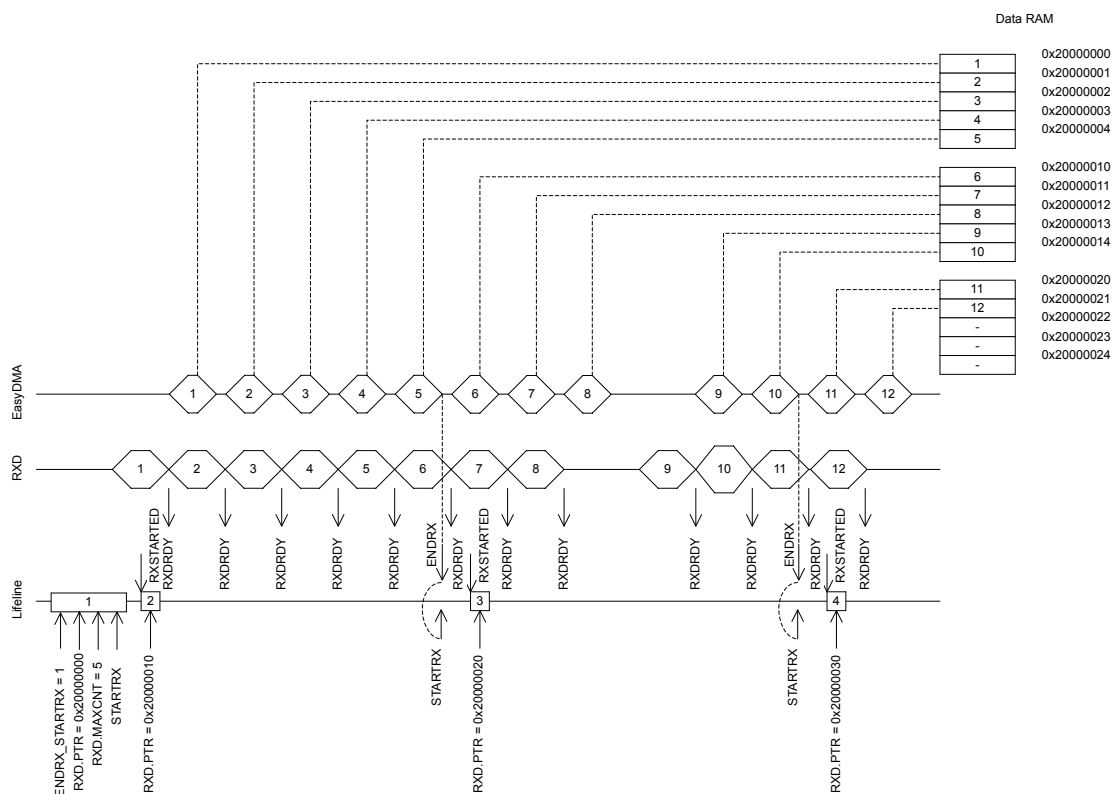


Figure 133: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

**Note:** If the ENDRX event has not been generated when the UARTE receiver stops, indicating that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To determine the amount of bytes the RX buffer has received, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered, as long as these are sent in succession immediately after the RTS signal is deactivated. After the RTS is deactivated, the UART is able to receive bytes for a period of time equal to the time needed to send four bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered. To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to  $RXD.MAXCNT > 4$ , as seen in the following figure. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

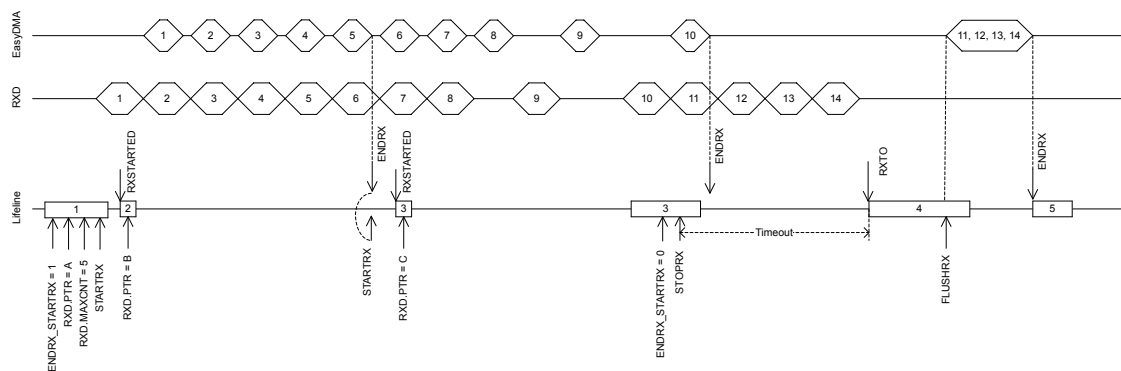


Figure 134: UARTE reception with forced stop via STOPRX

If HW flow control is enabled through the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See [POWER — Power supply](#) on page 49 for more information about power modes.

### 6.25.4 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

### 6.25.5 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

### 6.25.6 Parity and stop bit configuration

Automatic even parity generation for both transmission and reception can be configured using the register [CONFIG](#) on page 370. If odd parity is desired, it can be configured using the register [CONFIG](#) on page 370. See the register description for details.

The amount of stop bits can also be configured through the register [CONFIG](#) on page 370.

### 6.25.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOPTH and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTH and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

## 6.25.8 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS, PSEL.RTS, and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in the following table.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

Table 105: GPIO configuration before enabling peripheral

## 6.25.9 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal asynchronous receiver/transmitter with EasyDMA, unit 0	

Table 106: Instances

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD (but potentially not yet transferred to Data RAM)
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXT0	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcuts between local events and tasks
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

Register	Offset	Description
ERRORSRC	0x480	Error source
		This register is read/write one to clear.
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

Table 107: Register overview

### 6.25.9.1 TASKS\_STARTRX

Address offset: 0x000

Start UART receiver

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acces	Field	Value ID	Value	Description																										
A	W	TASKS_STARTRX			Start UART receiver																										
			Trigger	1	Trigger task																										

### 6.25.9.2 TASKS\_STOPRX

Address offset: 0x004

Stop UART receiver

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acces	Field	Value ID	Value	Description																										
A	W	TASKS_STOPRX			Stop UART receiver																										
			Trigger	1	Trigger task																										

### 6.25.9.3 TASKS\_STARTTX

Address offset: 0x008

Start UART transmitter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STARTTX	Trigger	1	Start UART transmitter Trigger task																											

#### 6.25.9.4 TASKS\_STOPTX

Address offset: 0x00C

Stop UART transmitter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STOPTX	Trigger	1	Stop UART transmitter Trigger task																											

#### 6.25.9.5 TASKS\_FLUSHRX

Address offset: 0x02C

Flush RX FIFO into RX buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_FLUSHRX	Trigger	1	Flush RX FIFO into RX buffer Trigger task																											

#### 6.25.9.6 EVENTS\_CTS

Address offset: 0x100

CTS is activated (set low). Clear To Send.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	RW	EVENTS_CTS	NotGenerated	0	CTS is activated (set low). Clear To Send. Event not generated																											
			Generated	1	Event generated																											

#### 6.25.9.7 EVENTS\_NCTS

Address offset: 0x104

CTS is deactivated (set high). Not Clear To Send.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																																A	
Reset	0x00000000																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																													
A	RW	EVENTS_NCTS		CTS is deactivated (set high). Not Clear To Send.																													
		NotGenerated	0	Event not generated																													
		Generated	1	Event generated																													

### 6.25.9.8 EVENTS\_RXDRDY

Address offset: 0x108

Data received in RXD (but potentially not yet transferred to Data RAM)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_RXDRDY		Data received in RXD (but potentially not yet transferred to Data RAM)																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.25.9.9 EVENTS\_ENDRX

Address offset: 0x110

Receive buffer is filled up

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_ENDRX		Receive buffer is filled up																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.25.9.10 EVENTS\_TXDRDY

Address offset: 0x11C

Data sent from TXD

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_TXDRDY		Data sent from TXD																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.25.9.11 EVENTS\_ENDTX

Address offset: 0x120

Last TX byte transmitted



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_ENDTX			Last TX byte transmitted																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.25.9.12 EVENTS\_ERROR

Address offset: 0x124

Error detected

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_ERROR			Error detected																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.25.9.13 EVENTS\_RXTO

Address offset: 0x144

Receiver timeout

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_RXTO			Receiver timeout																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.25.9.14 EVENTS\_RXSTARTED

Address offset: 0x14C

UART receiver has started

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
<b>Reset 0x00000000</b>	<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																											
A	RW EVENTS_RXSTARTED			UART receiver has started																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.25.9.15 EVENTS\_TXSTARTED

Address offset: 0x150

UART transmitter has started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_TXSTARTED		UART transmitter has started																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.25.9.16 EVENTS\_TXSTOPPED

Address offset: 0x158

Transmitter stopped

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_TXSTOPPED		Transmitter stopped																												
			NotGenerated	0	Event not generated																											
			Generated	1	Event generated																											

### 6.25.9.17 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C		
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
C	RW	ENDRX_STARTRX		Shortcut between event <a href="#">ENDRX</a> and task <a href="#">STARTRX</a>																												
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											
D	RW	ENDRX_STOPRX		Shortcut between event <a href="#">ENDRX</a> and task <a href="#">STOPRX</a>																												
			Disabled	0	Disable shortcut																											
			Enabled	1	Enable shortcut																											

### 6.25.9.18 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID											L	J	I	H											G	F	E	D	C	B	A	
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	CTS		Enable or disable interrupt for event <a href="#">CTS</a>																												
			Disabled	0	Disable																											
			Enabled	1	Enable																											
B	RW	NCTS		Enable or disable interrupt for event <a href="#">NCTS</a>																												
			Disabled	0	Disable																											
			Enabled	1	Enable																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	L J I H															G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
C	RW RXDRDY	Disabled	0	Disable																											
		Enabled	1	Enable																											
D	RW ENDRX	Disabled	0	Disable																											
		Enabled	1	Enable																											
E	RW TXDRDY	Disabled	0	Disable																											
		Enabled	1	Enable																											
F	RW ENDTX	Disabled	0	Disable																											
		Enabled	1	Enable																											
G	RW ERROR	Disabled	0	Disable																											
		Enabled	1	Enable																											
H	RW RXTO	Disabled	0	Disable																											
		Enabled	1	Enable																											
I	RW RXSTARTED	Disabled	0	Disable																											
		Enabled	1	Enable																											
J	RW TXSTARTED	Disabled	0	Disable																											
		Enabled	1	Enable																											
L	RW TXSTOPPED	Disabled	0	Disable																											
		Enabled	1	Enable																											

### 6.25.9.19 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	L J I H															G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW CTS	Set	1	Write '1' to enable interrupt for event CTS																											
		Disabled	0	Enable																											
		Enabled	1	Read: Disabled																											
B	RW NCTS	Set	1	Write '1' to enable interrupt for event NCTS																											
		Disabled	0	Enable																											
		Enabled	1	Read: Disabled																											
C	RW RXDRDY	Set	1	Write '1' to enable interrupt for event RXDRDY																											
		Disabled	0	Enable																											
		Enabled	1	Read: Disabled																											

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	L J I H															G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
D	RW ENDRX			Write '1' to enable interrupt for event <a href="#">ENDRX</a>																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
E	RW TXDRDY	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
F	RW ENDTX	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
G	RW ERROR	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
H	RW RXTO	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
I	RW RXSTARTED	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
J	RW TXSTARTED	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											
L	RW TXSTOPPED	Enabled	1	Read: Enabled																											
		Set	1	Enable																											
		Disabled	0	Read: Disabled																											

### 6.25.9.20 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	L J I H															G F E D C B A															
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW CTS			Write '1' to disable interrupt for event <a href="#">CTS</a>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
B	RW NCTS	Enabled	1	Read: Enabled																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		L J I H																G F E D C B A											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
		Enabled	1	Read: Enabled																									
C	RW RXDRDY			Write '1' to disable interrupt for event <a href="#">RXDRDY</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
D	RW ENDRX			Write '1' to disable interrupt for event <a href="#">ENDRX</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
E	RW TXDRDY			Write '1' to disable interrupt for event <a href="#">TXDRDY</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
F	RW ENDTX			Write '1' to disable interrupt for event <a href="#">ENDTX</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
G	RW ERROR			Write '1' to disable interrupt for event <a href="#">ERROR</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
H	RW RXTO			Write '1' to disable interrupt for event <a href="#">RXTO</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
I	RW RXSTARTED			Write '1' to disable interrupt for event <a href="#">RXSTARTED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
J	RW TXSTARTED			Write '1' to disable interrupt for event <a href="#">TXSTARTED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
L	RW TXSTOPPED			Write '1' to disable interrupt for event <a href="#">TXSTOPPED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									

### 6.25.9.21 ERRORSRC

Address offset: 0x480

Error source

This register is read/write one to clear.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												D	C	B	A	
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	OVERRUN		Overrun error																												
				A start bit is received while the previous data still lies in RXD. (Previous data is lost.)																												
		NotPresent	0	Read: error not present																												
		Present	1	Read: error present																												
B	RW	PARITY		Parity error																												
				A character with bad parity is received, if HW parity check is enabled.																												
		NotPresent	0	Read: error not present																												
		Present	1	Read: error present																												
C	RW	FRAMING		Framing error occurred																												
				A valid stop bit is not detected on the serial data input after all bits in a character have been received.																												
		NotPresent	0	Read: error not present																												
		Present	1	Read: error present																												
D	RW	BREAK		Break condition																												
				The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit).																												
		NotPresent	0	Read: error not present																												
		Present	1	Read: error present																												

### 6.25.9.22 ENABLE

Address offset: 0x500

Enable UART

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												A	A	A	A	
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	ENABLE		Enable or disable UARTE																												
				Disable UARTE																												
		Disabled	0	Disable UARTE																												
		Enabled	8	Enable UARTE																												

### 6.25.9.23 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.25.9.24 PSEL.TXD

Address offset: 0x50C

Pin select for TXD signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.25.9.25 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.25.9.26 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	C																											A A A A A			
Reset 0xFFFFFFFF	1 1																														
ID	Acce	Field	Value ID	Value	Description																										
A	RW	PIN		[0..31]	Pin number																										
C	RW	CONNECT			Connection																										
			Disconnected	1	Disconnect																										
			Connected	0	Connect																										

### 6.25.9.27 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x04000000	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	RW	BAUDRATE			Baud rate																											
			Baud1200	0x0004F000	1200 baud (actual rate: 1205)																											
			Baud2400	0x0009D000	2400 baud (actual rate: 2396)																											
			Baud4800	0x0013B000	4800 baud (actual rate: 4808)																											
			Baud9600	0x00275000	9600 baud (actual rate: 9598)																											
			Baud14400	0x003AF000	14400 baud (actual rate: 14401)																											
			Baud19200	0x004EA000	19200 baud (actual rate: 19208)																											
			Baud28800	0x0075C000	28800 baud (actual rate: 28777)																											
			Baud31250	0x00800000	31250 baud																											
			Baud38400	0x009D0000	38400 baud (actual rate: 38369)																											
			Baud56000	0x00E50000	56000 baud (actual rate: 55944)																											
			Baud57600	0x00EB0000	57600 baud (actual rate: 57554)																											
			Baud76800	0x013A9000	76800 baud (actual rate: 76923)																											
			Baud115200	0x01D60000	115200 baud (actual rate: 115108)																											
			Baud230400	0x03B00000	230400 baud (actual rate: 231884)																											
			Baud250000	0x04000000	250000 baud																											
			Baud460800	0x07400000	460800 baud (actual rate: 457143)																											
			Baud921600	0x0F000000	921600 baud (actual rate: 941176)																											
			Baud1M	0x10000000	1 megabaud																											

### 6.25.9.28 RXD.PTR

Address offset: 0x534

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce	Field	Value ID	Value	Description																											
A	RW	PTR			Data pointer																											

See the memory chapter for details about which memories are available for EasyDMA.

### 6.25.9.29 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer



Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[0..0x7FFF]	Maximum number of bytes in receive buffer																												

### 6.25.9.30 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNT	[0..0x7FFF]	Number of bytes transferred in the last transaction																												

### 6.25.9.31 TXD.PTR

Address offset: 0x544

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	PTR		Data pointer																												

See the memory chapter for details about which memories are available for EasyDMA.

### 6.25.9.32 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[0..0x7FFF]	Maximum number of bytes in transmit buffer																												

### 6.25.9.33 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A A A A A A A A A A A																															
Reset	0x00000000																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	Acce Field	Value ID	Value	Description																												
A	R	AMOUNT	[0..0x7FFF]	Number of bytes transferred in the last transaction																												

### 6.25.9.34 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																												D				C	B	B	B	A
Reset 0x00000000	0 0																																			
ID	Acce	Field	Value ID	Value	Description																															
A	RW	HWFC	Disabled	0	Hardware flow control Disabled																															
			Enabled	1	Enabled																															
B	RW	PARITY	Excluded	0x0	Parity Exclude parity bit																															
			Included	0x7	Include even parity bit																															
C	RW	STOP	One	0	Stop bits One stop bit																															
			Two	1	Two stop bits																															
D	RW	PARITYTYPE	Even	0	Even or odd parity type Even parity																															
			Odd	1	Odd parity																															

## 6.25.10 Electrical specification

### 6.25.10.1 UARTE electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
$f_{UARTE}$	Baud rate for UARTE <sup>32</sup> .			1000	kbps
$t_{UARTE,CTSH}$	CTS high time	1			$\mu$ s
$t_{UARTE,START}$	Time from STARTRX/STARTTX task to transmission started		1		$\mu$ s

## 6.26 USB — Universal serial bus device

The USB device (USB\_D) controller implements a full speed USB device function that meets 2.0 revision of the USB specification.

<sup>32</sup> High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

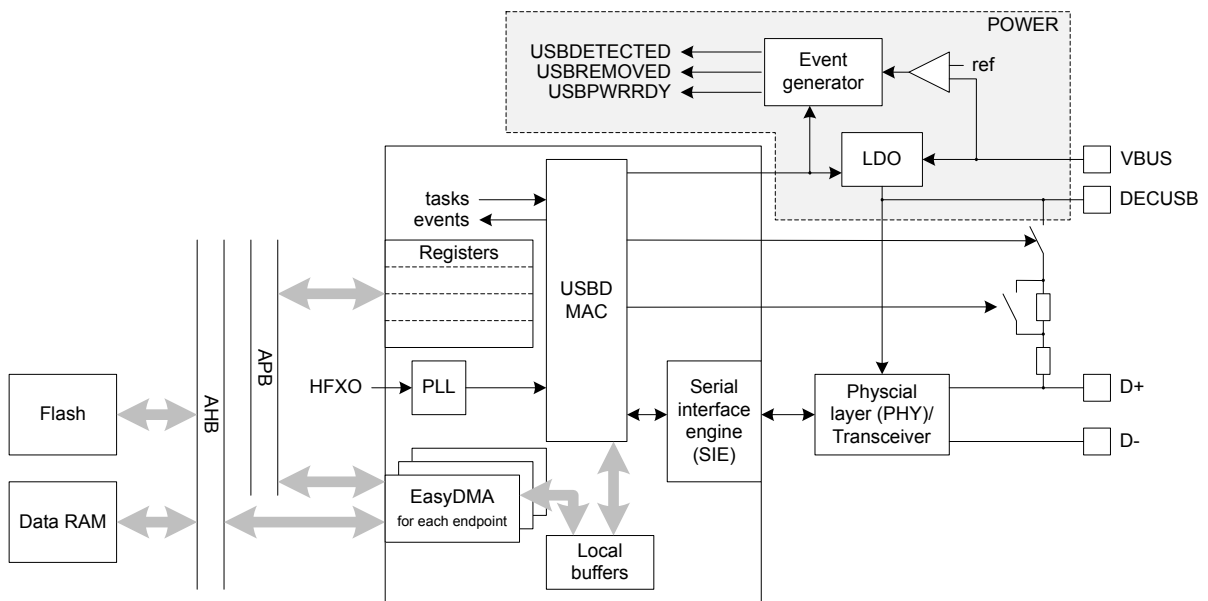


Figure 135: USB device block diagram

Listed here are the main features for USB:

- Full-speed (12 Mbps) device fully compliant to [Universal Serial Bus Specification Revision 2.0](#), including following engineering change notices (ECNs) issued by USB Implementers Forum:
  - *Pull-up/pull-down Resistors ECN*
  - *5V Short Circuit Withstand Requirement Change ECN*
- USB device stack available in the Nordic SDK
- Integrated (on-chip) USB transceiver (PHY)
- Software controlled on-chip pull-up on D+
- Endpoints:
  - Two control (1 IN, 1 OUT)
  - 14 bulk/interrupt (7 IN, 7 OUT)
  - Two isochronous (1 IN, 1 OUT)
- Double buffering for isochronous (ISO) endpoints (IN/OUT) support
- USB suspend, resume, and remote wake-up support
- 64 bytes buffer size for each bulk/interrupt endpoint
- Up to 1023 bytes buffer size for ISO endpoints
- EasyDMA for all data transfers

### 6.26.1 USB device states

The behavior of a USB device can be modelled through a state diagram.

The *USB 2.0 Specification* (see *Chapter 9 USB Device Framework*) defines a number of states for a USB device, as shown in the following figure.

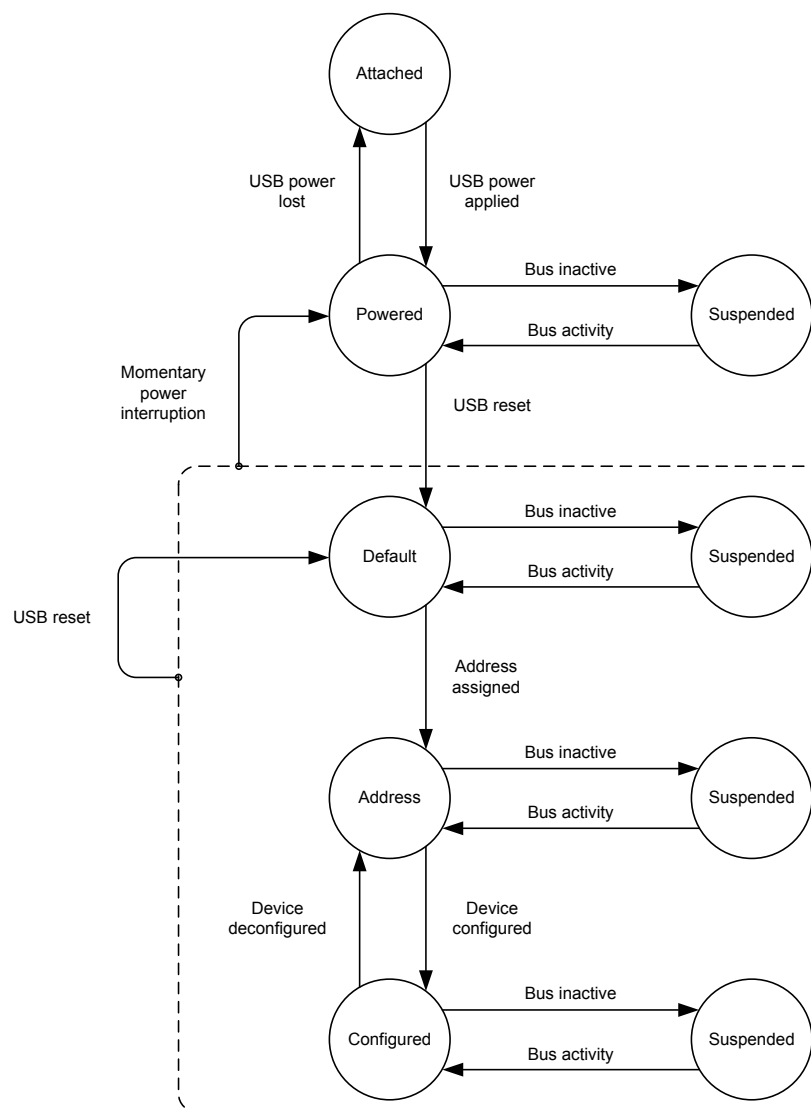


Figure 136: Device state diagram

The device must change state according to host-initiated traffic and USB bus states. It is up to the software to implement a state machine that matches the above definition. To detect the presence or absence of USB supply (VBUS), two events USBDETECTED and USBREMOVED can be used to implement the state machine. For more details on these events, see [USB supply](#) on page 54.

As a general rule when implementing the software, the host behavior shall never be assumed to be predictable. In particular the sequence of commands received during an enumeration. The software shall always react to the current bus conditions or commands sent by the host.

### 6.26.2 USB terminology

The USB specification defines bus states, rather than logic levels on the D+ and D- lines.

For a full speed device, the bus state where the D+ line is high and the D- line is low is defined as the J state. The bus state where D+ is low and D- high is called the K state.

An idle bus, where D+ and D- lines are only polarized through the pull-up on D+ and pull-downs on the host side, will be in J state.

Both lines low are called SE0 (single-ended 0), and both lines high SE1 (single-ended 1).

### 6.26.3 USB pins

The USBD peripheral features a number of dedicated pins.

The dedicated USB pins can be grouped in two categories, signal and power. The signal pins consist of the D+ and D- pins, which are to be connected to the USB host. They are dedicated pins, and not available as standard GPIOs. The USBD peripheral is implemented according to the USB specification revision 2.0, *5V Short Circuit Withstand ECN Requirement Change*, meaning these two pins are not 5 V tolerant.

The signal pins and the pull-up will operate only while VBUS is in its valid voltage range, and USBD is enabled through the **ENABLE** register. For details on the USB power supply and VBUS detection, see [USB supply](#) on page 54.

For more information about the pinout, see [Pin assignments](#) on page 415.

### 6.26.4 USBD power-up sequence

The physical layer interface (PHY)/USB transceiver is powered separately from the rest of the device (VBUS pin), which has some implications on the USBD power-up sequence.

The device is not able to properly signal its presence to the USB host and handle traffic from the host, unless the PHY's power supply is enabled and stable. Turning the PHY's power supply on/off is directly linked to register **ENABLE**. The device provides events that help synchronizing software to the various steps during the power-up sequence.

To make sure that all resources in USBD are available and the dedicated USB voltage regulator stabilized, the following is recommended:

- Enable USBD only after VBUS has been detected
- Turn the USB pull-up on after the following events have occurred:
  - USBPWRRDY
  - USBEVENT, with the READY condition flagged in **EVENTCAUSE**

The following sequence chart illustrates a typical handling of VBUS power-up:

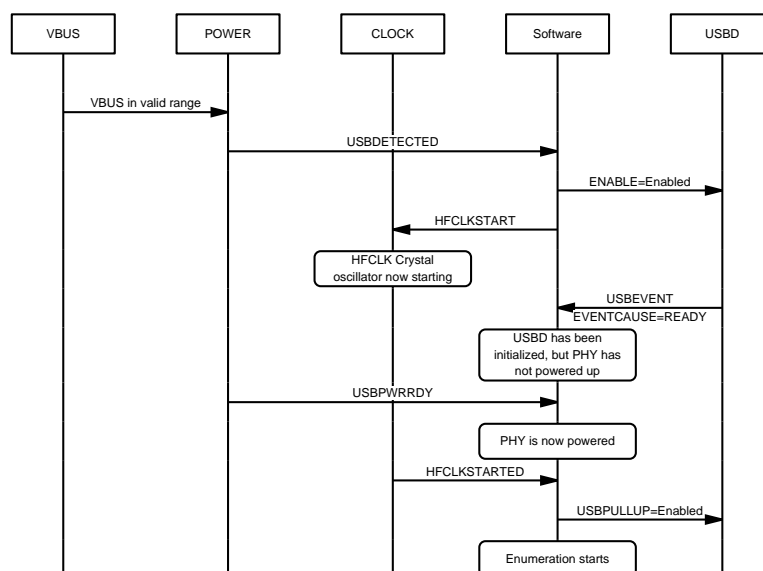


Figure 137: VBUS power-up sequence

Upon detecting VBUS removal, it is recommended to wait for ongoing EasyDMA transfers to finish before disabling USBD (relevant ENDEPIN[n], ENDISOIN, ENDEPOUT[n], or ENDISOOUT events, see [EasyDMA](#) on page 376). The USBREMOVED event, described in [USB supply](#) on page 54, signals when the VBUS is removed. Reading the **ENABLE** register will return Enabled until USBD is completely disabled.

### 6.26.5 USB pull-up

The USB pull-up serves two purposes: it indicates to the host that the device is connected to the USB bus, and it indicates the device's speed capability.

When no pull-up is connected to the USB bus, the host sees both D+ and D- lines low, as they are pulled down on the host side by 15 k $\Omega$  resistors. The device is not seen by the host and hence is in a detached state, even though it could be physically connected to the host. The USB Specification does not allow any current drawn on the VBUS in that type of situation.

When a full-speed device connects its 1.5 k $\Omega$  pull-up to D+, the host sees the corresponding line high. The device is then in the attached state. During the enumeration process, the host attempts to determine if the full-speed device also supports higher speeds and initiates communication with the device to further identify it. The USB peripheral implemented in this device supports only full-speed (12 Mbps), and thus ignores the negotiation for higher speeds in accordance with the USB specification revision 2.0.

Register `USBPULLUP` provides means to connect or disconnect the pull-up on D+ under software control. This allows the software to control when USB enumeration takes place. It also allows to emulate a physical disconnect from the USB bus, for instance when re-enumeration is required. `USBPULLUP` has to be enabled to allow the USB peripheral to handle USB traffic and generate appropriate events. This forbids the use of an external pull-up.

Note that disconnecting the pull-up through register `USBPULLUP` while connected to a host, will result in both D+ and D- lines to be pulled low by the host's pull-down resistors. However, as mentioned above, this will also inhibit the generation of the `USBRESET` event. The pull-up is disabled by default after a chip reset.

The pull-up shall only get connected after USB peripheral has been enabled through register `ENABLE`. The USB pull-up value is automatically changed depending on the bus activity, as specified in *Resistor ECN* which amends the original *USB 2.0 Specification*. The user does not have access to this function as it is handled in hardware.

While they should never be used in normal traffic activity, lines D+ and D- may at any time be forced into state specified in register `DPDMVALUE` by the task `DPDMDRIVE`. The `DPDMNODRIVE` task stops driving them, and PHY returns to normal operation.

### 6.26.6 USB reset

The USB specification defines a USB reset, which is not to be confused with a chip reset. The USB reset is a normal USB bus condition, and is used as part of the enumeration sequence, it does not reset the chip.

The USB reset results from a single-ended low state (SEO) on lines D+/D- for a  $t_{\text{USB,DETRST}}$  amount of time. Only the host is allowed to drive a USB reset condition on the bus. The USB peripheral automatically interprets a SEO longer than  $t_{\text{USB,DETRST}}$  as a USB reset. When the device detects a USB reset and generates a `USBRESET` event, the device USB stack and related parts of the application shall re-initialize themselves, and go back to the default state.

Some of the registers in the USB peripheral get automatically reset to a known state, in particular all data endpoints are disabled and the `USBADDR` reset to 0.

After the device has connected to the USB bus (i.e. after VBUS is applied), the device shall not respond to any traffic from the time the pull-up is enabled until it has seen a USB reset condition. This is automatically ensured by the USB peripheral.

After a USB reset, the device shall be fully responsive after at most  $T_{\text{RSTRCY}}$  (according to chapter 7 in the USB specification). Software shall take into account this time that takes the hardware to recover from a USB reset condition.

## 6.26.7 USB suspend and resume

Normally, the host will maintain activity on the USB at least every millisecond according to USB specification. A USB device will enter suspend when there is no activity on the bus (idle) for a given time. The device will resume operation when it receives any non idle signalling.

To signal that the device shall go into low power mode (suspend), the host stops activity on the USB bus, which becomes idle. Only the device pull-up and host pull-downs act on D+ and D-, and the bus is thus kept at a constant J state. It is up to the device to detect this lack of activity, and enter the low power mode (suspend) within a specified time.

The USB host can decide to suspend or resume USB activity at any time. If remote wake-up is enabled, the device may signal to the host to resume from suspend.

### 6.26.7.1 Entering suspend

The USB peripheral automatically detects lack of activity for more than a defined amount of time, and performs steps needed to enter suspend.

When no activity has been detected for longer than  $t_{\text{USB,SUSPEND}}$ , the USB peripheral generates the USBEVENT event with SUSPEND bit set in register `EVENTCAUSE`. The software shall ensure that the current drawn from the USB supply line VBUS is within the specified limits before  $T_{2\text{SUSP}}$ , as defined in chapter 7 of the USB specification. In order to reduce idle current of USB peripheral, the software must explicitly place the USB peripheral in low power mode through writing `LowPower` to register `LOWPOWER`.

In order to save power, and provided that no other peripheral needs it, the crystal oscillator (HFXO) in `CLOCK` may be disabled by software during the USB suspend, while the USB pull-up is disconnected, or when VBUS is not present. Software must explicitly enable it at any other time. The USB peripheral will not be able to respond to USB traffic unless HFXO is enabled and stable.

### 6.26.7.2 Host-initiated resume

Once the host resumes the bus activity, it has to be responsive to incoming requests on the USB bus within the time  $T_{\text{RSMRCY}}$  (as defined in chapter 7 of the USB specification) and revert to normal power consumption mode.

If the host resumes bus activity with or without a RESUME condition (in other words: bus activity is defined as any non-J state), the USB peripheral will generate a USBEVENT event, with RESUME bit set in register `EVENTCAUSE`. If the host resumes bus activity simply by restarting sending frames, the USB peripheral will generate SOF events.

### 6.26.7.3 Device-initiated remote wake-up

Assuming the remote wake-up is supported by the device and enabled by the host, the device can request the host to resume from suspend if wake-up condition is met.

To do so, the HFXO needs to be enabled first. After waking up the HFXO, the software must bring USB peripheral out of the low power mode and into the normal power consumption mode through writing `ForceNormal` in register `LOWPOWER`. It can then instruct the USB peripheral to drive a RESUME condition (K state) on the USB bus by triggering the `DPDMDRIVE` task, and hence attempt to wake up the host. By choosing `Resume` in `DPDMVALUE`, the duration of the RESUME state is under hardware control ( $t_{\text{USB,DRIVEK}}$ ). By choosing `J` or `K`, the duration of that state is under software control (the J or K state is maintained until a `DPDMNODRIVE` task is triggered) and has to meet  $T_{\text{DRSMUP}}$  as specified in USB specification chapter 7.

Upon writing the `ForceNormal` in register `LOWPOWER`, a USBEVENT event is generated with the `USBWUALLOWED` bit set in register `EVENTCAUSE`.

The value in register `DPDMVALUE` on page 404 will only be captured and used when the `DPDMDRIVE` task is triggered. This value defines the state the bus will be forced into after the `DPDMDRIVE` task.

The device shall ensure that it does not initiate a remote wake-up request before  $T_{WTRSM}$  (according to USB specification chapter 7) after the bus has entered idle state. Using the recommended resume value in [DPDMVALUE](#) (rather than K) takes care of this, and postpones the RESUME state accordingly.

## 6.26.8 EasyDMA

The USBD peripheral implements EasyDMA for accessing memory without CPU involvement.

Each endpoint has an associated set of registers, tasks and events. EasyDMA and traffic on USB are tightly related. A number of events provide insight of what is happening on the USB bus with a number of tasks allowing an automated response to the traffic.

**Note:** Endpoint 0 (IN and OUT) are implemented as control endpoint. For more information, see [Control transfers](#) on page 377.

### Registers

Enabling endpoints is controlled through the [EPINEN](#) and [EPOUTEN](#) registers.

The following registers define the memory address of the buffer for a specific IN or OUT endpoint:

- [EPIN\[n\].PTR](#), (n=0..7)
- [EPOUT\[n\].PTR](#), (n=0..7)
- [ISOIN.PTR](#)
- [ISOOUT.PTR](#)

The following registers define the amount of bytes to be sent on USB for next transaction:

- [EPIN\[n\].MAXCNT](#), (n=0..7)
- [ISOIN.MAXCNT](#)

The following registers define the length of the buffer (in bytes) for next transfer of incoming data:

- [EPOUT\[n\].MAXCNT](#), (n=1..7)
- [ISOOUT.MAXCNT](#)

Since the host decides how many bytes are sent over USB, the MAXCNT value can be copied from register [SIZE.EPOUT\[n\]](#) (n=1..7) or register [SIZE.ISOOUT](#).

Register [EPOUT\[0\].MAXCNT](#) defines the length of the OUT buffer (in bytes) for the control endpoint 0. Register [SIZE.EPOUT\[0\]](#) shall indicate the same value as `MaxPacketSize` from the device descriptor or `wLength` from the SETUP command, whichever is the least.

The [.AMOUNT](#) registers indicate how many bytes actually have been transferred over EasyDMA during the last transfer.

Stalling bulk/interrupt endpoints is controlled through the [EPSTALL](#) register.

**Note:** Due to USB specification requirements, the effect of the stalling control endpoint 0 may be overridden by hardware, in particular when a new SETUP token is received.

EasyDMA will not copy the SETUP data to memory (it will only transfer data from the data stage). The following are separate registers in the USBD peripheral that have setup data.

- [BMREQUESTTYPE](#)
- [BREQUEST](#)
- [WVALUEL](#)
- [WVALUEH](#)
- [WINDEXL](#)
- [WINDEXH](#)



- [WLENGTHL](#)
- [WLENGTHH](#)

The [EVENTCAUSE](#) register provides details on what caused a given USBEVENT event, for instance if a CRC error is detected during a transaction, or if bus activity stops or resumes.

## Tasks

Tasks [STARTEPIN\[n\]](#), [STARTEPOUT\[n\]](#) (n=0..7), [STARTISOIN](#), and [STARTISOOUT](#) capture the values for [.PTR](#) and [.MAXCNT](#) registers. For IN endpoints, a transaction over USB gets automatically triggered when the EasyDMA transfer is complete. For OUT endpoints, it is up to software to allow the next transaction over USB. See the examples in [Control transfers](#) on page 377, [Bulk and interrupt transactions](#) on page 380, and [Isochronous transactions](#) on page 382.

For the control endpoint 0, OUT transactions are allowed through the [EPORCVOUT](#) task. The [EPOSTATUS](#) task allows a status stage to be initiated, and the [EPOSTALL](#) task allows stalling further traffic (data or status stage) on the control endpoint.

## Events

The [STARTED](#) event confirms that the values of the [.PTR](#) and [.MAXCNT](#) registers of the endpoints flagged in register [EPSTATUS](#) have been captured. Those can then be modified by software for the next transfer.

Events [ENDEPIN\[n\]](#), [ENDEPOUT\[n\]](#) (n=0..7), [ENDISOIN](#), and [ENDISOOUT](#) events indicate that the entire buffer has been consumed. The buffer can be accessed safely by the software.

Only a single EasyDMA transfer can take place in USB at any time. Software must ensure that tasks [STARTEPIN\[n\]](#) (n=0..7), [STARTISOIN](#), [STARTEPOUT\[n\]](#) (n=0..7), or [STARTISOOUT](#) are not triggered before events [ENDEPIN\[n\]](#) (n=0..7), [ENDISOIN](#), [ENDEPOUT\[n\]](#) (n=0..7), or [ENDISOOUT](#) are received from an on-going transfer.

The [EPDATA](#) event indicates that a successful (acknowledged) data transaction has occurred on the data endpoint(s) flagged in register [EPDATASTATUS](#). A successful (acknowledged) data transaction on endpoint 0 is signalled by the [EPODATADONE](#) event.

At any time a [USBEVENT](#) event may be sent, with details provided in [EVENTCAUSE](#) register.

The [EPOSETUP](#) event indicates that a SETUP token has been received on the control endpoint 0, and that the setup data is available in [#unique\\_932/unique\\_932\\_Connect\\_42\\_setup\\_data\\_registers](#) on page 376.

### 6.26.9 Control transfers

The USB specification mandates every USB device to implement endpoint 0 IN and OUT as control endpoints.

A control transfer consists of two or three stages:

- Setup stage
- Data stage (optional)
- Status stage

Each control transfer can be one of following types:

- Control read
- Control read no data
- Control write
- Control write no data

An [EPOSETUP](#) event indicates that the data in the setup stage (following the SETUP token) is available in [registers](#).

The data in the data stage (following the IN or OUT token) is transferred from or to the desired location using EasyDMA.

The control endpoint buffer can be of any size.

After receiving the SETUP token, the USB controller will not accept (NAK) any incoming IN or OUT tokens until the software has finished decoding the command, determined the type of transfer, and prepared for the next stage (data or status) appropriately.

The software can stall a command when in the data and status stages, through the EPOSTALL task, when the command is not supported or if its wValue, wIndex or wLength parameters are wrong. The following shows a stalled control read transfer, but the same mechanism (tasks) applies to stalling a control write transfer.

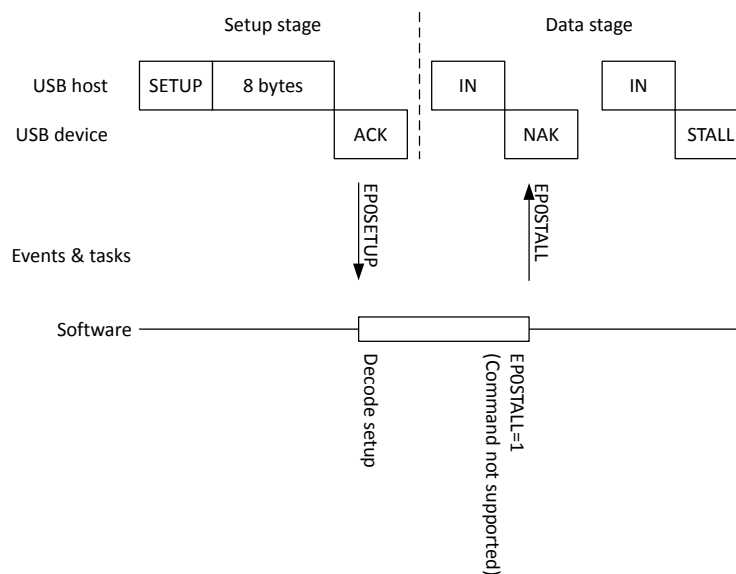


Figure 138: Control read gets stalled

See the *USB 2.0 Specification* and relevant class specifications for rules on stalling commands.

**Note:** The USB peripheral handles the SetAddress transfer by itself. As a consequence, the software shall not process this command other than updating its state machine (see [Device state diagram](#)), nor initiate a status stage. If necessary, the address assigned by the host can be read out from the USBADDR register after the command has been processed.

### 6.26.9.1 Control read transfer

This section describes how the software behaves when responding to a control read transfer.

As mentioned earlier, the USB controller will not accept (NAK) any incoming IN tokens until software has finished decoding the command, determining the type of transfer, and preparing for the next stage (data or status) appropriately.

For a control read, transferring the data from memory into USB will trigger a valid, acknowledged (ACK) IN transaction on USB.

The software has to prepare EasyDMA by pointing to the buffer containing the data to be transferred. If no other EasyDMA transfers are on-going with USB, the software can send the STARTEPIN0 task, which will initiate the data transfer and transaction on USB.

A STARTED event (with EPIN0 bit set in the EPSTATUS register) will be generated as soon as the EPIN[0].PTR and .MAXCNT registers have been captured. Software may then prepare them for the next data transaction.

An ENDEPIN[0] event will be generated when the data has been transferred from memory to the USB peripheral.

Finally, an EPODATADONE event will be generated when the data has been transmitted over USB and acknowledged by the host.

The software can then either prepare and transmit the next data transaction by repeating the above sequence, or initiate the status stage through the EPOSTATUS task.

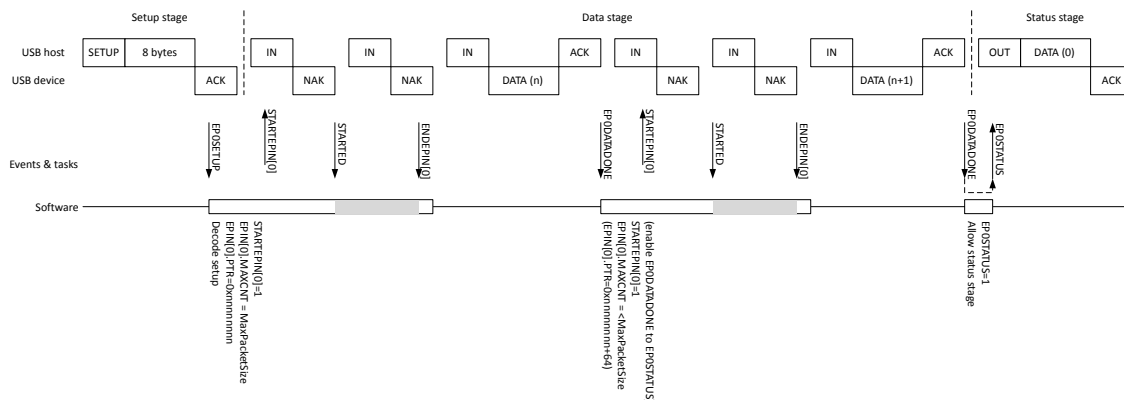


Figure 139: Control read transfer

It is possible to enable a shortcut from the EPODATADONE event to the EPOSTATUS task, typically if the data stage is expected to take a single transfer. If there is no data stage, the software can initiate the status stage through the EPOSTATUS task right away, as shown in the following figure.

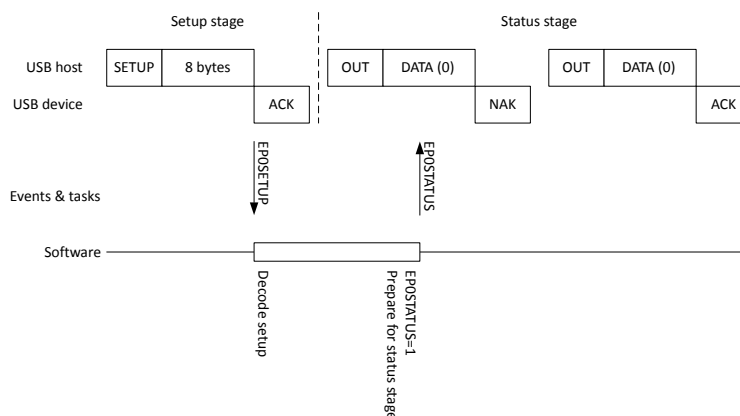


Figure 140: Control read no data transfer

### 6.26.9.2 Control write transfer

This section describes how the software responds to a control write transfer.

The software has to prepare EasyDMA by pointing to the buffer in memory that shall contain the incoming data. If no other EasyDMA transfers are ongoing with USB, the software can then send the EPORCVOUT task, which will make USB acknowledge (ACK) the first OUT+DATA transaction from the host.

An EPODATADONE event will be generated when a new OUT+DATA has been transmitted over USB, and is about to get acknowledged by the device.

After receiving the first transaction, a STARTED event (the EPOUT0 bit set in the EPSTATUS register) is generated when the EPOUT[0].PTR and .MAXCNT registers have been captured. Software may then prepare them for the next data transaction.

An ENDEPOUT[0] event will be generated when the data has been transferred from the USB peripheral to memory. The software can then either prepare to receive the next data transaction by repeating the above sequence, or initiate the status stage through the EPOSTATUS task. Until then, further incoming OUT +DATA transactions get a NAK response by the device.

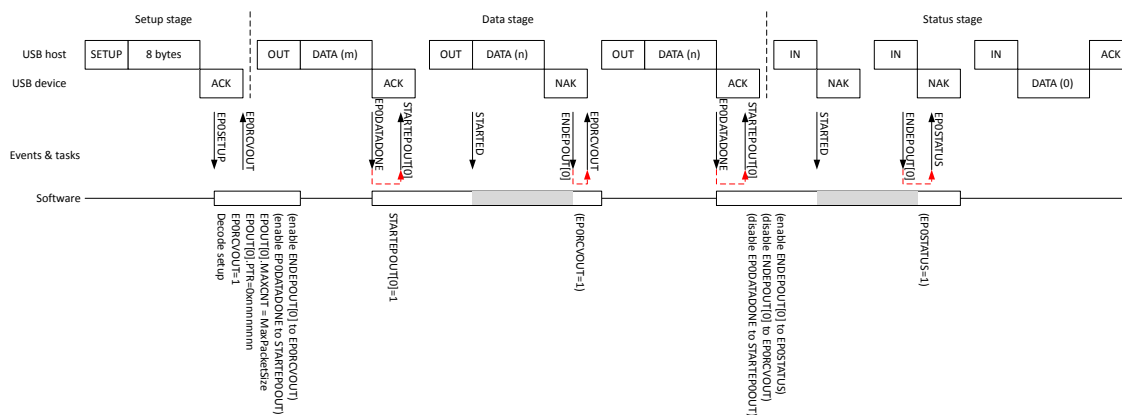


Figure 141: Control write transfer

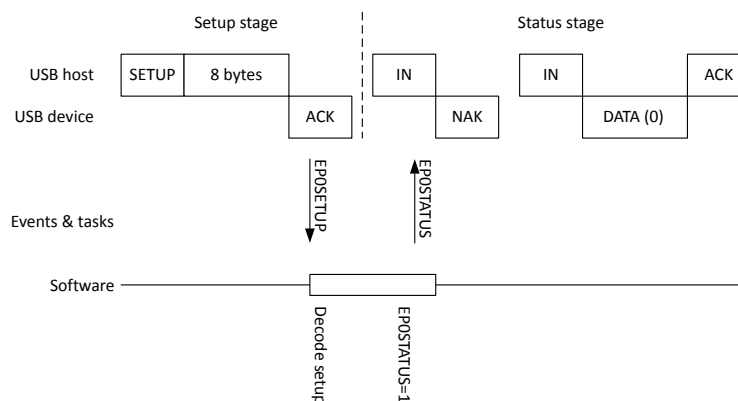


Figure 142: Control write no data transfer

## 6.26.10 Bulk and interrupt transactions

The USB peripheral implements seven pairs of bulk/interrupt endpoints.

The bulk/interrupt endpoints have a fixed USB endpoint number, summarized in the following table.

Bulk endpoint #	USB IN endpoint	USB OUT endpoint
[1]	0x81	0x01
[2]	0x82	0x02
[3]	0x83	0x03
[4]	0x84	0x04
[5]	0x85	0x05
[6]	0x86	0x06
[7]	0x87	0x07

Table 108: Bulk/interrupt endpoint numbering

A bulk/interrupt transaction consists of a single data stage. Two consecutive, successful transactions are distinguished through alternating leading process ID (PID): DATA0 follows DATA1, DATA1 follows DATA0, etc. A repeated transaction is detected by re-using the same PID as previous transaction, i.e. DATA0 follows DATA0, or DATA1 follows DATA1.

The USB controller automatically toggles DATA0/DATA1 PIDs for every bulk/interrupt transaction.

If incoming data is corrupted (CRC does not match), the USB controller automatically prevents DATA0/DATA1 from toggling, to request the host to resend the data.

In some specific cases, the software may want to force a data toggle (usually reset) on a specific IN endpoint, or force the expected toggle on an OUT endpoint, for instance as a consequence of the host issuing **ClearFeature**, **SetInterface**, or selecting an alternate setting. Controlling the data toggle of data IN or OUT endpoint  $n$  ( $n=1..7$ ) is done through register **DTOGGLE**.

The bulk/interrupt transaction in USB full-speed can be of any size up to 64 bytes. It must be a multiple of four bytes and 32-bit aligned in memory.

When the USB transaction has completed, an EPDATA event is generated. Until new data has been transferred by EasyDMA from memory to the USB peripheral (signalled by the ENDEPIN[ $n$ ] event), the hardware will automatically respond with NAK to all incoming IN tokens. Software has to configure and start the EasyDMA transfer once it is ready to send more data.

Each IN or OUT data endpoint has to be explicitly enabled by software through register **EPINEN** or **EPOUTEN**, according to the configuration declared by the device and selected by the host through the **SetConfig** command.

A disabled data endpoint will not respond to any traffic from the host. An enabled data endpoint will normally respond NAK or ACK (depending on the readiness of the buffers), or STALL (if configured in register **EPSTALL**), in which case the endpoint is asked to halt. The halted (or not) state of a given endpoint can be read back from register HALTED.EPIN[ $n$ ] or HALTED.EPOUT[ $n$ ]. The format of the returned 16-bit value can be copied as is, as a response to a **GetStatusEndpoint** request from the host.

Enabling or disabling an endpoint will not change its halted state. However, a USB reset will disable and clear the halted state of all data endpoints.

The control endpoint 0 IN and OUT can also be enabled and/or halted using the same mechanisms, but due to USB specification, receiving a SETUP will override its state.

### 6.26.10.1 Bulk and interrupt IN transaction

The host issues IN tokens to receive bulk/interrupt data. In order to send data, the software has to enable the endpoint and prepare an EasyDMA transfer on the desired endpoint.

Bulk/interrupt IN endpoints are enabled or disabled through their respective IN $n$  bit ( $n=1..7$ ) in **EPINEN** register.

It is also possible to stall or resume communication on an endpoint through the **EPSTALL** register.

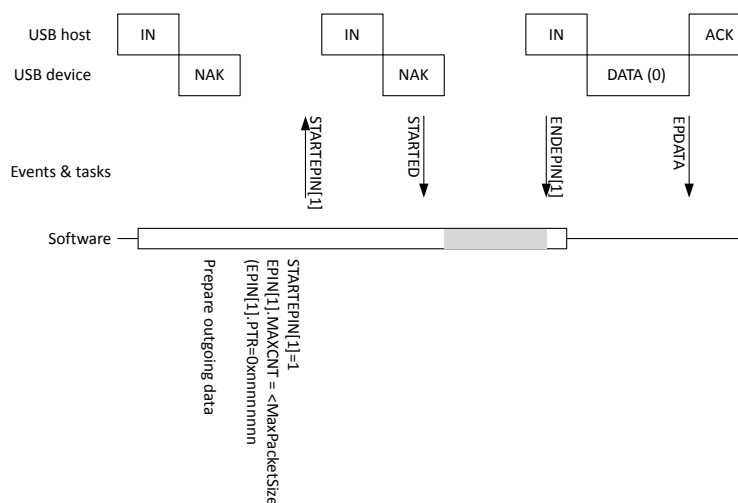


Figure 143: Bulk/interrupt IN transaction

It is possible (and in some situations it is required) to respond to an IN token with a zero-length data packet.

**Note:** On many USB hosts, not responding (DATA+ACK or NAK) to three IN tokens on an interrupt endpoint would have the host disable that endpoint as a consequence. Re-enumerating the device (unplug-replug) may be required to restore functionality. Make sure that the relevant data endpoints are enabled for normal operation as soon as the device gets configured through a **SetConfig** request.

### 6.26.10.2 Bulk and interrupt OUT transaction

When the host wants to transmit bulk/interrupt data, it issues an OUT token (packet) followed by a DATA packet on a given endpoint  $n$  ( $n=1..7$ ).

A NAK is returned until the software writes any value to register `SIZE.EPOUT[n]`, indicating that the content of the local buffer can be overwritten. Upon receiving the next OUT+DATA transaction, an ACK is returned to the host while an `EPDATA` event is generated (and the `EPDATASTATUS` register flags are set to indicate on which endpoint this happened). Once the EasyDMA is prepared and enabled, by writing the `EPOUT[n]` registers and triggering the `STARTEPOUT[n]` task, the incoming data will be transferred to memory. Until that transfer is finished, the hardware will automatically NAK any other incoming OUT+DATA packets. Only when the EasyDMA transfer is done (signalled by the `ENDEPOUT[n]` event), or as soon as any values are written by the software in register `SIZE.EPOUT[n]`, the endpoint  $n$  will accept incoming OUT+DATA again.

It is allowed for the host to send zero-length data packets.

Bulk/interrupt OUT endpoints are enabled or disabled through their respective `OUTn` bit ( $n=1..7$ ) in the `EPOUTEN` register. It is also possible to stall or resume communication on an endpoint through the `EPSTALL` register.

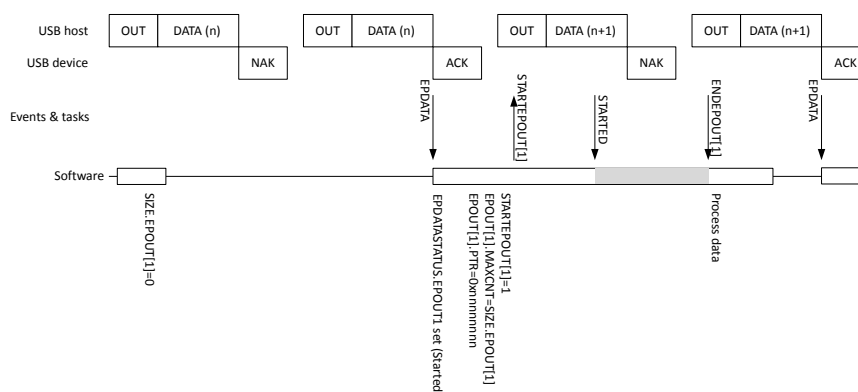


Figure 144: Bulk/interrupt OUT transaction

### 6.26.11 Isochronous transactions

The USB peripheral implements isochronous (ISO) endpoints.

The ISO endpoints have a fixed USB endpoint number, summarized in the following table.

ISO endpoint #	USB IN endpoint	USB OUT endpoint
[0]	0x88	0x08

Table 109: Isochronous endpoint numbering

An isochronous transaction consists of a single, non-acknowledged data stage. The host sends out a start of frame at a regular interval (1 ms), and data follows IN or OUT tokens within each frame.

EasyDMA allows transferring ISO data directly from and to memory. EasyDMA transfers must be initiated by the software, which can synchronize with the SOF (start of frame) events.

Because the timing of the start of frame is very accurate, the SOF event can be used for jobs such as synchronizing a local timer through the SOF event and PPI. The SOF event gets synchronized to the 16 MHz clock prior to being made available to the PPI.

Every start of frame increments a free-running counter, which can be read by software through the `FRAMECNTR` register.

Each IN or OUT ISO data endpoint has to be explicitly enabled by software through register `EPINEN` or `EPOUTEN`, according to the configuration declared by the device and selected by the host through the `SetConfig` command. A disabled ISO IN data endpoint will not respond to any traffic from the host. A disabled ISO OUT data endpoint will ignore any incoming traffic from the host.

The USB peripheral has an internal 1 kB buffer associated with ISO endpoints. The user can either allocate the full amount to the IN or the OUT endpoint, or split the buffer allocation between the two using register `ISOSPLIT`.

The internal buffer also sets the maximum size of the ISO OUT and ISO IN transfers: 1023 bytes when the full buffer is dedicated to either ISO OUT or ISO IN, and half when the buffer is split between the two.

### 6.26.11.1 Isochronous IN transaction

When the host wants to receive isochronous (ISO) data, it issues an IN token on the isochronous endpoint.

After the data has been transferred using the EasyDMA, the USB controller on the isochronous IN endpoint responds to the IN token with the transferred data using the `ISOIN.MAXCNT` for the size of the packet.

The ISO IN data endpoint has to be explicitly enabled by software through the `ISOIN0` bit in register `EPINEN`.

When an ISO IN endpoint is enabled and no data transferred with EasyDMA, the response of the USB peripheral depends on the setting of the `RESPONSE` field in register `ISOINCONFIG`. It can either provide no response to an IN token or respond with a zero-length data.

If the EasyDMA transfer on the isochronous endpoint is not completed before the next SOF event, the result of the transfer is undefined.

The maximum size of an ISO IN transfer in USB full-speed is 1023 bytes. The data buffer has to be a multiple of 4 bytes 32-bit aligned in memory. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 bytes, if not shared with an OUT ISO endpoint).

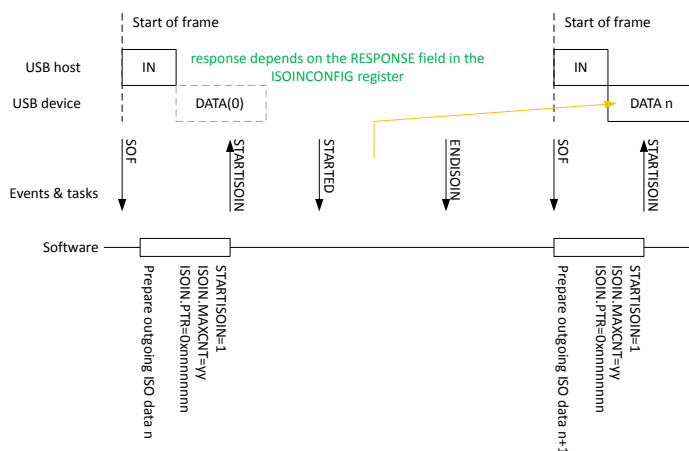


Figure 145: Isochronous IN transfer

### 6.26.11.2 Isochronous OUT transaction

When the host wants to send isochronous (ISO) data, it issues an OUT token on the isochronous endpoint, followed by data.

The ISO OUT data endpoint has to be explicitly enabled by software through the ISOOUT0 bit in register **EPOUTEN**.

The amount of last received ISO OUT data is provided in the **SIZE.ISOOUT** register. Software shall interpret the ZERO and SIZE fields as presented in the following table.

ZERO	SIZE	Last received data size
Normal	0	No data received at all
Normal	1..1023	1..1023 bytes of data received
ZeroData	(not of interest)	Zero-length data packet received

Table 110: ISO OUT incoming data size

When EasyDMA is prepared and started, triggering a STARTISOOUT task initiates an EasyDMA transfer to memory. Software shall synchronize ISO OUT transfers with the SOF events. EasyDMA uses the address in **ISOOUT.PTR** and size in **ISOOUT.MAXCNT** for every new transfer.

If the EasyDMA transfer on the isochronous endpoint is not completed before the next SOF event, the result of the transfer is undefined.

The maximum size of an isochronous OUT transfer in USB full-speed is 1023 bytes. The data buffer has to be a multiple of 4 bytes and 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 bytes if not shared with an IN ISO endpoint).

If the last received ISO data packet is corrupted (wrong CRC), the USB controller generates an USBEVENT event (at the same time as SOF) and indicates a CRC error on ISOOUTCRC in register **EVENTCAUSE**. EasyDMA will transfer the data anyway if it has been set up properly.

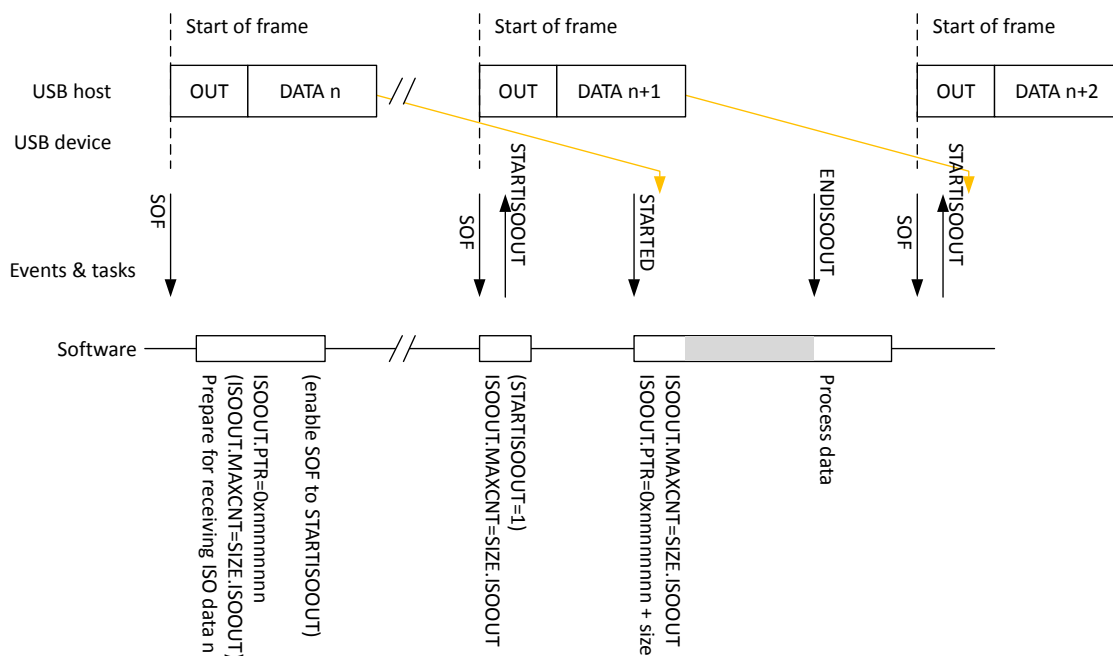


Figure 146: Isochronous OUT transfer



## 6.26.12 USB register access limitations

Some of the registers in USBD cannot be accessed in specific conditions.

This may be the case when USBD is not enabled (using the **ENABLE** register) and ready (signalled by the **READY** bit in **EVENTCAUSE** after a **USBEVENT** event), or when USBD is in low power mode while the USB bus is suspended.

Triggering any tasks, including the tasks triggered through the PPI, is affected by this behavior. In addition, the following registers are affected:

- HALTED.EPIN[0..7]
- HALTED.EPOUT[0..7]
- USBADDR
- BMREQUESTTYPE
- BREQUEST
- WVALUEL
- WVALUEH
- WINDEXL
- WINDEXH
- WLENGTHL
- WLENGTHH
- SIZE.EPOUT[0..7]
- SIZE.ISOOUT
- USBPULLUP
- DTOGGLE
- EPINEN
- EPOUTEN
- EPSTALL
- ISOSPLIT
- FRAMECNTR

## 6.26.13 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40027000	USB	USB	Universal serial bus device	

Table 111: Instances

Register	Offset	Description
TASKS_STARTEPIN[0]	0x004	Captures the EPIN[0].PTR and EPIN[0].MAXCNT registers values, and enables endpoint IN 0 to respond to traffic from host
TASKS_STARTEPIN[1]	0x008	Captures the EPIN[1].PTR and EPIN[1].MAXCNT registers values, and enables endpoint IN 1 to respond to traffic from host
TASKS_STARTEPIN[2]	0x00C	Captures the EPIN[2].PTR and EPIN[2].MAXCNT registers values, and enables endpoint IN 2 to respond to traffic from host
TASKS_STARTEPIN[3]	0x010	Captures the EPIN[3].PTR and EPIN[3].MAXCNT registers values, and enables endpoint IN 3 to respond to traffic from host
TASKS_STARTEPIN[4]	0x014	Captures the EPIN[4].PTR and EPIN[4].MAXCNT registers values, and enables endpoint IN 4 to respond to traffic from host
TASKS_STARTEPIN[5]	0x018	Captures the EPIN[5].PTR and EPIN[5].MAXCNT registers values, and enables endpoint IN 5 to respond to traffic from host

Register	Offset	Description
TASKS_STARTEPIN[6]	0x01C	Captures the EPIN[6].PTR and EPIN[6].MAXCNT registers values, and enables endpoint IN 6 to respond to traffic from host
TASKS_STARTEPIN[7]	0x020	Captures the EPIN[7].PTR and EPIN[7].MAXCNT registers values, and enables endpoint IN 7 to respond to traffic from host
TASKS_STARTISOIN	0x024	Captures the ISOIN.PTR and ISOIN.MAXCNT registers values, and enables sending data on ISO endpoint
TASKS_STARTEPOUT[0]	0x028	Captures the EPOUT[0].PTR and EPOUT[0].MAXCNT registers values, and enables endpoint 0 to respond to traffic from host
TASKS_STARTEPOUT[1]	0x02C	Captures the EPOUT[1].PTR and EPOUT[1].MAXCNT registers values, and enables endpoint 1 to respond to traffic from host
TASKS_STARTEPOUT[2]	0x030	Captures the EPOUT[2].PTR and EPOUT[2].MAXCNT registers values, and enables endpoint 2 to respond to traffic from host
TASKS_STARTEPOUT[3]	0x034	Captures the EPOUT[3].PTR and EPOUT[3].MAXCNT registers values, and enables endpoint 3 to respond to traffic from host
TASKS_STARTEPOUT[4]	0x038	Captures the EPOUT[4].PTR and EPOUT[4].MAXCNT registers values, and enables endpoint 4 to respond to traffic from host
TASKS_STARTEPOUT[5]	0x03C	Captures the EPOUT[5].PTR and EPOUT[5].MAXCNT registers values, and enables endpoint 5 to respond to traffic from host
TASKS_STARTEPOUT[6]	0x040	Captures the EPOUT[6].PTR and EPOUT[6].MAXCNT registers values, and enables endpoint 6 to respond to traffic from host
TASKS_STARTEPOUT[7]	0x044	Captures the EPOUT[7].PTR and EPOUT[7].MAXCNT registers values, and enables endpoint 7 to respond to traffic from host
TASKS_STARTISOOUT	0x048	Captures the ISOOUT.PTR and ISOOUT.MAXCNT registers values, and enables receiving of data on ISO endpoint
TASKS_EPORCVOUT	0x04C	Allows OUT data stage on control endpoint 0
TASKS_EPOSTATUS	0x050	Allows status stage on control endpoint 0
TASKS_EPOSTALL	0x054	Stalls data and status stage on control endpoint 0
TASKS_DPDMDRIVE	0x058	Forces D+ and D- lines into the state defined in the DPDMVALUE register
TASKS_DPDMNODRIVE	0x05C	Stops forcing D+ and D- lines into any state (USB engine takes control)
EVENTS_USBRESET	0x100	Signals that a USB reset condition has been detected on USB lines
EVENTS_STARTED	0x104	Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register
EVENTS_ENDEPIN[0]	0x108	The whole EPIN[0] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[1]	0x10C	The whole EPIN[1] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[2]	0x110	The whole EPIN[2] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[3]	0x114	The whole EPIN[3] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[4]	0x118	The whole EPIN[4] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[5]	0x11C	The whole EPIN[5] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[6]	0x120	The whole EPIN[6] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPIN[7]	0x124	The whole EPIN[7] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_EPODATADONE	0x128	An acknowledged data transfer has taken place on the control endpoint
EVENTS_ENDISOIN	0x12C	The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[0]	0x130	The whole EPOUT[0] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[1]	0x134	The whole EPOUT[1] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[2]	0x138	The whole EPOUT[2] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[3]	0x13C	The whole EPOUT[3] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[4]	0x140	The whole EPOUT[4] buffer has been consumed. The buffer can be accessed safely by software.

Register	Offset	Description
EVENTS_ENDEPOUT[5]	0x144	The whole EPOUT[5] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[6]	0x148	The whole EPOUT[6] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDEPOUT[7]	0x14C	The whole EPOUT[7] buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_ENDISOOUT	0x150	The whole ISOOUT buffer has been consumed. The buffer can be accessed safely by software.
EVENTS_SOF	0x154	Signals that a SOF (start of frame) condition has been detected on USB lines
EVENTS_USBEVENT	0x158	An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause.
EVENTS_EPOSETUP	0x15C	A valid SETUP token has been received (and acknowledged) on the control endpoint
EVENTS_EPDATA	0x160	A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register
SHORTS	0x200	Shortcuts between local events and tasks
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVENTCAUSE	0x400	Details on what caused the USBEVENT event
HALTED.EPIN[0]	0x420	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[1]	0x424	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[2]	0x428	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[3]	0x42C	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[4]	0x430	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[5]	0x434	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[6]	0x438	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPIN[7]	0x43C	IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[0]	0x444	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[1]	0x448	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[2]	0x44C	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[3]	0x450	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[4]	0x454	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[5]	0x458	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[6]	0x45C	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
HALTED.EPOUT[7]	0x460	OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.
EPSTATUS	0x468	Provides information on which endpoint's EasyDMA registers have been captured
EPDATASTATUS	0x46C	Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)
USBADDR	0x470	Device USB address
BMREQUESTTYPE	0x480	SETUP data, byte 0, bmRequestType
BREQUEST	0x484	SETUP data, byte 1, bRequest
WVALUEL	0x488	SETUP data, byte 2, LSB of wValue
WVALUEH	0x48C	SETUP data, byte 3, MSB of wValue
WINDEXL	0x490	SETUP data, byte 4, LSB of wIndex
WINDEXH	0x494	SETUP data, byte 5, MSB of wIndex
WLENGTHL	0x498	SETUP data, byte 6, LSB of wLength
WLENGTHH	0x49C	SETUP data, byte 7, MSB of wLength

Register	Offset	Description
SIZE.EPOUT[0]	0x4A0	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[1]	0x4A4	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[2]	0x4A8	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[3]	0x4AC	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[4]	0x4B0	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[5]	0x4B4	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[6]	0x4B8	Number of bytes received last in the data stage of this OUT endpoint
SIZE.EPOUT[7]	0x4BC	Number of bytes received last in the data stage of this OUT endpoint
SIZE.ISOOUT	0x4C0	Number of bytes received last on this ISO OUT data endpoint
ENABLE	0x500	Enable USB
USBPULLUP	0x504	Control of the USB pull-up
DPDMVALUE	0x508	State D+ and D- lines will be forced into by the DPDMDRIVE task. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing).
DTOGGLE	0x50C	Data toggle control and status
EPINEN	0x510	Endpoint IN enable
EPOUTEN	0x514	Endpoint OUT enable
EPSTALL	0x518	STALL endpoints
ISOSPLIT	0x51C	Controls the split of ISO buffers
FRAMECNTR	0x520	Returns the current value of the start of frame counter
LOWPOWER	0x52C	Controls USB peripheral low power mode during USB suspend
ISOINCONFIG	0x530	Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent
EPIN[0].PTR	0x600	Data pointer
EPIN[0].MAXCNT	0x604	Maximum number of bytes to transfer
EPIN[0].AMOUNT	0x608	Number of bytes transferred in the last transaction
EPIN[1].PTR	0x614	Data pointer
EPIN[1].MAXCNT	0x618	Maximum number of bytes to transfer
EPIN[1].AMOUNT	0x61C	Number of bytes transferred in the last transaction
EPIN[2].PTR	0x628	Data pointer
EPIN[2].MAXCNT	0x62C	Maximum number of bytes to transfer
EPIN[2].AMOUNT	0x630	Number of bytes transferred in the last transaction
EPIN[3].PTR	0x63C	Data pointer
EPIN[3].MAXCNT	0x640	Maximum number of bytes to transfer
EPIN[3].AMOUNT	0x644	Number of bytes transferred in the last transaction
EPIN[4].PTR	0x650	Data pointer
EPIN[4].MAXCNT	0x654	Maximum number of bytes to transfer
EPIN[4].AMOUNT	0x658	Number of bytes transferred in the last transaction
EPIN[5].PTR	0x664	Data pointer
EPIN[5].MAXCNT	0x668	Maximum number of bytes to transfer
EPIN[5].AMOUNT	0x66C	Number of bytes transferred in the last transaction
EPIN[6].PTR	0x678	Data pointer
EPIN[6].MAXCNT	0x67C	Maximum number of bytes to transfer
EPIN[6].AMOUNT	0x680	Number of bytes transferred in the last transaction
EPIN[7].PTR	0x68C	Data pointer
EPIN[7].MAXCNT	0x690	Maximum number of bytes to transfer
EPIN[7].AMOUNT	0x694	Number of bytes transferred in the last transaction
ISOIN.PTR	0x6A0	Data pointer
ISOIN.MAXCNT	0x6A4	Maximum number of bytes to transfer
ISOIN.AMOUNT	0x6A8	Number of bytes transferred in the last transaction
EPOUT[0].PTR	0x700	Data pointer
EPOUT[0].MAXCNT	0x704	Maximum number of bytes to transfer
EPOUT[0].AMOUNT	0x708	Number of bytes transferred in the last transaction
EPOUT[1].PTR	0x714	Data pointer
EPOUT[1].MAXCNT	0x718	Maximum number of bytes to transfer

Register	Offset	Description
EPOUT[1].AMOUNT	0x71C	Number of bytes transferred in the last transaction
EPOUT[2].PTR	0x728	Data pointer
EPOUT[2].MAXCNT	0x72C	Maximum number of bytes to transfer
EPOUT[2].AMOUNT	0x730	Number of bytes transferred in the last transaction
EPOUT[3].PTR	0x73C	Data pointer
EPOUT[3].MAXCNT	0x740	Maximum number of bytes to transfer
EPOUT[3].AMOUNT	0x744	Number of bytes transferred in the last transaction
EPOUT[4].PTR	0x750	Data pointer
EPOUT[4].MAXCNT	0x754	Maximum number of bytes to transfer
EPOUT[4].AMOUNT	0x758	Number of bytes transferred in the last transaction
EPOUT[5].PTR	0x764	Data pointer
EPOUT[5].MAXCNT	0x768	Maximum number of bytes to transfer
EPOUT[5].AMOUNT	0x76C	Number of bytes transferred in the last transaction
EPOUT[6].PTR	0x778	Data pointer
EPOUT[6].MAXCNT	0x77C	Maximum number of bytes to transfer
EPOUT[6].AMOUNT	0x780	Number of bytes transferred in the last transaction
EPOUT[7].PTR	0x78C	Data pointer
EPOUT[7].MAXCNT	0x790	Maximum number of bytes to transfer
EPOUT[7].AMOUNT	0x794	Number of bytes transferred in the last transaction
ISOOUT.PTR	0x7A0	Data pointer
ISOOUT.MAXCNT	0x7A4	Maximum number of bytes to transfer
ISOOUT.AMOUNT	0x7A8	Number of bytes transferred in the last transaction

Table 112: Register overview

### 6.26.13.1 TASKS\_STARTEPIN[n] (n=0..7)

Address offset:  $0x004 + (n \times 0x4)$

Captures the EPIN[n].PTR and EPIN[n].MAXCNT registers values, and enables endpoint IN n to respond to traffic from host

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce	Field	Value ID	Value	Description																										
A	W	TASKS_STARTEPIN			Captures the EPIN[n].PTR and EPIN[n].MAXCNT registers values, and enables endpoint IN n to respond to traffic from host																										
			Trigger	1	Trigger task																										

### 6.26.13.2 TASKS\_STARTISOIN

Address offset: 0x024

Captures the ISOIN.PTR and ISOIN.MAXCNT registers values, and enables sending data on ISO endpoint

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STARTISOIN			Captures the ISOIN.PTR and ISOIN.MAXCNT registers values, and enables sending data on ISO endpoint																											
			Trigger	1	Trigger task																											

### 6.26.13.3 TASKS\_STARTEPOUT[n] (n=0..7)

Address offset: 0x028 + (n × 0x4)

Captures the EPOUT[n].PTR and EPOUT[n].MAXCNT registers values, and enables endpoint n to respond to traffic from host

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STARTEPOUT			Captures the EPOUT[n].PTR and EPOUT[n].MAXCNT registers values, and enables endpoint n to respond to traffic from host																											
			Trigger	1	Trigger task																											

### 6.26.13.4 TASKS\_STARTISOOUT

Address offset: 0x048

Captures the ISOOUT.PTR and ISOOUT.MAXCNT registers values, and enables receiving of data on ISO endpoint

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_STARTISOOUT			Captures the ISOOUT.PTR and ISOOUT.MAXCNT registers values, and enables receiving of data on ISO endpoint																											
			Trigger	1	Trigger task																											

### 6.26.13.5 TASKS\_EP0RCVOUT

Address offset: 0x04C

Allows OUT data stage on control endpoint 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce	Field	Value ID	Value	Description																											
A	W	TASKS_EP0RCVOUT			Allows OUT data stage on control endpoint 0																											
			Trigger	1	Trigger task																											

### 6.26.13.6 TASKS\_EPOSTATUS

Address offset: 0x050

Allows status stage on control endpoint 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_EPOSTATUS			Allows status stage on control endpoint 0																												
		Trigger	1	Trigger task																												

### 6.26.13.7 TASKS\_EPOSTALL

Address offset: 0x054

Stalls data and status stage on control endpoint 0

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_EPOSTALL			Stalls data and status stage on control endpoint 0																												
		Trigger	1	Trigger task																												

### 6.26.13.8 TASKS\_DPDMDRIVE

Address offset: 0x058

Forces D+ and D- lines into the state defined in the DPDMVALUE register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_DPDMDRIVE			Forces D+ and D- lines into the state defined in the DPDMVALUE register																												
		Trigger	1	Trigger task																												

### 6.26.13.9 TASKS\_DPDMNODRIVE

Address offset: 0x05C

Stops forcing D+ and D- lines into any state (USB engine takes control)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_DPDMNODRIVE			Stops forcing D+ and D- lines into any state (USB engine takes control)																												
		Trigger	1	Trigger task																												

### 6.26.13.10 EVENTS\_USBRESET

Address offset: 0x100

Signals that a USB reset condition has been detected on USB lines

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_USBRESET		Signals that a USB reset condition has been detected on USB lines																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.11 EVENTS\_STARTED

Address offset: 0x104

Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_STARTED		Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.12 EVENTS\_ENDEPIN[n] (n=0..7)

Address offset: 0x108 + (n × 0x4)

The whole EPIN[n] buffer has been consumed. The buffer can be accessed safely by software.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDEPIN		The whole EPIN[n] buffer has been consumed. The buffer can be accessed safely by software.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.13 EVENTS\_EPODATADONE

Address offset: 0x128

An acknowledged data transfer has taken place on the control endpoint



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_EPODATADONE		An acknowledged data transfer has taken place on the control endpoint																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.14 EVENTS\_ENDISOIN

Address offset: 0x12C

The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDISOIN		The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.15 EVENTS\_ENDEPOUT[n] (n=0..7)

Address offset: 0x130 + (n × 0x4)

The whole EPOUT[n] buffer has been consumed. The buffer can be accessed safely by software.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDEPOUT		The whole EPOUT[n] buffer has been consumed. The buffer can be accessed safely by software.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.16 EVENTS\_ENDISOOUT

Address offset: 0x150

The whole ISOOUT buffer has been consumed. The buffer can be accessed safely by software.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
Reset	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	EVENTS_ENDISOOUT		The whole ISOOUT buffer has been consumed. The buffer can be accessed safely by software.																											
		NotGenerated	0	Event not generated																											
		Generated	1	Event generated																											

### 6.26.13.17 EVENTS\_SOF

Address offset: 0x154

Signals that a SOF (start of frame) condition has been detected on USB lines

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_SOF		Signals that a SOF (start of frame) condition has been detected on USB lines																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.26.13.18 EVENTS\_USBEVENT

Address offset: 0x158

An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_USBEVENT		An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause.																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.26.13.19 EVENTS\_EPOSETUP

Address offset: 0x15C

A valid SETUP token has been received (and acknowledged) on the control endpoint

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_EPOSETUP		A valid SETUP token has been received (and acknowledged) on the control endpoint																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.26.13.20 EVENTS\_EPDATA

Address offset: 0x160

A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																												
A	RW	EVENTS_EPDATA		A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.26.13.21 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
ID																																E	D	C	B	A
Reset	0x00000000																																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
ID	Acce Field	Value ID	Value	Description																																
A	RW	EPODATADONE_STARTEPIN0		Shortcut between event <a href="#">EPODATADONE</a> and task <a href="#">STARTEPIN[0]</a>																																
		Disabled	0	Disable shortcut																																
		Enabled	1	Enable shortcut																																
B	RW	EPODATADONE_STARTEP		Shortcut between event <a href="#">EPODATADONE</a> and task <a href="#">STARTEP[0]</a>																																
		Disabled	0	Disable shortcut																																
		Enabled	1	Enable shortcut																																
C	RW	EPODATADONE_EPOSTATUS		Shortcut between event <a href="#">EPODATADONE</a> and task <a href="#">EPOSTATUS</a>																																
		Disabled	0	Disable shortcut																																
		Enabled	1	Enable shortcut																																
D	RW	ENDEPOUTO_EPOSTATUS		Shortcut between event <a href="#">ENDEPOUTO[0]</a> and task <a href="#">EPOSTATUS</a>																																
		Disabled	0	Disable shortcut																																
		Enabled	1	Enable shortcut																																
E	RW	ENDEPOUTO_EPORCVOUT		Shortcut between event <a href="#">ENDEPOUTO[0]</a> and task <a href="#">EPORCVOUT</a>																																
		Disabled	0	Disable shortcut																																
		Enabled	1	Enable shortcut																																

### 6.26.13.22 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																																Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset	0x00000000																																																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																									
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	USBRESET		Enable or disable interrupt for event <a href="#">USBRESET</a>																																																				
		Disabled	0	Disable																																																				
		Enabled	1	Enable																																																				
B	RW	STARTED		Enable or disable interrupt for event <a href="#">STARTED</a>																																																				
		Disabled	0	Disable																																																				
		Enabled	1	Enable																																																				
C-J	RW	ENDEPIN[i] (i=0..7)		Enable or disable interrupt for event <a href="#">ENDEPIN[i]</a>																																																				
		Disabled	0	Disable																																																				

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	Y X W V U T S R Q P O N M L K J I H G F E D C B A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
		Enabled	1	Enable																											
K	RW EP0DATADONE	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">EP0DATADONE</a>																											
L	RW ENDISOIN	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">ENDISOIN</a>																											
M-T	RW ENDEPOUT[i] (i=0..7)	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">ENDEPOUT[i]</a>																											
U	RW ENDISOOUT	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">ENDISOOUT</a>																											
V	RW SOF	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">SOF</a>																											
W	RW USBEVENT	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">USBEVENT</a>																											
X	RW EPOSETUP	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">EPOSETUP</a>																											
Y	RW EPDATA	Disabled	0	Disable																											
		Enabled	1	Enable																											
				Enable or disable interrupt for event <a href="#">EPDATA</a>																											

### 6.26.13.23 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	Y X W V U T S R Q P O N M L K J I H G F E D C B A																														
Reset 0x00000000	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW USBRESET	Set	1	Write '1' to enable interrupt for event <a href="#">USBRESET</a>																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
B	RW STARTED	Set	1	Write '1' to enable interrupt for event <a href="#">STARTED</a>																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
C-J	RW ENDEPIN[i] (i=0..7)	Set	1	Write '1' to enable interrupt for event <a href="#">ENDEPIN[i]</a>																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											
K	RW EP0DATADONE	Set	1	Write '1' to enable interrupt for event <a href="#">EP0DATADONE</a>																											
				Enable																											

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		Y X W V U T S R Q P O N M L K J I H G F E D C B A																											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
L	RW ENDISOIN			Write '1' to enable interrupt for event <a href="#">ENDISOIN</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
M-T	RW ENDEPOUT[i] (i=0..7)			Write '1' to enable interrupt for event <a href="#">ENDEPOUT[i]</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
U	RW ENDISOOUT			Write '1' to enable interrupt for event <a href="#">ENDISOOUT</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
V	RW SOF			Write '1' to enable interrupt for event <a href="#">SOF</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
W	RW USBEVENT			Write '1' to enable interrupt for event <a href="#">USBEVENT</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
X	RW EPOSETUP			Write '1' to enable interrupt for event <a href="#">EPOSETUP</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
Y	RW EPDATA			Write '1' to enable interrupt for event <a href="#">EPDATA</a>																									
		Set	1	Enable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									

### 6.26.13.24 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																											
ID		Y X W V U T S R Q P O N M L K J I H G F E D C B A																											
Reset 0x00000000		0 0																											
ID	Acce Field	Value ID	Value	Description																									
A	RW USBRESET			Write '1' to disable interrupt for event <a href="#">USBRESET</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
B	RW STARTED			Write '1' to disable interrupt for event <a href="#">STARTED</a>																									
		Clear	1	Disable																									
		Disabled	0	Read: Disabled																									
		Enabled	1	Read: Enabled																									
C-J	RW ENDEPIN[i] (i=0..7)			Write '1' to disable interrupt for event <a href="#">ENDEPIN[i]</a>																									

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID		Y X W V U T S R Q P O N M L K J I H G F E D C B A																														
Reset 0x00000000		0 0																														
ID	Acce Field	Value ID	Value	Description																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
K	RW EPODATADONE			Write '1' to disable interrupt for event <a href="#">EPODATADONE</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
L	RW ENDISOIN			Write '1' to disable interrupt for event <a href="#">ENDISOIN</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
M-T	RW ENDEPOUT[i] (i=0..7)			Write '1' to disable interrupt for event <a href="#">ENDEPOUT[i]</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
U	RW ENDISOOUT			Write '1' to disable interrupt for event <a href="#">ENDISOOUT</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
V	RW SOF			Write '1' to disable interrupt for event <a href="#">SOF</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
W	RW USBEVENT			Write '1' to disable interrupt for event <a href="#">USBEVENT</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
X	RW EPOSETUP			Write '1' to disable interrupt for event <a href="#">EPOSETUP</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												
Y	RW EPDATA			Write '1' to disable interrupt for event <a href="#">EPDATA</a>																												
		Clear	1	Disable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.26.13.25 EVENTCAUSE

Address offset: 0x400

Details on what caused the USBEVENT event

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID		E D C B A																														
Reset 0x00000000		0 0																														
ID	Acce Field	Value ID	Value	Description																												
A	RW ISOOUTCRC			CRC error was detected on isochronous OUT endpoint 8.																												
				Write '1' to clear.																												
		NotDetected	0	No error detected																												
		Detected	1	Error detected																												

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																													E	D	C	B				A
<b>Reset 0x00000000</b>	<b>0 0</b>																																			
ID	Acce Field	Value ID	Value	Description																																
B	RW SUSPEND			Signals that USB lines have been idle long enough for the device to enter suspend. Write '1' to clear.																																
		NotDetected	0	Suspend not detected																																
		Detected	1	Suspend detected																																
C	RW RESUME			Signals that a RESUME condition (K state or activity restart) has been detected on USB lines. Write '1' to clear.																																
		NotDetected	0	Resume not detected																																
		Detected	1	Resume detected																																
D	RW USBWUALLOWED			USB MAC has been woken up and operational. Write '1' to clear.																																
		NotAllowed	0	Wake up not allowed																																
		Allowed	1	Wake up allowed																																
E	RW READY			USB device is ready for normal operation. Write '1' to clear.																																
		NotDetected	0	USBEVENT was not issued due to USB peripheral ready																																
		Ready	1	USB peripheral is ready																																

### 6.26.13.26 HALTED.EPIN[n] (n=0..7)

Address offset:  $0x420 + (n \times 0x4)$

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																								
ID																													A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																																								
ID	Acce Field	Value ID	Value	Description																																																					
A	R GETSTATUS			IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.																																																					
		NotHalted	0	Endpoint is not halted																																																					
		Halted	1	Endpoint is halted																																																					

### 6.26.13.27 HALTED.EPOUT[n] (n=0..7)

Address offset:  $0x444 + (n \times 0x4)$

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																								
ID																													A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	<b>0 0</b>																																																								
ID	Acce Field	Value ID	Value	Description																																																					
A	R GETSTATUS			OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.																																																					
		NotHalted	0	Endpoint is not halted																																																					
		Halted	1	Endpoint is halted																																																					

### 6.26.13.28 EPSTATUS

Address offset: 0x468

Provides information on which endpoint's EasyDMA registers have been captured

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	R Q P O N M L K J															I H G F E D C B A																
<b>Reset 0x00000000</b>		<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																												
A-I	RW EPIN[i] (i=0..8)			Captured state of endpoint's EasyDMA registers. Write '1' to clear.																												
		NoData	0	EasyDMA registers have not been captured for this endpoint																												
		DataDone	1	EasyDMA registers have been captured for this endpoint																												
J-R	RW EPOUT[i] (i=0..8)			Captured state of endpoint's EasyDMA registers. Write '1' to clear.																												
		NoData	0	EasyDMA registers have not been captured for this endpoint																												
		DataDone	1	EasyDMA registers have been captured for this endpoint																												

### 6.26.13.29 EPDATASTATUS

Address offset: 0x46C

Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID	N M L K J I H															G F E D C B A																
<b>Reset 0x00000000</b>		<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																												
A-G	RW EPIN[i] (i=1..7)			Acknowledged data transfer on this IN endpoint. Write '1' to clear.																												
		NotDone	0	No acknowledged data transfer on this endpoint																												
		DataDone	1	Acknowledged data transfer on this endpoint has occurred																												
H-N	RW EPOUT[i] (i=1..7)			Acknowledged data transfer on this OUT endpoint. Write '1' to clear.																												
		NotStarted	0	No acknowledged data transfer on this endpoint																												
		Started	1	Acknowledged data transfer on this endpoint has occurred																												

### 6.26.13.30 USBADDR

Address offset: 0x470

Device USB address

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																	A A A A A A A															
<b>Reset 0x00000000</b>		<b>0 0</b>																														
ID	Acce Field	Value ID	Value	Description																												
A	R ADDR			Device USB address																												

### 6.26.13.31 BMREQUESTTYPE

Address offset: 0x480

SETUP data, byte 0, bmRequestType



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																														
ID																															C	B	B	A	A	A	A										
<b>Reset 0x00000000</b>	<b>0 0</b>																																														
ID	Acce	Field	Value ID	Value	Description																																										
A	R	RECIPIENT			Data transfer type																																										
			Device	0	Device																																										
			Interface	1	Interface																																										
			Endpoint	2	Endpoint																																										
			Other	3	Other																																										
B	R	TYPE			Data transfer type																																										
			Standard	0	Standard																																										
			Class	1	Class																																										
			Vendor	2	Vendor																																										
C	R	DIRECTION			Data transfer direction																																										
			HostToDevice	0	Host-to-device																																										
			DeviceToHost	1	Device-to-host																																										

### 6.26.13.32 BREQUEST

Address offset: 0x484

SETUP data, byte 1, bRequest

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																													
ID																															A	A	A	A	A	A										
<b>Reset 0x00000000</b>	<b>0 0</b>																																													
ID	Acce	Field	Value ID	Value	Description																																									
A	R	BREQUEST			SETUP data, byte 1, bRequest. Values provided for standard requests only, user must implement class and vendor values.																																									
			STD_GET_STATUS	0	Standard request GET_STATUS																																									
			STD_CLEAR_FEATURE	1	Standard request CLEAR_FEATURE																																									
			STD_SET_FEATURE	3	Standard request SET_FEATURE																																									
			STD_SET_ADDRESS	5	Standard request SET_ADDRESS																																									
			STD_GET_DESCRIPTOR	6	Standard request GET_DESCRIPTOR																																									
			STD_SET_DESCRIPTOR	7	Standard request SET_DESCRIPTOR																																									
			STD_GET_CONFIGURATION	8	Standard request GET_CONFIGURATION																																									
			STD_SET_CONFIGURATION	9	Standard request SET_CONFIGURATION																																									
			STD_GET_INTERFACE	10	Standard request GET_INTERFACE																																									
			STD_SET_INTERFACE	11	Standard request SET_INTERFACE																																									
			STD_SYNCH_FRAME	12	Standard request SYNCH_FRAME																																									

### 6.26.13.33 WVALUEL

Address offset: 0x488

SETUP data, byte 2, LSB of wValue

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																													
ID																															A	A	A	A	A	A										
<b>Reset 0x00000000</b>	<b>0 0</b>																																													
ID	Acce	Field	Value ID	Value	Description																																									
A	R	WVALUEL			SETUP data, byte 2, LSB of wValue																																									

### 6.26.13.34 WVALUEH

Address offset: 0x48C

SETUP data, byte 3, MSB of wValue

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	WVALUEH		SETUP data, byte 3, MSB of wValue																												

### 6.26.13.35 WINDEXL

Address offset: 0x490

SETUP data, byte 4, LSB of wIndex

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	WINDEXL		SETUP data, byte 4, LSB of wIndex																												

### 6.26.13.36 WINDEXH

Address offset: 0x494

SETUP data, byte 5, MSB of wIndex

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	WINDEXH		SETUP data, byte 5, MSB of wIndex																												

### 6.26.13.37 WLENGTHL

Address offset: 0x498

SETUP data, byte 6, LSB of wLength

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A A A A A A A A																															
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	R	WLENGTHL		SETUP data, byte 6, LSB of wLength																												

### 6.26.13.38 WLENGTHH

Address offset: 0x49C

SETUP data, byte 7, MSB of wLength

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																											A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0																										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																				
A	R	WLENGTHH		SETUP data, byte 7, MSB of wLength																																																				

### 6.26.13.39 SIZE.EPOUT[n] (n=0..7)

Address offset: 0x4A0 + (n × 0x4)

Number of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																											A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00000000</b>	0																										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	SIZE		Number of bytes received last in the data stage of this OUT endpoint																																																				

### 6.26.13.40 SIZE.ISOOUT

Address offset: 0x4C0

Number of bytes received last on this ISO OUT data endpoint

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0											
ID														B														A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
<b>Reset 0x00010000</b>	0													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																							
A	R	SIZE		Number of bytes received last on this ISO OUT data endpoint																																							
B	R	ZERO		Zero-length data packet received																																							
		Normal	0	No zero-length data received, use value in SIZE																																							
		ZeroData	1	Zero-length data received, ignore value in SIZE																																							

### 6.26.13.41 ENABLE

Address offset: 0x500

Enable USB

After writing Disabled to this register, reading the register will return Enabled until USB is completely disabled.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																								
ID																											A																													
<b>Reset 0x00000000</b>	0																										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce Field	Value ID	Value	Description																																																				
A	RW	ENABLE		Enable USB																																																				
		Disabled	0	USB peripheral is disabled																																																				
		Enabled	1	USB peripheral is enabled																																																				

### 6.26.13.42 USBPULLUP

Address offset: 0x504

Control of the USB pull-up

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW CONNECT			Control of the USB pull-up on the D+ line																												
		Disabled	0	Pull-up is disconnected																												
		Enabled	1	Pull-up is connected to D+																												

### 6.26.13.43 DPDMVALUE

Address offset: 0x508

State D+ and D- lines will be forced into by the DPDMDRIVE task. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing).

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A A A A A
<b>Reset 0x00000000</b>	<b>0 0</b>																															
ID	Acce Field	Value ID	Value	Description																												
A	RW STATE			State D+ and D- lines will be forced into by the DPDMDRIVE task																												
		Resume	1	D+ forced low, D- forced high (K state) for a timing preset in hardware (50 $\mu$ s or 5 ms, depending on bus state)																												
		J	2	D+ forced high, D- forced low (J state)																												
		K	4	D+ forced low, D- forced high (K state)																												

### 6.26.13.44 DTOGGLE

Address offset: 0x50C

Data toggle control and status

Write this register first with VALUE=Nop to select the endpoint; then read it to get the status from VALUE, or write it again with VALUE=Data0 or Data1

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																													C C B			A A A		
<b>Reset 0x00000100</b>		<b>0 0</b>																																
ID	Acce Field	Value ID	Value	Description																														
A	RW EP			Select bulk endpoint number																														
B	RW IO			Selects IN or OUT endpoint																														
		Out	0	Selects OUT endpoint																														
		In	1	Selects IN endpoint																														
C	RW VALUE			Data toggle value																														
		Nop	0	No action on data toggle when writing the register with this value																														
		Data0	1	Data toggle is DATA0 on endpoint set by EP and IO																														
		Data1	2	Data toggle is DATA1 on endpoint set by EP and IO																														

### 6.26.13.45 EPINEN

Address offset: 0x510

Endpoint IN enable

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																													I H G F E D C B A			
<b>Reset 0x00000001</b>		<b>0 1</b>																														
ID	Acce Field	Value ID	Value	Description																												
A-H	RW IN[i] (i=0..7)			Enable IN endpoint i																												
		Disable	0	Disable endpoint IN i (no response to IN tokens)																												
		Enable	1	Enable endpoint IN i (response to IN tokens)																												
I	RW ISOIN			Enable ISO IN endpoint																												
		Disable	0	Disable ISO IN endpoint 8																												
		Enable	1	Enable ISO IN endpoint 8																												

### 6.26.13.46 EPOUTEN

Address offset: 0x514

Endpoint OUT enable

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																													I H G F E D C B A			
<b>Reset 0x00000001</b>		<b>0 1</b>																														
ID	Acce Field	Value ID	Value	Description																												
A-H	RW OUT[i] (i=0..7)			Enable OUT endpoint i																												
		Disable	0	Disable endpoint OUT i (no response to OUT tokens)																												
		Enable	1	Enable endpoint OUT i (response to OUT tokens)																												
I	RW ISOOUT			Enable ISO OUT endpoint 8																												
		Disable	0	Disable ISO OUT endpoint 8																												
		Enable	1	Enable ISO OUT endpoint 8																												

### 6.26.13.47 EPSTALL

Address offset: 0x518

STALL endpoints

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																		
ID																													C	B				A	A	A
Reset 0x00000000		0 0																																		
ID	Acce Field	Value ID	Value	Description																																
A	W EP			Select endpoint number																																
B	W IO			Selects IN or OUT endpoint																																
		Out	0	Selects OUT endpoint																																
		In	1	Selects IN endpoint																																
C	W STALL			Stall selected endpoint																																
		UnStall	0	Don't stall selected endpoint																																
		Stall	1	Stall selected endpoint																																

### 6.26.13.48 ISOSPLIT

Address offset: 0x51C

Controls the split of ISO buffers

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																						
ID																													A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000		0 0																																																						
ID	Acce Field	Value ID	Value	Description																																																				
A	RW SPLIT			Controls the split of ISO buffers																																																				
		OneDir	0x0000	Full buffer dedicated to either ISO IN or OUT																																																				
		HalfIN	0x0080	Lower half for IN, upper half for OUT																																																				

### 6.26.13.49 FRAMECNTR

Address offset: 0x520

Returns the current value of the start of frame counter

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																						
ID																													A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000		0 0																																																						
ID	Acce Field	Value ID	Value	Description																																																				
A	R	FRAMECNTR		Returns the current value of the start of frame counter																																																				

### 6.26.13.50 LOWPOWER

Address offset: 0x52C

Controls USB peripheral low power mode during USB suspend

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	LOWPOWER		Controls USB peripheral low-power mode during USB suspend																												
		ForceNormal	0	Software must write this value to exit low power mode and before performing a remote wake-up																												
		LowPower	1	Software must write this value to enter low power mode after DMA and software have finished interacting with the USB peripheral																												

### 6.26.13.51 ISOINCONFIG

Address offset: 0x530

Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	RESPONSE		Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent																												
		NoResp	0	Endpoint does not respond in that case																												
		ZeroData	1	Endpoint responds with a zero-length data packet in that case																												

### 6.26.13.52 EPIN[n].PTR (n=0..7)

Address offset: 0x600 + (n × 0x14)

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	PTR		Data pointer																												
				See the memory chapter for details about which memories are available for EasyDMA.																												

### 6.26.13.53 EPIN[n].MAXCNT (n=0..7)

Address offset: 0x604 + (n × 0x14)

Maximum number of bytes to transfer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												A	A	A	A	A
Reset	0x00000000																															
Reset	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	MAXCNT	[64..0]	Maximum number of bytes to transfer																												





Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset	0x00000000																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	PTR		Data pointer

See the memory chapter for details about which memories are available for EasyDMA.

### 6.26.13.59 EPOUT[n].MAXCNT (n=0..7)

Address offset: 0x704 + (n × 0x14)

Maximum number of bytes to transfer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
ID																																	A	A	A	A	A	A
Reset	0x00000000																																					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

ID	Acce Field	Value ID	Value	Description
A	RW	MAXCNT	[64..0]	Maximum number of bytes to transfer

### 6.26.13.60 EPOUT[n].AMOUNT (n=0..7)

Address offset: 0x708 + (n × 0x14)

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
ID																																			A	A	A	A	A	A
Reset	0x00000000																																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

ID	Acce Field	Value ID	Value	Description
A	R	AMOUNT		Number of bytes transferred in the last transaction

### 6.26.13.61 ISOOUT.PTR

Address offset: 0x7A0

Data pointer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset	0x00000000																																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	Acce Field	Value ID	Value	Description
A	RW	PTR		Data pointer

See the memory chapter for details about which memories are available for EasyDMA.

### 6.26.13.62 ISOOUT.MAXCNT

Address offset: 0x7A4

Maximum number of bytes to transfer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																																																		
A	RW	MAXCNT			Maximum number of bytes to transfer																																																		

### 6.26.13.63 ISOOUT.AMOUNT

Address offset: 0x7A8

Number of bytes transferred in the last transaction

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																							
ID																								A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	Acce	Field	Value ID	Value	Description																																																		
A	R	AMOUNT			Number of bytes transferred in the last transaction																																																		

## 6.26.14 Electrical specification

### 6.26.14.1 USB Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
R <sub>USB,PU,ACTIVE</sub>	Value of pull-up on D+, bus active (upstream device transmitting)	1425	2300	3090	Ω
R <sub>USB,PU,IDLE</sub>	Value of pull-up on D+, bus idle	900	1200	1575	Ω
t <sub>USB,DETRST</sub>	Minimum duration of an SE0 state to be detected as a USB reset condition				μs
f <sub>USB,CLK</sub>	Frequency of local clock, USB active		48		MHz
f <sub>USB,TOL</sub>	Accuracy of local clock, USB active <sup>33</sup>			±1000	ppm
T <sub>USB,JITTER</sub>	Jitter on USB local clock, USB active			±1	ns

## 6.27 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by the following equation:

$$\text{timeout [s]} = ( \text{CRV} + 1 ) / 32768$$

<sup>33</sup> The local clock can be stopped during USB suspend

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter [CLOCK — Clock control](#) on page 69.

### 6.27.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

### 6.27.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

### 6.27.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See [Reset](#) on page 57 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see [Reset behavior](#) on page 58.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.

### 6.27.4 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog timer	

Table 113: Instances

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4

Register	Offset	Description
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

Table 114: Register overview

### 6.27.4.1 TASKS\_START

Address offset: 0x000

Start the watchdog

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W TASKS_START			Start the watchdog																												
		Trigger	1	Trigger task																												

### 6.27.4.2 EVENTS\_TIMEOUT

Address offset: 0x100

Watchdog timeout

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW EVENTS_TIMEOUT			Watchdog timeout																												
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### 6.27.4.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID																																A
Reset 0x00000000	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	RW TIMEOUT			Write '1' to enable interrupt for event TIMEOUT																												
		Set	1	Enable																												
		Disabled	0	Read: Disabled																												
		Enabled	1	Read: Enabled																												

### 6.27.4.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	TIMEOUT		Write '1' to disable interrupt for event <b>TIMEOUT</b>																											
		Clear	1	Disable																											
		Disabled	0	Read: Disabled																											
		Enabled	1	Read: Enabled																											

### 6.27.4.5 RUNSTATUS

Address offset: 0x400

Run status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A																														
Reset	0x00000000																														
0	0 0																														
ID	Acce Field	Value ID	Value	Description																											
A	R	RUNSTATUS		Indicates whether or not the watchdog is running																											
		NotRunning	0	Watchdog not running																											
		Running	1	Watchdog is running																											

### 6.27.4.6 REQSTATUS

Address offset: 0x404

Request status

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID																													H G F E D C B A		
Reset	0x00000001																														
0	0 1																														
ID	Acce Field	Value ID	Value	Description																											
A-H	R	RR[i] (i=0..7)		Request status for RR[i] register																											
		DisabledOrRequested	0	RR[i] register is not enabled, or are already requesting reload																											
		EnabledAndUnrequested	1	RR[i] register is enabled, and are not yet requesting reload																											

### 6.27.4.7 CRV

Address offset: 0x504

Counter reload value

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																														
ID	A A																														
Reset	0xFFFFFFFF																														
1	1 1																														
ID	Acce Field	Value ID	Value	Description																											
A	RW	CRV	[0xF..0xFFFFFFFF]	Counter reload value in number of cycles of the 32.768 kHz clock																											

### 6.27.4.8 RREN

Address offset: 0x508

Enable register for reload request registers

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID																											H	G	F	E	D	C	B	A
<b>Reset 0x00000001</b>	0 1																																	
ID	Acce Field	Value ID	Value	Description																														
A-H	RW	RR[i] (i=0..7)		Enable or disable RR[i] register																														
		Disabled	0	Disable RR[i] register																														
		Enabled	1	Enable RR[i] register																														

### 6.27.4.9 CONFIG

Address offset: 0x50C

Configuration register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																											C	A				
<b>Reset 0x00000001</b>	0 1																															
ID	Acce Field	Value ID	Value	Description																												
A	RW	SLEEP		Configure the watchdog to either be paused, or kept running, while the CPU is sleeping																												
		Pause	0	Pause watchdog while the CPU is sleeping																												
		Run	1	Keep the watchdog running while the CPU is sleeping																												
C	RW	HALT		Configure the watchdog to either be paused, or kept running, while the CPU is halted by the debugger																												
		Pause	0	Pause watchdog while the CPU is halted by the debugger																												
		Run	1	Keep the watchdog running while the CPU is halted by the debugger																												

### 6.27.4.10 RR[n] (n=0..7)

Address offset: 0x600 + (n × 0x4)

Reload request n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	0 0																															
ID	Acce Field	Value ID	Value	Description																												
A	W	RR		Reload request register																												
		Reload	0x6E524635	Value to request a reload of the watchdog timer																												

## 6.27.5 Electrical specification

### 6.27.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
t <sub>WDT</sub>	Time out interval	458		36	μs

# 7 Hardware and layout

## 7.1 Pin assignments

The pin assignment figures and tables describe the pinouts for the product variants of the chip.

The nRF52820 device provides flexibility regarding GPIO pin routing and configuration. However, some pins have limitations or recommendations for pin configurations and uses.

### 7.1.1 QFN40 pin assignments

The pin assignment figure and table describe the assignments for this variant of the chip.

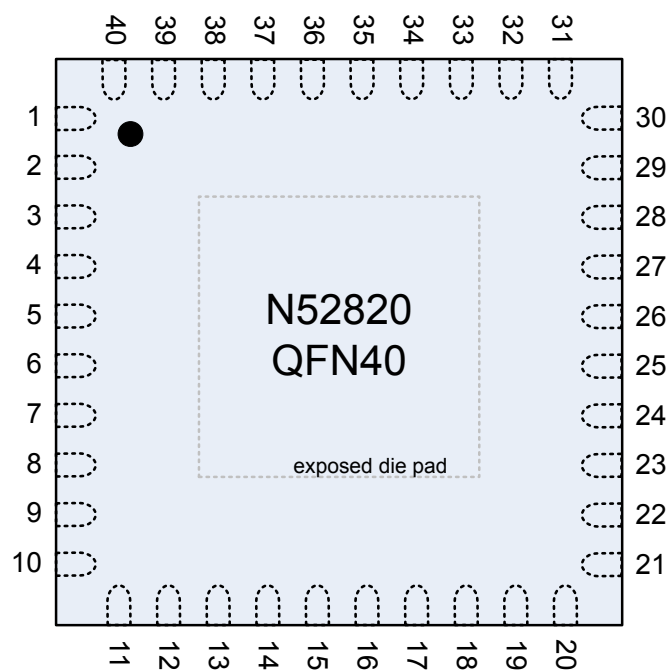


Figure 147: QFN40 pin assignments, top view

Pin	Name	Function	Description	Recommended usage
<b>Left side of the chip</b>				
1	DEC1	Power	1.1 V Digital supply decoupling	
2	P0.00	Digital I/O	General purpose I/O	
	XL1	Analog input	Connection for 32.768 kHz crystal	
3	P0.01	Digital I/O	General purpose I/O	
	XL2	Analog input	Connection for 32.768 kHz crystal	
4	P0.04	Digital I/O	General purpose I/O	
	AIN2	Analog input	Analog input	
5	P0.05	Digital I/O	General purpose I/O	
	AIN3	Analog input	Analog input	
6	P0.06	Digital I/O	General purpose I/O	
7	P0.07	Digital I/O	General purpose I/O	
8	VDD	Power	Power supply	
9	VDDH	Power	High voltage power supply	
10	VBUS	Power	5 V input for USB 3.3 V regulator	
<b>Bottom side of the chip</b>				
11	DECUSB	Power	USB 3.3 V regulator supply decoupling	
12	D-	USB	USB D-	
13	D+	USB	USB D+	
14	P0.14	Digital I/O	General purpose I/O	
15	P0.15	Digital I/O	General purpose I/O	
16	P0.18	Digital I/O	General purpose I/O	
	nRESET		Configurable as pin RESET	
17	P0.20	Digital I/O	General purpose I/O	
18	VDD	Power	Power supply	
19	SWDIO	Debug	Serial wire debug I/O for debug and programming	
20	SWDCLK	Debug	Serial wire debug clock input for debug and programming	
<b>Right side of the chip</b>				
21	DEC5	Power	1.3 V regulator supply decoupling	
22	P0.16	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
23	P0.17	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
24	ANT	RF	Single-ended radio antenna connection	See <a href="#">Reference circuitry</a> on page 418 for guidelines on how to ensure good RF performance
25	VSS_PA	Power	Ground (radio supply)	
26	DEC6	Power	1.3 V regulator supply decoupling	Must be connected to DEC4 (pin 38)
27	DEC3	Power	Power supply, decoupling	
28	XC1	Analog input	Connection for 32 MHz crystal	
29	XC2	Analog input	Connection for 32 MHz crystal	
30	VDD	Power	Power supply	
<b>Top side of the chip</b>				
31	P0.08	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
32	P0.29	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
33	P0.30	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only



Pin	Name	Function	Description	Recommended usage
34	P0.28	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
35	P0.03	Digital I/O	General purpose I/O	Standard drive, low frequency I/O only
	AIN1	Analog input	Analog input	
36	P0.02	Digital I/O	General purpose I/O	
	AIN0	Analog input	Analog input	
37	VSS	Power	Ground	
38	DEC4	Power	1.3 V regulator supply decoupling	Must be connected to DEC6 (pin 26)
39	DCC	Power	DC/DC converter output	
40	VDD	Power	Power supply	
<b>Backside of the the chip</b>				
Die pad	VSS	Power	Ground pad	Exposed die pad must be connected to ground (VSS) for proper device operation

Table 115: QFN40 pin assignments

For more information on standard drive, see [GPIO — General purpose input/output](#) on page 127. Low frequency I/O is a signal with a frequency up to 10 kHz.

## 7.2 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

### 7.2.1 QFN40 5 x 5 mm package

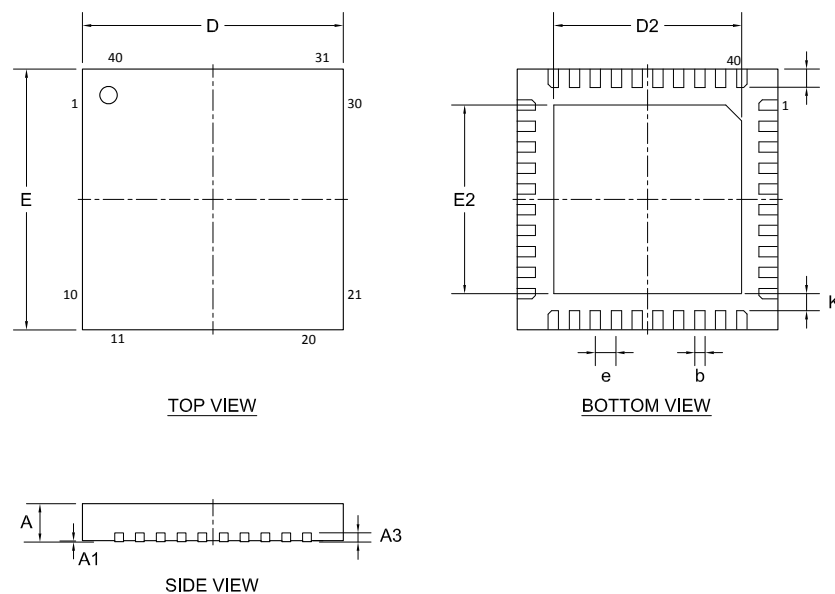


Figure 148: QFN40 5 x 5 mm package

	A	A1	A3	b	D, E	D2, E2	e	K	L
<b>Min.</b>	0.80	0.00		0.15	4.90	3.50		0.20	0.30
<b>Nom.</b>	0.85	0.035	0.203	0.20	5.00	3.60	0.40		0.35
<b>Max.</b>	0.90	0.05		0.25	5.10	3.70			0.40

Table 116: QFN40 dimensions in millimeters

## 7.3 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

In this section there are reference circuits for QDAA QFN40 package, showing the components and component values to support on-chip features in a design.

**Note:** This is not a complete list of configurations, but all required circuitry is shown for further configurations.

Some general guidance is summarized here:

- When supplying power from a USB source only, VBUS must be connected to VDDH if USB is to be used.
- Components required for DC/DC function are only needed if DC/DC mode is enabled for that regulator.
- USB can be used in any configuration as long as VBUS is supplied by the USB host.
- The schematics include an optional series resistor on the USB supply for improved immunity to transient overvoltage during VBUS connection. Using the series resistor is recommended for new designs.

### Circuit configurations for QDAA QFN40

Config no.	Supply configuration		Features that can be enabled for each configuration example	
	VDDH	VDD	DCDCEN1	USB
Config. 1	USB (VDDH = VBUS)	N/A	No	Yes
Config. 2	N/A	Battery/Ext. regulator	Yes	Yes
Config. 3	N/A	Battery/Ext. regulator	No	Yes
Config. 4	N/A	Battery/Ext. regulator	No	No

Table 117: Circuit configurations

#### 7.3.1 Circuit configuration no. 1 for QDAA QFN40

This section contains a configuration summary, a schematic, and bill of materials table for QDAA QFN40 circuit configuration number 1.

Config no.	Supply configuration	Enabled features		
	VDDH	VDD	DCDCEN1	USB
Config. 1	USB (VDDH = VBUS)	N/A	No	Yes

Table 118: Configuration summary for circuit configuration no. 1

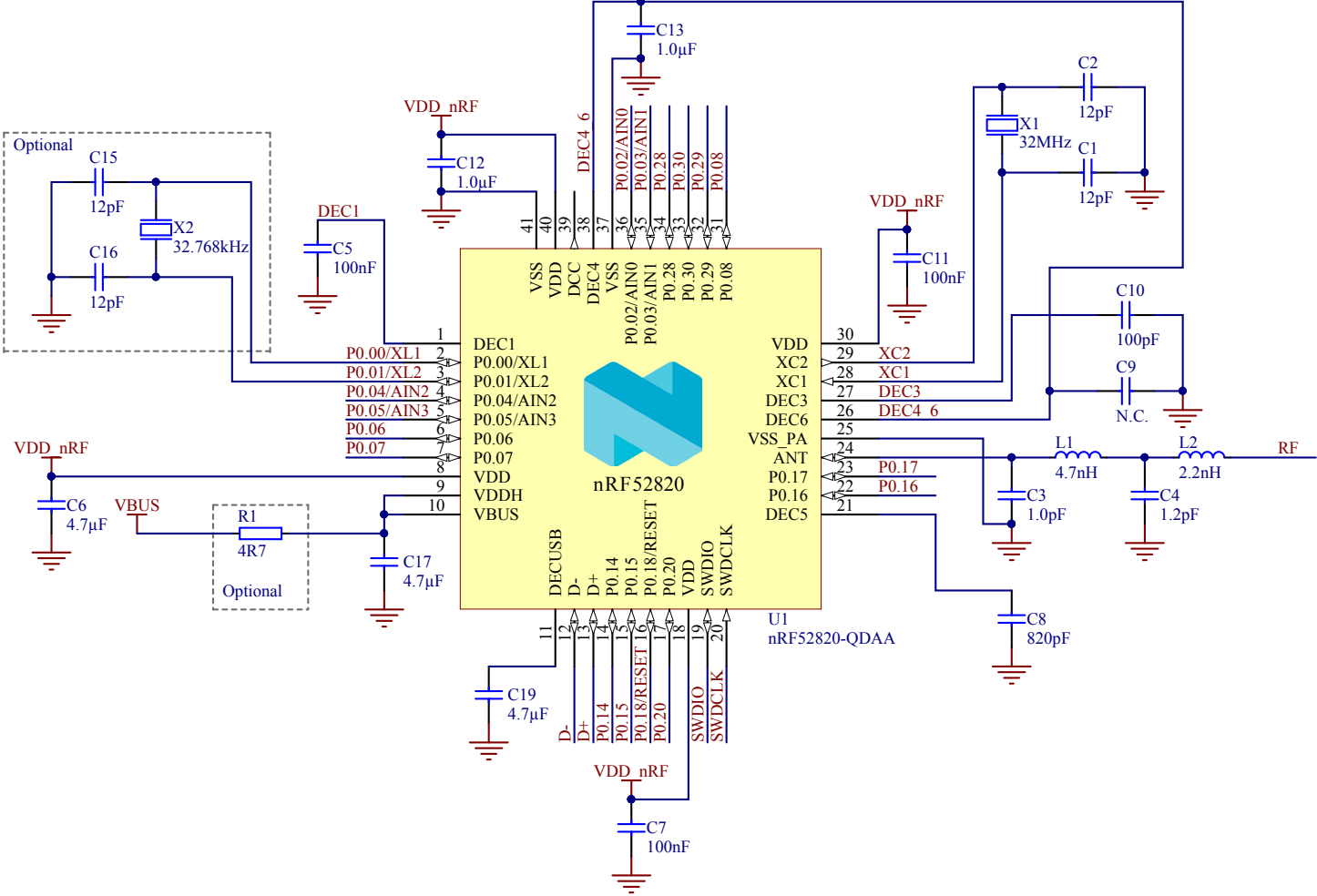


Figure 149: Circuit configuration no. 1 schematic for QDAA QFN40

**Note:** For PCB reference layouts, see the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

Designator	Value	Description	Footprint
C1, C2, C15, C16	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4	1.2 pF	Capacitor, NPO, $\pm 5\%$	0201
C5, C7, C11	100 nF	Capacitor, X7S, $\pm 10\%$	0201
C6, C19	4.7 $\mu$ F	Capacitor, X7R, $\pm 10\%$	0603
C8	820 pF	Capacitor, X7R, $\pm 10\%$	0201
C9	N.C.	Not mounted	0201
C10	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C12, C13	1.0 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0402
C17	4.7 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0603
L1	4.7 nH	High frequency chip inductor, $\pm 5\%$	0201
L2	2.2 nH	High frequency chip inductor, $\pm 5\%$	0201
R1	4R7	Resistor $\pm 1\%$ , 0.05 W	0201
U1	nRF52820-QDAA	Multiprotocol <i>Bluetooth</i> <sup>®</sup> Low Energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary System on Chip	QFN-40
X1	32 MHz	Crystal SMD 1612, 32 MHz, Cl=8 pF, Total Tol: $\pm 40$ ppm	XTAL_1612
X2	32.768 kHz	Crystal SMD 2012, 32.768 kHz, Cl=9 pF, Total Tol: $\pm 50$ ppm	XTAL_2012

Table 119: Bill of material for circuit configuration no. 1

### 7.3.2 Circuit configuration no. 2 for QDAA QFN40

This section contains a configuration summary, a schematic, and bill of materials table for QDAA QFN40 circuit configuration number 2.

Config no.	Supply configuration		Enabled features	
	VDDH	VDD	DCDCEN1	USB
Config. 2	N/A	Battery/Ext. regulator	Yes	Yes

Table 120: Configuration summary for circuit configuration no. 2

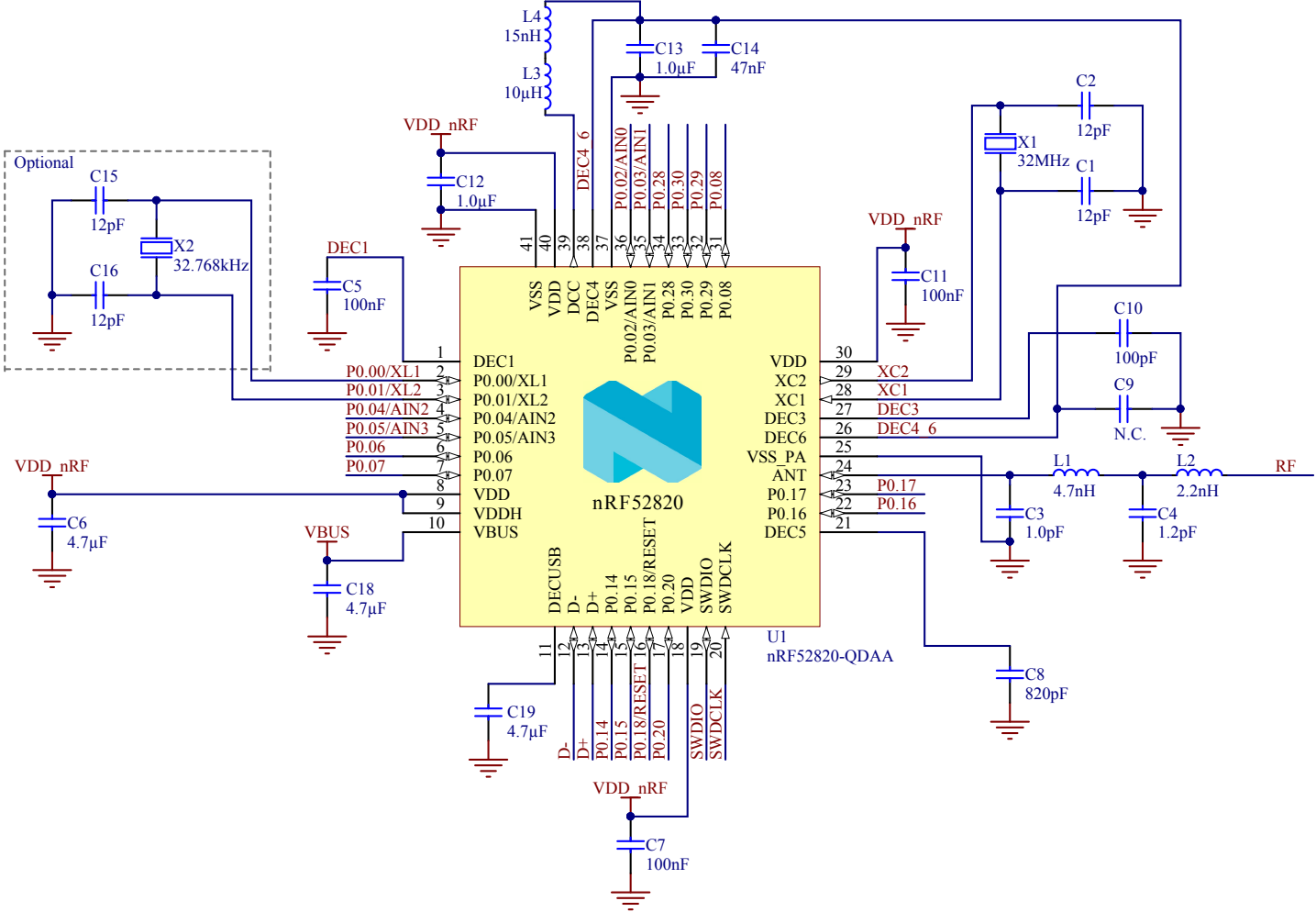


Figure 150: Circuit configuration no. 2 schematic for QDAA QFN40

**Note:** For PCB reference layouts, see the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

Designator	Value	Description	Footprint
C1, C2, C15, C16	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4	1.2 pF	Capacitor, NPO, $\pm 5\%$	0201
C5, C7, C11	100 nF	Capacitor, X7S, $\pm 10\%$	0201
C6, C19	4.7 $\mu$ F	Capacitor, X7R, $\pm 10\%$	0603
C8	820 pF	Capacitor, X7R, $\pm 10\%$	0201
C9	N.C.	Not mounted	0201
C10	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C12, C13	1.0 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0402
C14	47 nF	Capacitor, X7S, $\pm 10\%$	0201
C18	4.7 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0603
L1	4.7 nH	High frequency chip inductor, $\pm 5\%$	0201
L2	2.2 nH	High frequency chip inductor, $\pm 5\%$	0201
L3	10 $\mu$ H	Chip inductor, IDC,min = 50 mA, $\pm 20\%$	0603
L4	15 nH	High frequency chip inductor, $\pm 10\%$	0402
U1	nRF52820-QDAA	Multiprotocol <i>Bluetooth</i> <sup>®</sup> Low Energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary System on Chip	QFN-40
X1	32 MHz	Crystal SMD 1612, 32 MHz, Cl=8 pF, Total Tol: $\pm 40$ ppm	XTAL_1612
X2	32.768 kHz	Crystal SMD 2012, 32.768 kHz, Cl=9 pF, Total Tol: $\pm 50$ ppm	XTAL_2012

Table 121: Bill of material for circuit configuration no. 2

### 7.3.3 Circuit configuration no. 3 for QDAA QFN40

This section contains a configuration summary, a schematic, and bill of materials table for QDAA QFN40 circuit configuration number 3.

Config no.	Supply configuration		Enabled features	
	VDDH	VDD	DCDCEN1	USB
Config. 3	N/A	Battery/Ext. regulator	No	Yes

Table 122: Configuration summary for circuit configuration no. 3

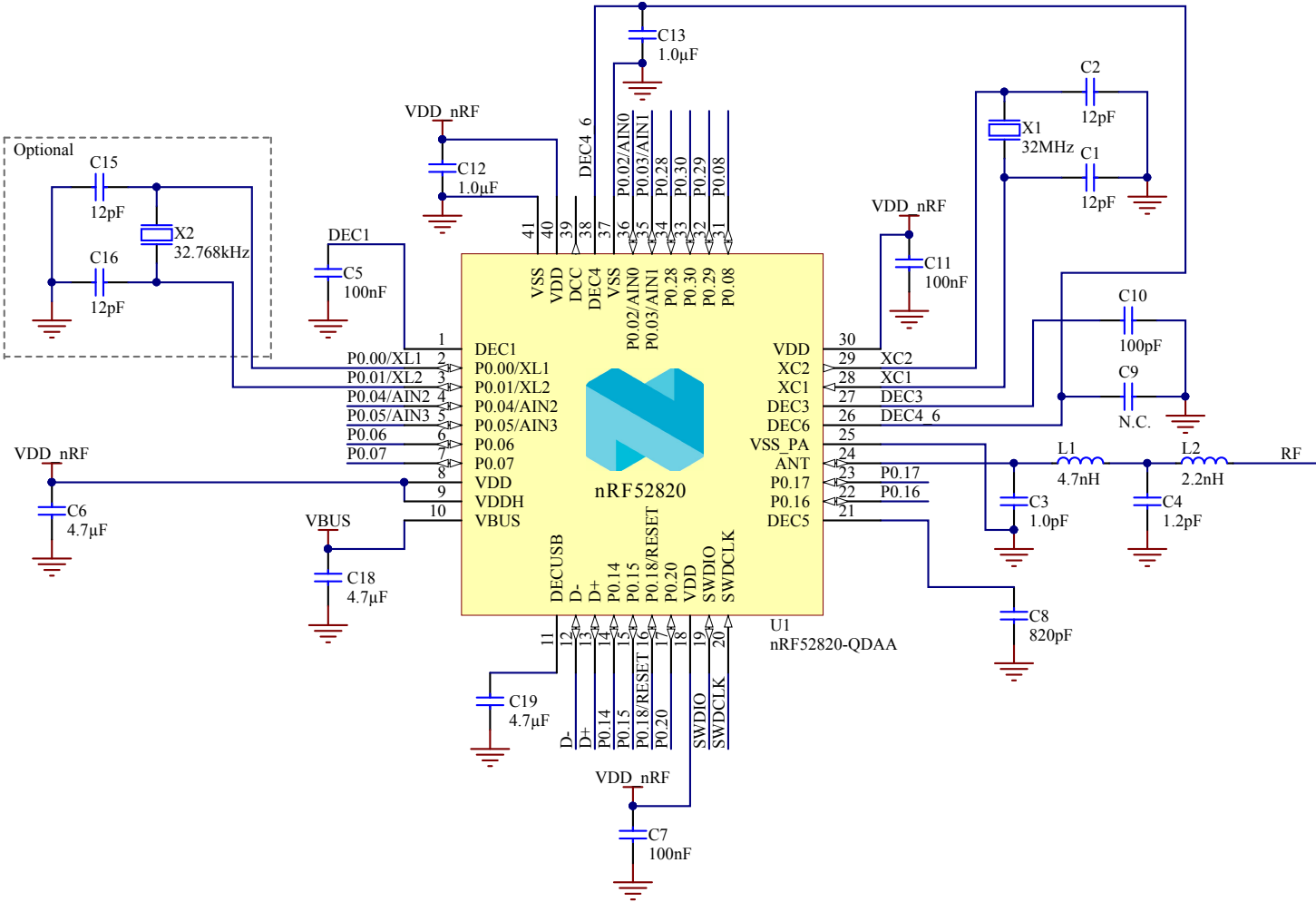


Figure 151: Circuit configuration no. 3 schematic for QDAA QFN40

**Note:** For PCB reference layouts, see the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

Designator	Value	Description	Footprint
C1, C2, C15, C16	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4	1.2 pF	Capacitor, NPO, $\pm 5\%$	0201
C5, C7, C11	100 nF	Capacitor, X7S, $\pm 10\%$	0201
C6, C19	4.7 $\mu$ F	Capacitor, X7R, $\pm 10\%$	0603
C8	820 pF	Capacitor, X7R, $\pm 10\%$	0201
C9	N.C.	Not mounted	0201
C10	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C12, C13	1.0 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0402
C18	4.7 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0603
L1	4.7 nH	High frequency chip inductor, $\pm 5\%$	0201
L2	2.2 nH	High frequency chip inductor, $\pm 5\%$	0201
U1	nRF52820-QDAA	Multiprotocol <i>Bluetooth</i> <sup>®</sup> Low Energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary System on Chip	QFN-40
X1	32 MHz	Crystal SMD 1612, 32 MHz, Cl=8 pF, Total Tol: $\pm 40$ ppm	XTAL_1612
X2	32.768 kHz	Crystal SMD 2012, 32.768 kHz, Cl=9 pF, Total Tol: $\pm 50$ ppm	XTAL_2012

Table 123: Bill of material for circuit configuration no. 3

### 7.3.4 Circuit configuration no. 4 for QDAA QFN40

This section contains a configuration summary, a schematic, and bill of materials table for QDAA QFN40 circuit configuration number 4.

Config no.	Supply configuration		Enabled features	
	VDDH	VDD	DCDCEN1	USB
Config. 4	N/A	Battery/Ext. regulator	No	No

Table 124: Configuration summary for circuit configuration no. 4



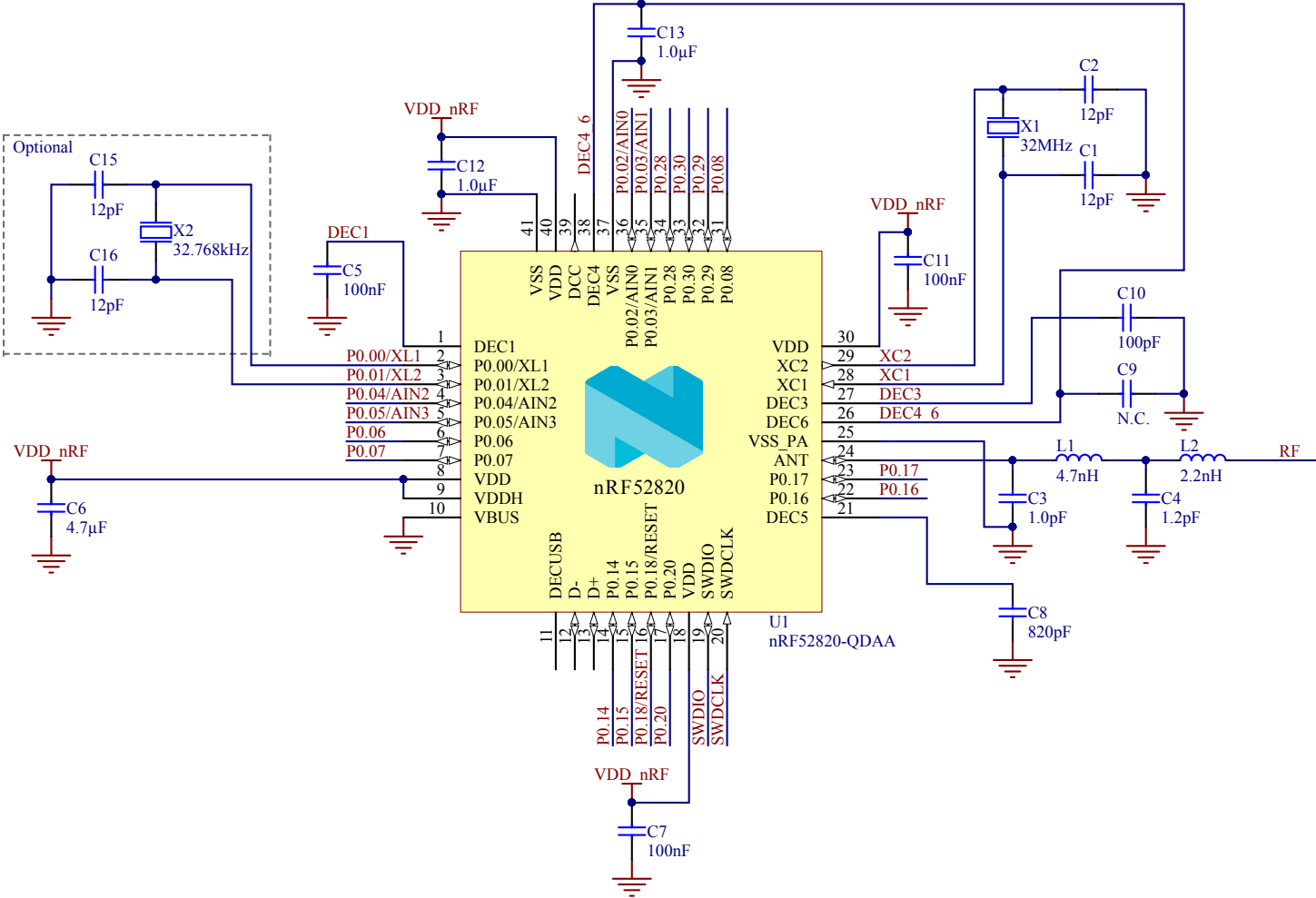


Figure 152: Circuit configuration no. 4 schematic for QDAA QFN40

**Note:** For PCB reference layouts, see the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

Designator	Value	Description	Footprint
C1, C2, C15, C16	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4	1.2 pF	Capacitor, NPO, $\pm 5\%$	0201
C5, C7, C11	100 nF	Capacitor, X7S, $\pm 10\%$	0201
C6	4.7 $\mu$ F	Capacitor, X7R, $\pm 10\%$	0603
C8	820 pF	Capacitor, X7R, $\pm 10\%$	0201
C9	N.C.	Not mounted	0201
C10	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C12, C13	1.0 $\mu$ F	Capacitor, X7S, $\pm 10\%$	0402
L1	4.7 nH	High frequency chip inductor, $\pm 5\%$	0201
L2	2.2 nH	High frequency chip inductor, $\pm 5\%$	0201
U1	nRF52820-QDAA	Multiprotocol <i>Bluetooth</i> <sup>®</sup> Low Energy, IEEE 802.15.4, ANT, and 2.4 GHz proprietary System on Chip	QFN-40
X1	32 MHz	Crystal SMD 1612, 32 MHz, Cl=8 pF, Total Tol: $\pm 40$ ppm	XTAL_1612
X2	32.768 kHz	Crystal SMD 2012, 32.768 kHz, Cl=9 pF, Total Tol: $\pm 50$ ppm	XTAL_2012

Table 125: Bill of material for circuit configuration no. 4

### 7.3.5 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. Poor layout can lead to loss in performance or functionality.

A qualified RF layout for the device and its surrounding components, including matching networks, can be downloaded from [www.nordicsemi.com](http://www.nordicsemi.com).

To ensure optimal performance it is essential that you follow the schematics and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All reference circuits are designed for use with a 50  $\Omega$  single-ended antenna.

A PCB with a minimum of four layers, including a ground plane, is recommended for optimal performance. On the inner layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50  $\Omega$ ) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended package reference circuitry in [Reference circuitry](#) on page 418.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the device. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

### 7.3.6 PCB layout example

The PCB layout shown in the following figures is a reference layout for the QFN package with internal LDO setup and VBUS supply.

**Note:** Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS\_PA pin 25. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the product page for the nRF52820 on [www.nordicsemi.com](http://www.nordicsemi.com).

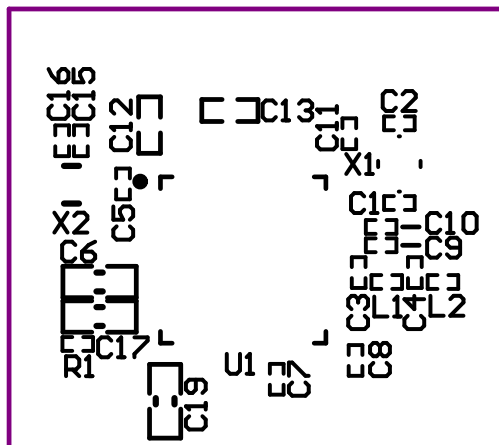


Figure 153: Top silk layer

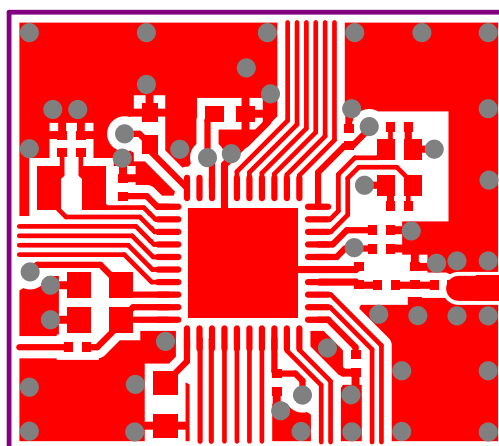


Figure 154: Top layer

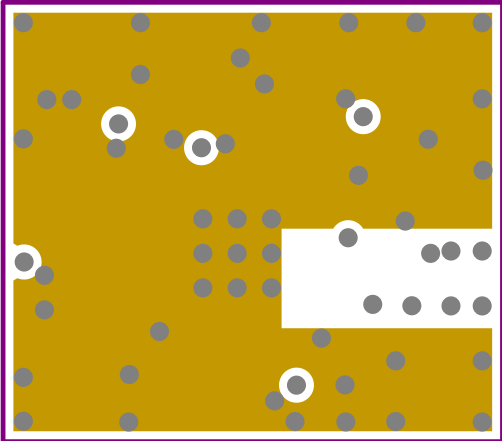


Figure 155: Mid layer 1

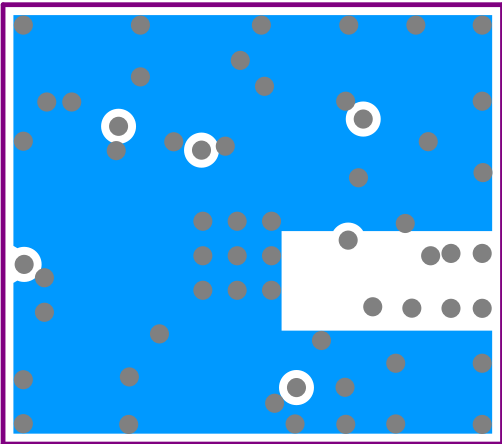


Figure 156: Mid layer 2

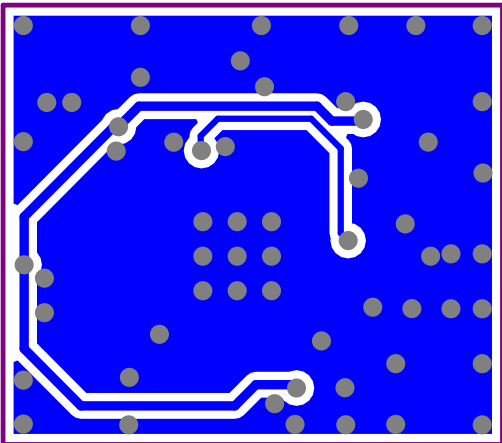


Figure 157: Bottom layer

**Note:** No components in bottom layer.

### 7.4 Package thermal characteristics

The thermal characteristics for the available device packages are found in the following table.

---

Symbol	Package	Typ.	Unit
$\theta_{JA,QFN40}$	QFN40	136.59	°C/W

Table 126: Package thermal characteristics

Values obtained by simulation following the EIA/JESD51-2 for still air condition.

# 8 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Units
VDD	VDD supply voltage, independent of DCDC enable	1.7	3.0	3.6	V
VDDPOR	VDD supply voltage needed during power-on reset	1.75			V
VDDH	VDDH supply voltage	2.5	3.7	5.5	V
VBUS	VBUS USB supply voltage	4.35	5.0	5.5	V
t <sub>R_VDD</sub>	Supply rise time (0 V to 1.7 V)			60	ms
t <sub>R_VDDH</sub>	Supply rise time (0 V to 3.7 V)			100	ms
T <sub>A</sub>	Operating temperature	-40	25	85	°C
T <sub>AEXT</sub>	Extended operating temperature	85		105	°C
T <sub>J</sub>	Junction temperature			110	°C

Table 127: Recommended operating conditions

**Note:** The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

## 8.1 Extended Operating Temperature

The operating temperature range for the device is defined in [Recommended operating conditions](#) on page 430. The range extends from T<sub>A</sub> minimum to T<sub>AEXT</sub> maximum.

Some electrical parameters are valid only for the T<sub>A</sub> operating temperature conditions. When this is the case, an additional parameter for the T<sub>AEXT</sub> extended operating temperature condition is provided.

**Note:** When running the device in the extended operating temperature conditions range, the register [LFXODEBOUNCE](#) on page 81 must be set to `Extended`.

To avoid surpassing the maximum die junction temperature, see [Recommended operating conditions](#) on page 430, it is important to minimize current consumption when operating in the extended operating temperature conditions. To achieve this, it is recommended to use the device in Normal Voltage mode with DC/DC enabled. See [POWER — Power supply](#) on page 49 for details about main supply modes.

# 9 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.<sup>34</sup>

	Note	Min.	Max.	Unit
<b>Supply voltages</b>				
VDD		-0.3	+3.9	V
VDDH		-0.3	+5.8	V
VBUS		-0.3	+5.8	V
VSS			0	V
<b>I/O pin voltage</b>				
$V_{I/O}$ , VDD $\leq$ 3.6 V		-0.3	VDD + 0.3	V
$V_{I/O}$ , VDD $>$ 3.6 V		-0.3	3.9	V
<b>Environmental QFN40 package</b>				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		3	kV
ESD HBM Class	Human Body Model Class		2	
ESD CDM	Charged Device Model		1	kV
<b>Flash memory</b>				
Endurance		10 000		write/erase cycles
Retention at 85 °C		10		years
Retention at 105 °C	Limited to 1000 write/erase cycles	3		years
Retention at 105 °C-85 °C, execution split	Limited to 1000 write/erase cycles	6.7		years

75% execution time at 85 °C or less

Table 128: Absolute maximum ratings



<sup>34</sup> For accelerated life time testing (HTOL, etc) supply voltage should not exceed the recommended operating conditions max value, see [Recommended operating conditions](#) on page 430.

# 10 Ordering information

This chapter contains information on device marking, ordering codes, and container sizes.

## 10.1 Device marking

The nRF52820 package is marked as shown in the following figure.

N	5	2	8	2	0
<P>	P>	<V>	V>	<H>	<P>
<Y>	Y>	<W>	W>	<L>	L>

Figure 158: Package marking

## 10.2 Box labels

The following figures show the box labels used for nRF52820.

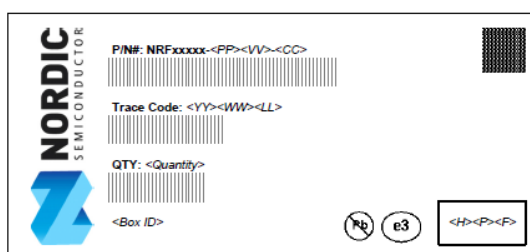


Figure 159: Inner box label



Figure 160: Outer box label

### 10.3 Order code

The following are the order codes and definitions for nRF52820.

n	R	F	5	2	8	2	0	-	<P	P>	<V	V>	-	<C	C>
---	---	---	---	---	---	---	---	---	----	----	----	----	---	----	----

Figure 161: Order code

Abbreviation	Definition and implemented codes
N52/nRF52	nRF52 Series product
820	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 129: Abbreviations

## 10.4 Code ranges and values

Defined here are the nRF52820 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QD	QFN	5 x 5	40	0.4

Table 130: Package variant codes

<VV>	Flash (kB)	RAM (kB)
AA	256	32

Table 131: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 132: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 133: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 134: Production version codes

<YY>	Description
[00 . . 99]	Production year: 2000 to 2099

Table 135: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 136: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 137: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 138: Container codes

## 10.5 Product options

Defined here are the nRF52820 product options.

Order code	MOQ <sup>35</sup>
nRF52820-QDAA-R7	1500
nRF52820-QDAA-R	4000

Table 139: nRF52820 order codes

<sup>35</sup> Minimum Ordering Quantity

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