Datasheet

Automotive Power Management IC

PMIC for Automotive Camera

BD86852MUF-C

General Description

BD86852MUF-C is a power management IC with primary buck converter (DC/DC1), secondary buck converters (DC/DC2 and DC/DC3), external linear regulator control block and the power-on reset function for CMOS sensor and image sensing power supply. Output voltage and sequence are selectable and applicable to various image sensor power supply.
This device adopts small package VQFN24FV4040 which is optimal for camera module. In addition, this device has a pin that can be programmed to turn on/off the spread spectrum providing a lower noise regulated outputs.

Features

- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Primary DC/DC (VO1)
  DC/DC with built-in FET
  High Efficiency with Synchronous Rectification
- Dual Secondary DC/DC (VO2, VO3)
  DC/DC with built-in FET
  High Efficiency with Synchronous Rectification
- Each Protection Function
- Spread Spectrum for EMC
- Fail Detection Pin (for each output)
- Selectable Output Voltage and Sequence

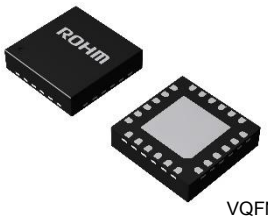
(Note 1) Grade 1

Key Specifications

- Power Supply Voltage Rating: 20 V (Max)
- Power Supply Voltage Range: 4.0 V to 18 V
- Output Voltage:
  - VO1: 3.3 V or 3.9 V (±2 %)
  - VO2: 1.1 V or 1.2 V (±2 %)
  - VO3: 1.8 V (±2 %)
- Output Current:
  - VO1: 2 A (Max)
  - VO2: 1 A (Max)
  - VO3: 1 A (Max)
- Switching Frequency: 2.2 MHz (±200 kHz)
- Stand-by Current: 0 µA (Typ)
- Operating Ambient Temperature Range: -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
VQFN24FV4040	4.0 mm x 4.0 mm x 1.0 mm

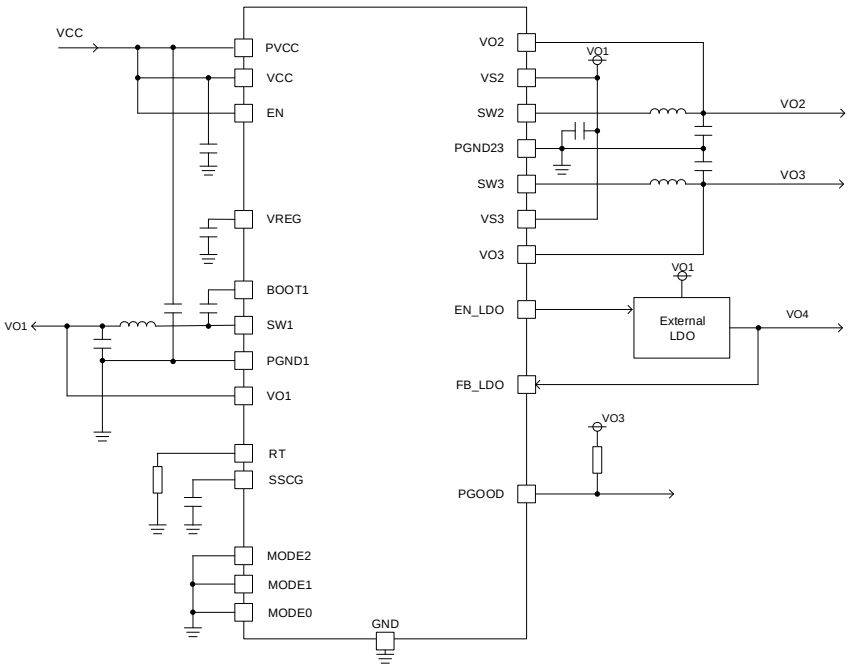


VQFN24FV4040
Wettable Flank Package

Applications

- ADAS
- Camera System (Automotive Camera and Security Camera) using CMOS Sensor

Typical Application Circuit



○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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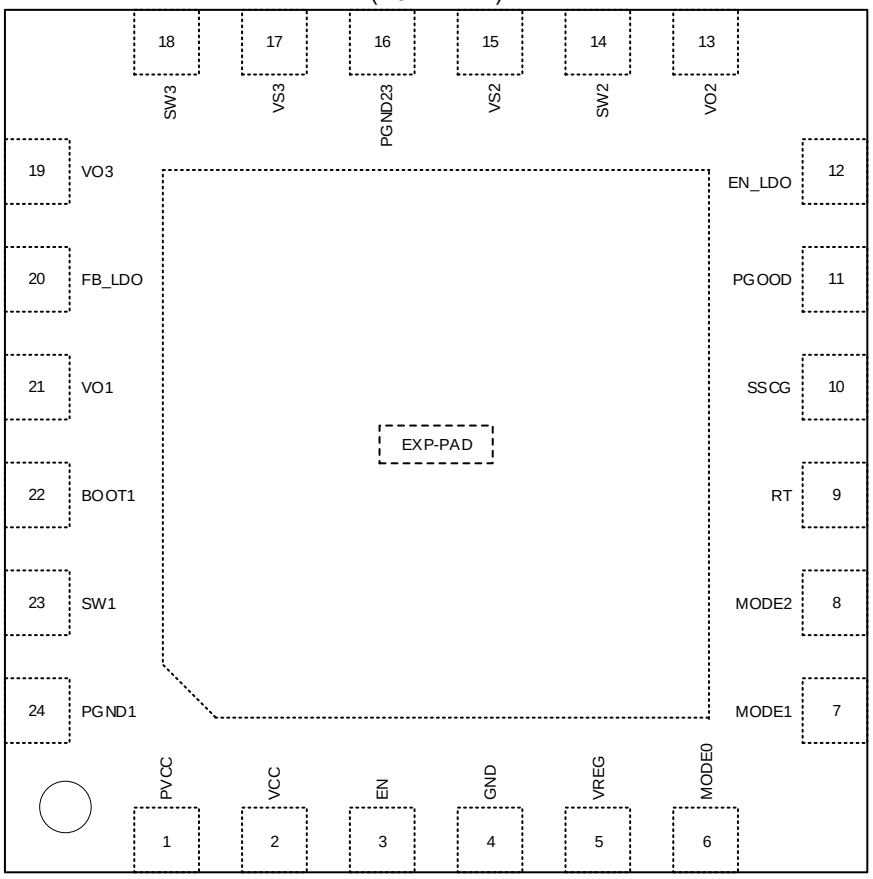
Pin Configuration

(TOP VIEW)



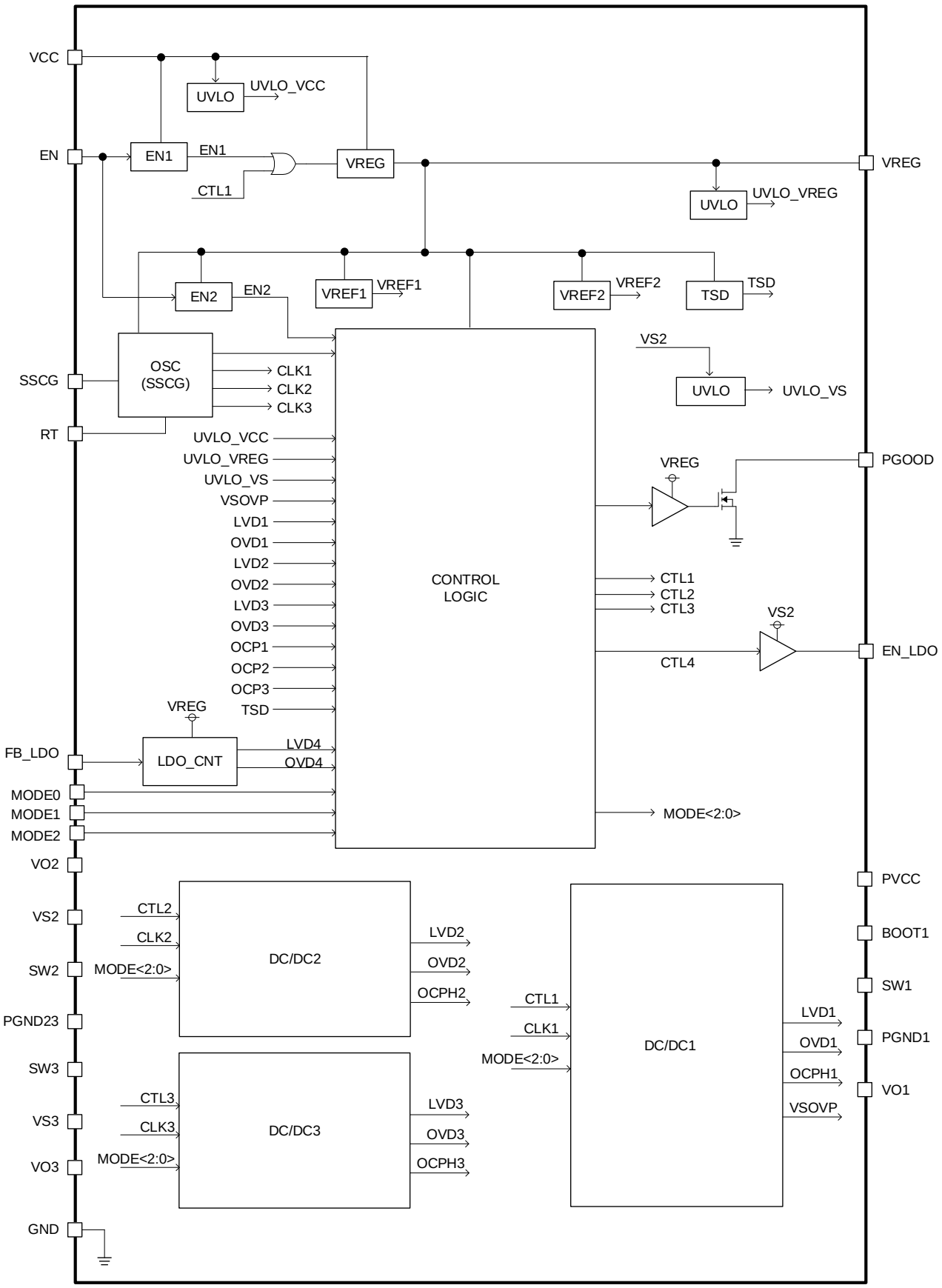
Pin Descriptions

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PVCC	Power supply for DC/DC1	13	VO2	DC/DC2 output voltage feedback
2	VCC	Power supply	14	SW2	DC/DC2 switching output
3	EN	Enable control input	15	VS2	Power supply for DC/DC2
4	GND	Ground	16	PGND23	Power ground for DC/DC2 and DC/DC3
5	VREG	Internal regulator output	17	VS3	Power supply for DC/DC3
6	MODE0	Mode select 0*(Note 1)*	18	SW3	DC/DC3 switching output
7	MODE1	Mode select 1*(Note 1)*	19	VO3	DC/DC3 output voltage feedback
8	MODE2	Mode select 2*(Note 1)*	20	FB_LDO	External LDO voltage feedback
9	RT	Adjust switching frequency	21	VO1	DC/DC1 output voltage feedback
10	SSCG	SSCG setting*(Note 2)*	22	BOOT1	DC/DC1 high side driver supply pin
11	PGOOD	Power Good *(Note 3)* (N-channel open-drain)	23	SW1	DC/DC1 switching output
12	EN_LDO	External LDO enable control output	24	PGND1	Power ground for DC/DC1
-	-	-	-	EXP-PAD	The EXP-PAD connect to GND, PGND1 and PGND23.

(Note 1) Connect to the GND pin or the VREG pin.
(Note 2) If not in use, connect to the GND pin.
(Note 3) If not in use, open.

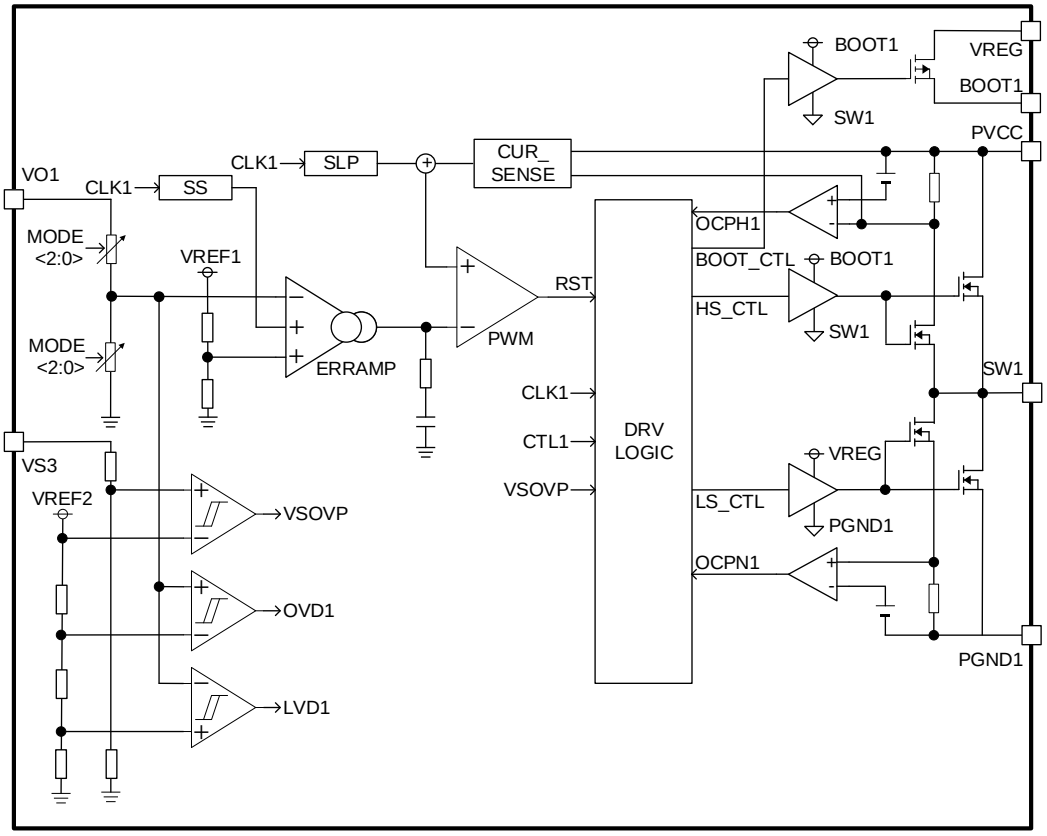
Block Diagrams

1. Top Block Diagram

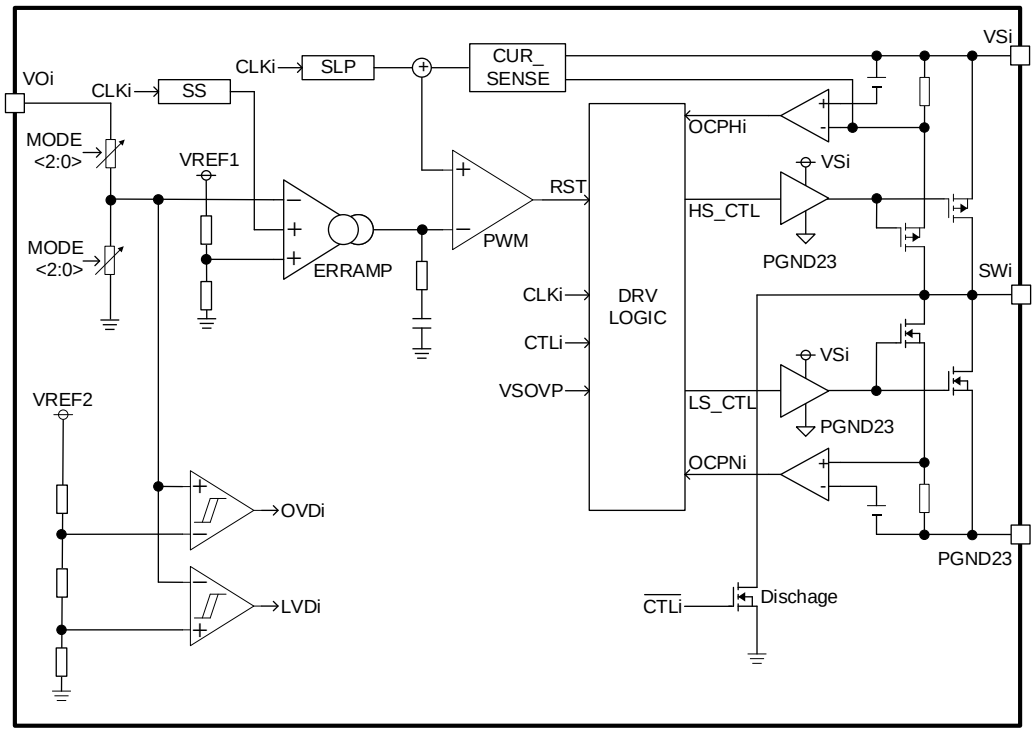


Block Diagrams – Continued

2. DC/DC1 Block Diagram



3. DC/DC2 and DC/DC3 Block Diagram (i = 2, 3)



Description of Blocks

- **Internal Regulator (VREG) Block**
  VREG is the linear regulator for PMIC use only (Do not use it for other purposes.).
  The VREG pin needs an appropriate external bypath capacitor. This is controlled by the EN1 internal signal.
  When the EN pin voltage is more than 2.6 V, the EN1 signal becomes high, and when it's less than 0.8 V, the EN1 signal becomes low.
  VREG stops when the EN1 signal and the CTL1 internal signal are low.

- **Reference Voltage (VREF1 and VREF2) Block**
  Two independent reference voltages, one for the output voltage and the other for the voltage detections.

- **Under Voltage Lock-Out Block for VCC (UVLO_VCC, UVLO_VREG and UVLO_VS)**
  Input low-voltage detections for the VCC, VREG and VS2 pins.
  If any one of these input low-voltages are detected, the device goes into the UVLO state (See below for more details).

  UVLO_VCC and UVLO_VREG
  When UVLO is detected from these pins, all the outputs (VO1 to VO3 and EN_LDO) turn off immediately. And then, the PGOOD pin changes to low. Once the UVLO condition is removed, the device waits 200 µs (Typ) and starts VO1 rail power-up.

  UVLO_VS
  When UVLO is detected from VS2 pins, the secondary outputs (VO2, VO3 and EN_LDO) turn off immediately. And then, the PGOOD pin changes to low. Once the UVLO condition is removed, VO2, VO3 and EN_LDO turn on by the normal sequence.

- **Thermal Shutdown Protection (TSD) Block**
  To prevent IC from causing thermal destruction and thermal runaway, the TSD operates when chip temperature reaches 175 °C (Typ) or more. When TSD operates, all of the outputs (VO1 to VO3 and EN_LDO) turn off at the same time, and PGOOD changes low. IC resumes by sequence after chip temperature decreases to certain temperature.
  However, this thermal protection circuit is designed to protect IC itself from destruction. Do not exceed the chip temperature Tjmax = 150 °C.

- **Oscillator (OSC) Block**
  OSC generates clock for DC/DC1, 2, 3 and CONTROL block. The DC/DC1 operates in phase with the DC/DC3, and the DC/DC2 operates 180 degrees out of phase to reduce the input ripple current.

- **Spread Spectrum Clock Generator (SSCG) Block**
  OSC block built in spread spectrum clock generator (SSCG) function. Insert a capacitor of 3300 pF between SSCG pin and GND, it enables the spread-spectrum function. In this mode, the frequency is reduced by 5 % from the RT programmed center frequency and is modulated by ±3 % with 2.5 kHz modulation frequency.

- **External LDO Controller (LDO_CNT) Block**
  This IC outputs the control signal to External LDO from the EN_LDO pin. The power supply of the EN_LDO output buffer is VS2. When detection (LVD4 and OVD4) of external LDO output is necessary, short the external LDO output and FB_LDO.

Description of Blocks – continued

- **Error Amplifier (ERRAMP) Block**
  Error Amplifier with reference voltage and VO voltage divider input.
  Controls On Duty width of switching pulse by output of ERRAMP.
  Capacitor and resistor for phase compensation are fixed.

- **Slope (SLP) Block**
  The saw tooth wave generator for the duty modulation. The summation of the saw tooth waveform and the upper FET current information will be sent to PWM.

- **Current Comparator (CUR_SENSE) Block**
  The CUR_SENSE block outputs a waveform depending on the current of the inductance.

- **Soft Start (SS) Block**
  The SS block slows down the rise of output voltage during start-up. This reduces inrush current during start-up and the overshoot of the output. The soft start ramp is generated by CLK and digital-to-analog converter (DAC).

- **PWM Comparator (PWM) Block**
  The PWM block compares the output of ERRAMP with the synthetic waveform of SLP and CUR_SENSE, and adjusts duty for switching operation.

- **Driver Logic (DRV LOGIC) Block and Driver (DRV) Block**
  The DRV_LOGIC block control BOOT_CTL, HS_CTL and LS_CTL. The DRV blocks drive Power FET.

- **Over Voltage Protection (VSOVP) Block at DC/DC1**
  When the VS3 pin voltage exceeds the threshold of VSOVP, high side FET and low side FET turn off.

- **Over Voltage Detection (OVD1, OVD2, OVD3 and OVD4)**
  PGOOD is an open-drain output which pull-up resistor is required when usage.
  The VO1, VO2, VO3 and FB_LDO pins have the over voltage detection feature. Any one of these over voltage detection can make the PGOOD pin to pull low. Once the over voltage is removed, the PGOOD pin follows in 10 ms (Typ). This timer is dependent on the programmed operating frequency. The PGOOD pin is an open-drain pin and needs an external pull-up resistor.

- **Lower Voltage Detection (LVD1, LVD2, LVD3 and LVD4)**
  PGOOD is open-drain output which pull-up resistor is required when usage.
  The VO1, VO2, VO3 and FB_LDO pins have the lower voltage detection feature. Any one of these lower voltage detection can make the PGOOD pin to pull low. Once the lower voltage is removed, the PGOOD pin follows in 10 ms (Typ). This timer is dependent on the programmed operating frequency. The PGOOD pin is open-drain pins and need an external pull-up resistor.

- **Over Current Protection (OCPH1, OCPH2, OCPH3, OCPN1, OCPN2 and OCPN3)**
  The over current protection feature limits the FET current and successfully protects all the FETs from the permanent damage.
  This feature is intended for an accidental short only minimizing secondary disasters. In the application, the continuous usage of this feature is not allowed.

  OCPH1, OCPH2 and OCPH3
  When DC/DC1, DC/DC2 and DC/DC3 high-side FET peak current cross the threshold, the high-side FET turns off immediately and this protection limits high-side FET ON time. When ON time is limited, the current of output is limited and the voltage of output decreases.

  OCPN1, OCPN2, OCPN3 (The incoming/sink over current.)
  When DC/DC1, DC/DC2 and DC/DC3 low-side FET peak negative current cross the threshold, the low-side FET turns off immediately and this protection limits low-side FET ON time.

- **Discharge Block at DC/DC2 and DC/DC3**
  When DC/DC control internal signal CTL2 or CTL3 is low, discharge block works.

Description of Blocks – continued

- **CONTROL LOGIC Block**

This block controls CTL1, CTL2, CTL3, and CTL4, ON/OFF sequence, PGOOD and each protection.
When the EN2 internal signal is high and UVLO_VCC and UVLO_VREG are released, CONTROL_LOGIC block is active.
When UVLO_VCC or UVLO_VREG is detected, CONTROL LOGIG Block will reset and initialize.
Output voltage and the sequence are decided by the combination of MODE pin (MODE0, MODE1 and MODE2) logic.
It is necessary to connect the MODE pins to VREG or GND. The following table is details of output voltage and ON/OFF sequences.

Table 1. Mode Setting Description

Mode name	MODE Pin *(Note 1)*			DCDC1 (VO1)	DCDC2 (VO2)	DCDC3 (VO3)	External LDO (VO4)	ON Sequence OFF Sequence	Protect
	2	1	0						
A-mode	L	L	L	3.3 V	1.2 V	1.8 V	2.7 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
B-mode	L	L	H	3.3 V	1.2 V	1.8 V	2.8 V	EN_LDO -> DCDC3 -> DCDC2 DCDC2 -> DCDC3 -> EN_LDO	Self-Restart
C-mode	L	H	L	3.3 V	1.2 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
D-mode	L	H	H	3.9 V	1.2 V	1.8 V	3.3 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
E-mode	H	L	L	3.3 V	1.1 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
F-mode	H	L	H	3.3 V	1.1 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Timer-Latch
G-mode	H	H	L	3.3 V	1.2 V	1.8 V	2.8 V	DCDC3 -> EN_LDO -> DCDC2 DCDC2 -> EN_LDO -> DCDC3	Self-Restart
H-mode	H	H	H	3.3 V	1.2 V	1.8 V	2.8 V	DCDC3 -> DCDC2 -> EN_LDO EN_LDO -> DCDC2 -> DCDC3	Self-Restart

(Note 1) L: GND short, H: VREG short

Description of Blocks - continued

- **CONTROL LOGIC Block (Protection of Self-Restart)**

When the EN pin is 0.8 V or less, IC is in the state of stand-by. In this state, the internal regulator and all outputs are off, and secondary DC/DC rails discharge function is active.
The following table shows the relation of protection (Self-Restart).

Table 2. Protection of Self-Restart

	Protection	PGOOD	Notice
ALL	UVLO_VCC	Low	All output is off.
	UVLO_VREG	Low	All output is off.
	UVLO_VS	Low	VO2, VO3 and EN_LDO are off.
	TSD	Low	All output is off.
DC/DC1 (VO1)	OCPH	Low*(Note 1)*	High side FET is off. Self-Restart after 10 ms.
	OCPN	-	Low side FET is off.
	VSOVP	Low	High and Low sides FET are off. Self-Restart after 10 ms.
	LVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
	OVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
DC/DC2 (VO2)	OCPH	Low*(Note 1)*	High side FET is off. Self-Restart after 10 ms.
	OCPN	-	Low side FET is off.
	LVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
	OVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
DC/DC3 (VO3)	OCPH	Low*(Note 1)*	High side FET is off Self-Restart after 10 ms.
	OCPN	-	Low side FET is off.
	LVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
	OVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
External LDO	LVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.
	OVD	Low	When more than 10 ms, all output is off. Self-Restart after 10 ms.

(Note 1) When protection detection is more than 10 ms, PGOOD turn into low.

Description of Blocks - continued

- **CONTROL LOGIC Block (Protection of Timer-Latch)**

When the protection detection passes for 10 ms (Typ) or more, “Timer-Latch” works and all output turns off and PGOOD turns to low. The cancellation method of “Timer-Latch” is to activate either UVLO_VCC, UVLO_VREG or TSD, or to turn EN low.
The following table shows the relation of protection (Timer-Latch).

Table 3. Protection of Timer-Latch

	Protection	PGOOD	Notice
ALL	UVLO_VCC	Low	All output is off. Release Timer-Latch
	UVLO_VREG	Low	All output is off. Release Timer-Latch
	UVLO_VS	Low	When protection detect 8 times, Timer-Latch works.
	TSD	Low	All output is off. Release Timer-Latch
DC/DC1 (VO1)	OCPH	Low*(Note 1)*	High side FET is off. Timer-Latch after 10 ms.
	OCPN	-	Low side FET is off.
	VSOVP	Low	High and Low sides FET are off Timer-Latch after 10 ms.
	LVD	Low	Timer-Latch after 10 ms.
	OVD	Low	Timer-Latch after 10 ms.
DC/DC2 (VO2)	OCPH	Low*(Note 1)*	High side FET is off. Timer-Latch after 10 ms.
	OCPN	-	Low side FET is off.
	LVD	Low	Timer-Latch after 10 ms.
	OVD	Low	Timer-Latch after 10 ms.
DC/DC3 (VO3)	OCPH	Low*(Note 1)*	High side FET is off. Timer-Latch after 10 ms.
	OCPN	-	Low side FET is off.
	LVD	Low	Timer-Latch after 10 ms.
	OVD	Low	Timer-Latch after 10 ms.
External LDO	LVD	Low	Timer-Latch after 10 ms.
	OVD	Low	When more than 10 ms, Timer-Latch works.

(Note 1) When protection detection is more than 10 ms, PGOOD turn into low.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage*(Note 1)*	V_{VCC}, V_{PVCC}	-0.3 to +20	V
EN Pin Voltage*(Note 2)*	V_{EN}	-0.3 to +20	V
Power Supply Voltage*(Note 1)*	V_{VS2}, V_{VS3}	-0.3 to +6	V
VO Pin Voltage	V_{VO1}, V_{VO2}, V_{VO3}	-0.3 to +6	V
FB_LDO Pin Voltage	V_{FBLDO}	-0.3 to +6	V
PGOOD Pin Voltage	V_{PGOOD}	-0.3 to +6	V
MODE Pin Voltage	V_{MODE0}, V_{MODE1}, V_{MODE2}	-0.3 to +6	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Do not exceed maximum junction temperature.

(Note 2) The VCC and EN pin start-up is sequence free if it is within guaranteed operating voltage range.

Thermal Resistance*(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
VQFN24FV4040				
Junction to Ambient	θ_{JA}	111.6	39.9	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	19	12	°C/W

(Note 3) Based on JESD51-2A (Still-Air)

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3.

(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notice
Power Supply Voltage*(Note 1)*	V_{VCC}	4.0*(Note 2)*	6.0	18.0	V	-
Power Supply Voltage*(Note 1)*	V_{VS2}, V_{VS3}	3.2	-	4.0	V	VS2 and VS3 must be short to VO1
Output Current*(Note 1)*	I_{VO1}	-	-	2	A	-
Output Current*(Note 1)*	I_{VO2}	-	-	1	A	-
Output Current*(Note 1)*	I_{VO3}	-	-	1	A	-
Switching Frequency	f_{OSC}	1.8	2.2	2.4	MHz	-
Operating Temperature	Topr	-40	+25	+125	°C	-

(Note 1) Do not exceed the maximum junction temperature rating.
(Note 2) If differences between Power Supply Voltage of VCC and VO1 Output Voltage are small, VO1 Output Voltage may drop.

Electrical Characteristics

(Unless otherwise specified,
Tj = -40 to +150 °C, V_{VCC} = V_{PVCC} = 4.0 V to 18.0 V, V_{VS2} = V_{VS3} = 3.2 V to 4.0 V, V_{EN} = 4.0 V, V_{SSCG} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Stand-by Current1	I_{STB1}	-	0	10	μA	Tj = 25 °C, V_{EN} = 0 V
Stand-by Current2	I_{STB2}	-	-	50	μA	Tj = 150 °C, V_{EN} = 0 V
Operating Current	I_{CC1}	-	3	6	mA	V_{VCC} = V_{PVCC} = 6.0 V, V_{VO1}, V_{VO2}, V_{VO3} and V_{LDO_FB} is setting voltage x 1.1
VCC UVLO Operating Voltage	$V_{UVLOVCC\_ON}$	3.30	3.45	3.60	V	VCC pin voltage
VCC UVLO Hysteresis Voltage	$V_{UVLOVCC\_HYS}$	300	350	400	mV	VCC pin voltage
VREG Output Voltage	V_{REG}	-	4.9	-	V	VCC = 5.0 V to 18 V
VREG UVLO Operating Voltage	$V_{UVLOVREG\_ON}$	2.71	2.98	3.25	V	VREG pin voltage
VREG UVLO Release Voltage	$V_{UVLOVREG\_OFF}$	-	3.10	3.44	V	VREG pin voltage
VS UVLO Operating Voltage	V_{UVLOVS_ON}	2.42	2.65	2.88	V	VS2 pin voltage
VS UVLO Release Voltage	V_{UVLOVS_OFF}	-	2.75	3.05	V	VS2 pin voltage
Switching Frequency1	f_{OSC1}	2.0	2.2	2.4	MHz	R_{RT} = 27 kΩ, V_{SSCG} = 0 V
Switching Frequency2	f_{OSC2}	1.8	2.1	f_{OSC1}	MHz	R_{RT} = 27 kΩ C_{SSC} = 3300 pF

Electrical Characteristics - continued

(Unless otherwise specified,
Tj = -40 to +150 °C, V_{VCC} = V_{PVCC} = 4.0 V to 18.0 V, V_{VS2} = V_{VS3} = 3.2 V to 4.0 V, V_{EN} = 4.0 V, V_{SSCG} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<CH1 Output, Primary DC/DC1>						
VO1 Output Voltage Accuracy	V_{VO1}	-2.0	-	+2.0	%	-
VO1 Input Current	I_{VO1_CUR}	4.0	7.3	13.0	µA	V_{VO1} = 3.9 V
VO1 LVD Operating Voltage	V_{LVD11}	VO1 x 0.73	VO1 x 0.80	VO1 x 0.87		VO1 pin voltage
VO1 LVD Release Voltage	V_{LVD12}	-	VO1 x 0.86	-		VO1 pin voltage
VO1 OVD Operating Voltage	V_{OVD11}	VO1 x 1.10	VO1 x 1.20	VO1 x 1.30	V	VO1 pin voltage
VO1 OVD Release Voltage	V_{OVD12}	-	VO1 x 1.15	-	V	VO1 pin voltage
VS OVP Operating Voltage	V_{VSOVP_ON}	5.1	5.5	5.9	V	VS3 pin voltage
VS OVP Release Voltage	V_{VSOVP_OFF}	4.95	5.35	5.75	V	VS3 pin voltage
High Side FET ON Resistance 1	$R_{ONH\_SW1\_1}$	-	200	350	mΩ	I_{SW1} = -20 mA 5.0 V ≤ V_{VCC} ≤ 18 V
Low Side FET ON Resistance 1	$R_{ONL\_SW1\_1}$	-	200	350	mΩ	I_{SW1} = +20 mA 5.0 V ≤ V_{VCC} ≤ 18 V
High Side FET ON Resistance 2	$R_{ONH\_SW1\_2}$	-	250	400	mΩ	I_{SW1} = -20 mA 4.0 V ≤ V_{VCC} < 5.0 V
Low Side FET ON Resistance 2	$R_{ONL\_SW1\_2}$	-	250	400	mΩ	I_{SW1} = +20 mA 4.0 V ≤ V_{VCC} < 5.0 V
<CH2 Output, Secondary DC/DC2>						
VO2 Output Voltage Accuracy	V_{VO2}	-2.0	-	+2.0	%	
VO2 Input Current	I_{VO2_CUR}	-	1.8	2.8	µA	V_{VO2} = 1.2 V
VO2 LVD Operating Voltage	V_{LVD21}	VO2 x 0.73	VO2 x 0.80	VO2 x 0.87	V	VO2 pin voltage
VO2 LVD Release Voltage	V_{LVD22}	-	VO2 x 0.86	-	V	VO2 pin voltage
VO2 OVD Operating Voltage	V_{OVD21}	VO2 x 1.1	VO2 x 1.2	VO2 x 1.3	V	VO2 pin voltage
VO2 OVD Release Voltage	V_{OVD22}	-	VO2 x 1.15	-	V	VO2 pin voltage
High Side FET ON Resistance	R_{ONH_SW2}	-	220	390	mΩ	I_{SW2} = -20 mA
Low Side FET ON Resistance	R_{ONL_SW2}	-	190	330	mΩ	I_{SW2} = +20 mA
VO2 Discharge Resistance	R_{VO2DIS}	-	150	400	Ω	I_{SW2} = +1 mA

Electrical Characteristics - continued

(Unless otherwise specified,
Tj = -40 to +150 °C, V_{VCC} = V_{PVCC} = 4.0 V to 18.0 V, V_{VS2} = V_{VS3} = 3.2 V to 4.0 V, V_{EN} = 4.0 V, V_{SSCG} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<CH3 Output, Secondary DC/DC3>						
VO3 Output Voltage Accuracy	V_{VO3}	-2.0	-	+2.0	%	
VO3 Input Current	I_{VO3_CUR}	-	2.5	3.9	µA	V_{VO3} = 1.8 V
VO3 LVD Operating Voltage	V_{LVD31}	VO3 x 0.73	VO3 x 0.80	VO3 x 0.87	V	VO3 pin voltage
VO3 LVD Release Voltage	V_{LVD32}	-	VO3 x 0.86	-	V	VO3 pin voltage
VO3 OVD Operating Voltage	V_{OVD31}	VO3 x 1.1	VO3 x 1.2	VO3 x 1.3	V	VO3 pin voltage
VO3 OVD Release Voltage	V_{OVD32}	-	VO3 x 1.15	-	V	VO3 pin voltage
High Side FET ON Resistance	R_{ONH_SW3}	-	220	390	mΩ	I_{SW3} = -20 mA
Low Side FET ON Resistance	R_{ONL_SW3}	-	190	330	mΩ	I_{SW3} = +20 mA
VO3 Discharge Resistance	R_{VO3DIS}	-	150	400	Ω	I_{SW3} = +1 mA
<CH4 Operating, Secondary LDO_CNT>						
FB_LDO Input Current	I_{FBLDO_CUR}	2.0	4.4	6.8	µA	V_{FB_LDO} = 3.3 V
VO4 LVD Operating Voltage	V_{LVD41}	VO4 x 0.89	VO4 x 0.92	VO4 x 0.95	V	FB_LDO pin voltage
VO4 LVD Release Voltage	V_{LVD42}	-	VO4 x 0.94	-	V	FB_LDO pin voltage
VO4 OVD Operating Voltage	V_{OVD41}	VO4 x 1.045	VO4 x 1.080	VO4 x 1.115	V	FB_LDO pin voltage
VO4 OVD Release Voltage	V_{OVD42}	-	VO4 x 1.06	-	V	FB_LDO pin voltage
<PGOOD Output>						
PGOOD Resistance	R_{ON_PG}	-	-	250	Ω	I_{PGOOD} = +1 mA
PGOOD Delay Time	t_{PGOOD}	8.5	10.0	11.5	ms	f_{OSC2} = 2.1 MHz
<Others>						
EN1 Threshold Voltage	V_{TH_EN1}	0.8	1.7	2.6	V	For VREG
EN2 Threshold Voltage	V_{TH_EN2}	1.5	1.7	2.6	V	For output
EN Input Current	I_{EN}	5	25	45	µA	V_{EN} = 5 V
EN_LDO High Side Resistance	R_{ON1_ENLDO}	-	-	200	Ω	I_{EN_LDO} = -1 mA
EN_LDO Low Side Resistance	R_{ON2_ENLDO}	-	-	200	Ω	I_{EN_LDO} = +1 mA

Typical Performance Curves

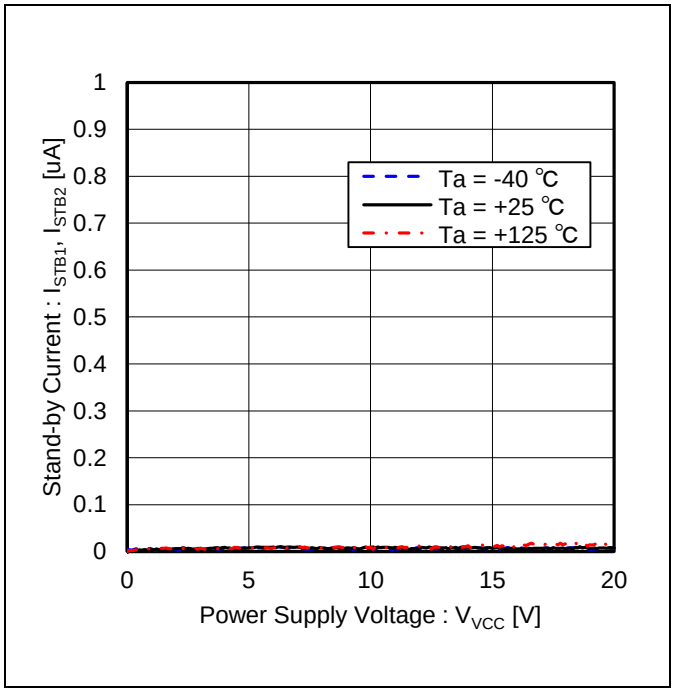


Figure 1. Stand-by Current vs Power Supply Voltage

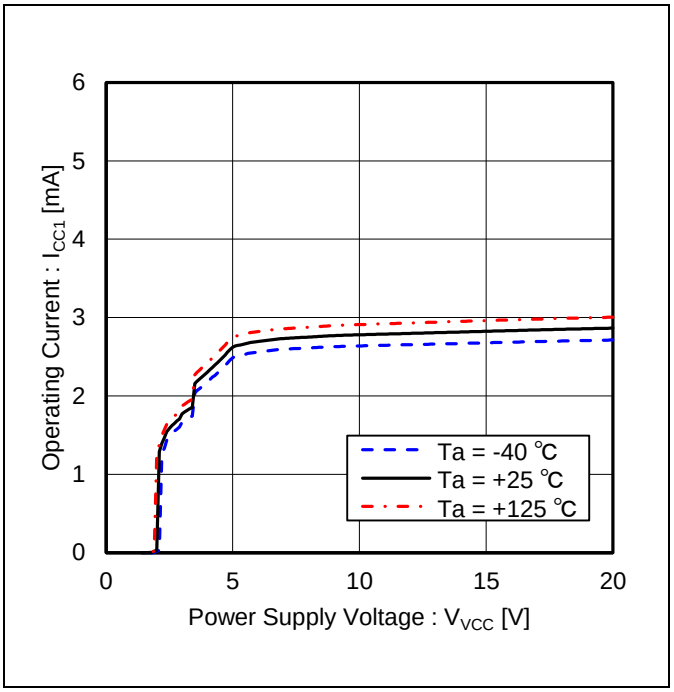


Figure 2. Operating Current vs Power Supply Voltage

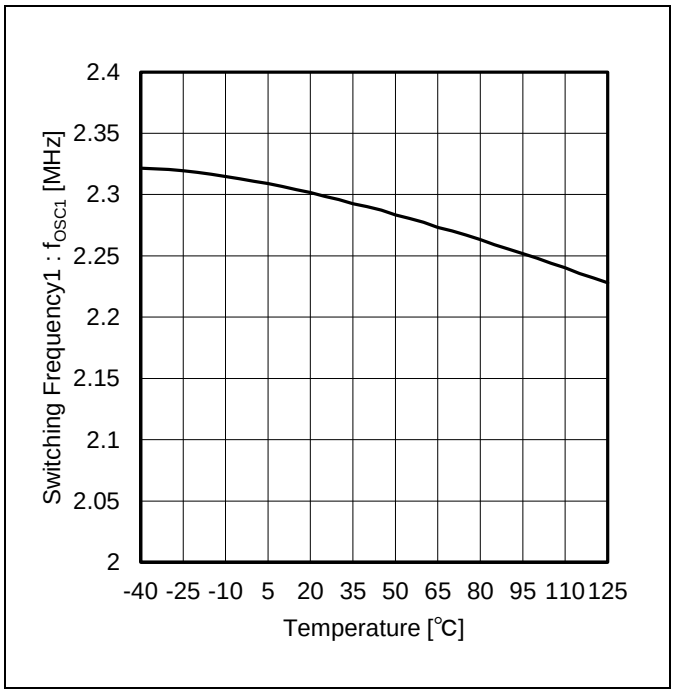


Figure 3. Switching Frequency1 vs Temperature
(R_{RT} = 27 kΩ, SSCG = GND)

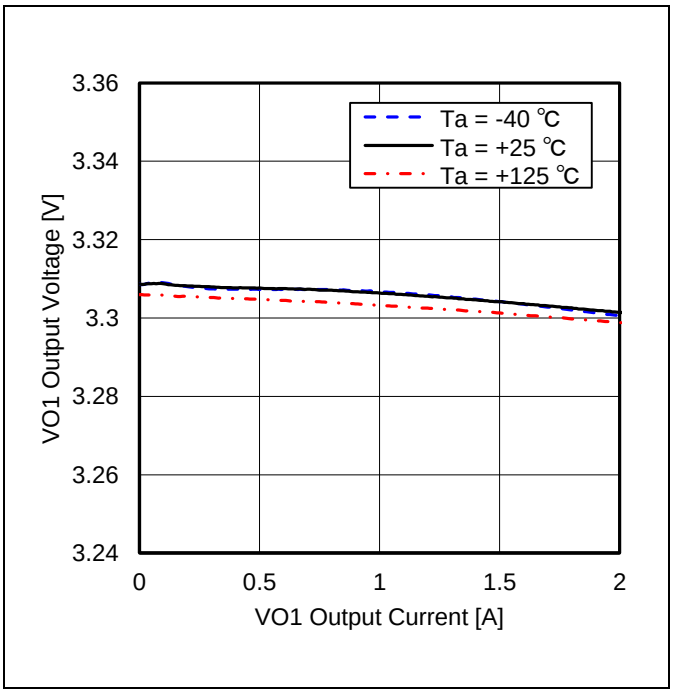


Figure 4. VO1 Output Voltage vs VO1 Output Current
(VO1 Load Regulation)

Typical Performance Curves – continued

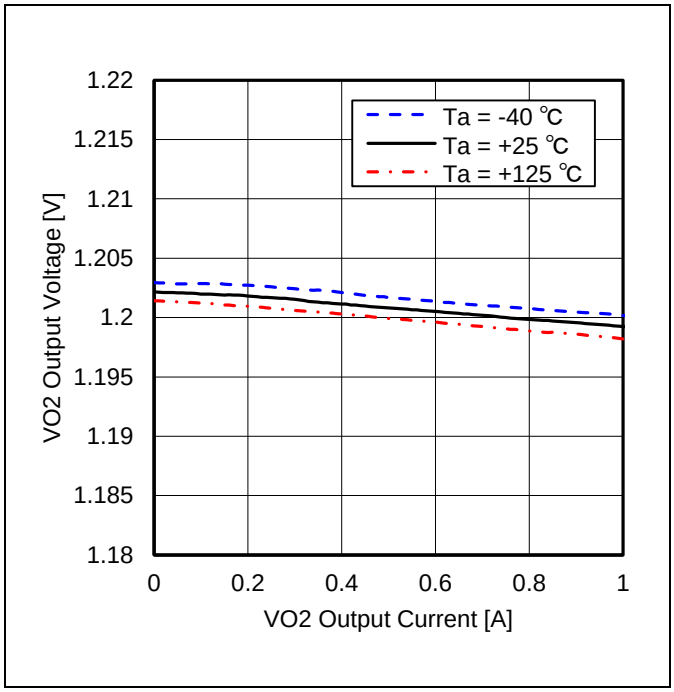


Figure 5. VO2 Output Voltage vs VO2 Output Current
(VO2 Load Regulation)

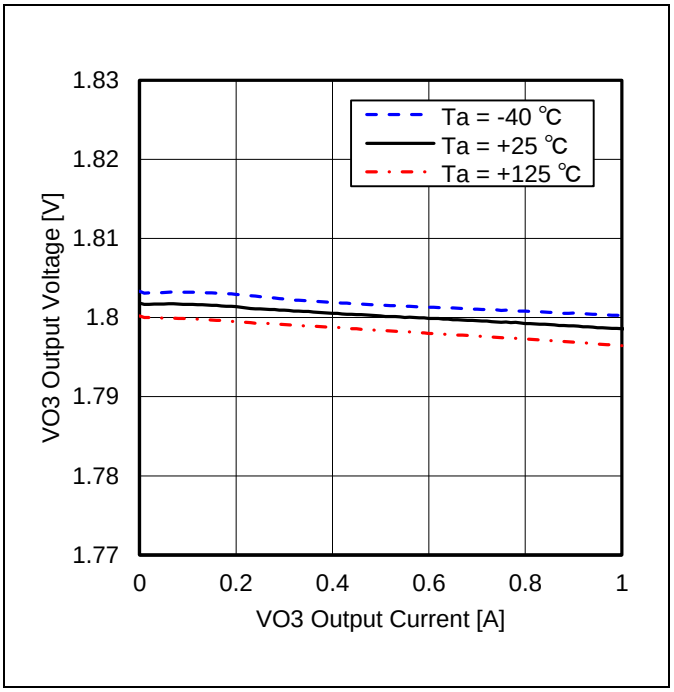


Figure 6. VO3 Output Voltage vs VO3 Output Current
(VO3 Load Regulation)

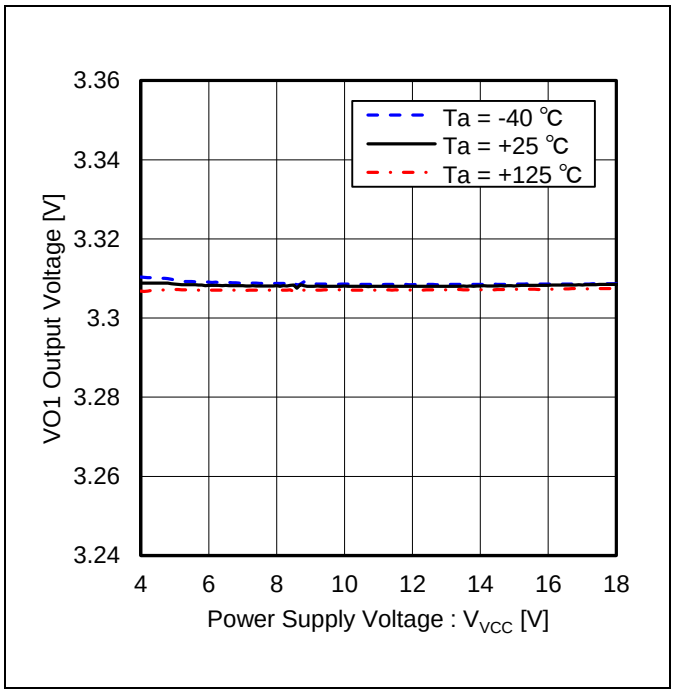


Figure 7. VO1 Output Voltage vs Power Supply Voltage
(VO1 Line Regulation)

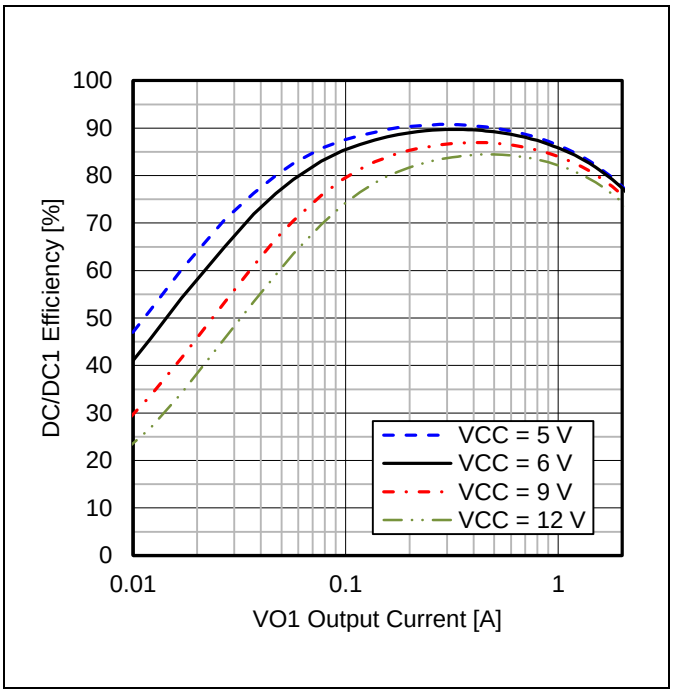


Figure 8. DC/DC1 Efficiency vs VO1 Output Current
(VO1 = 3.3 V)

Typical Performance Curves – continued

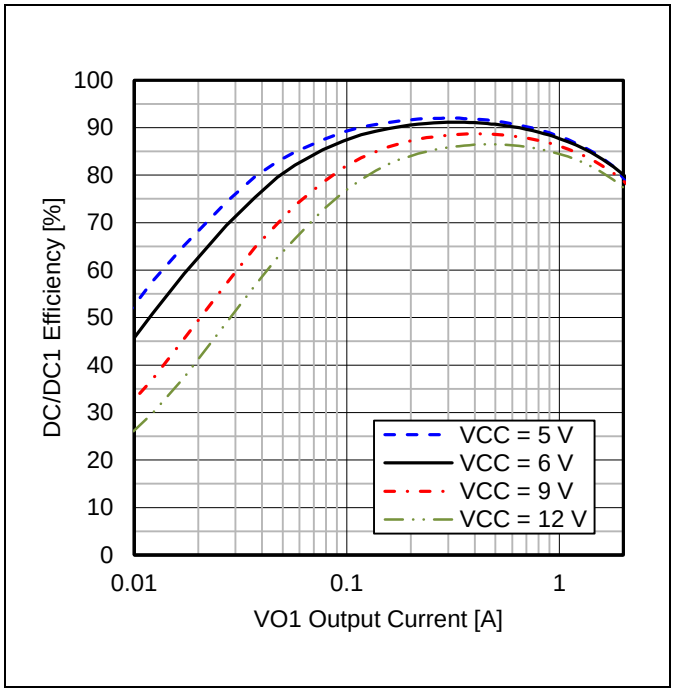


Figure 9. DC/DC1 Efficiency vs VO1 Output Current
(VO1 = 3.9 V)

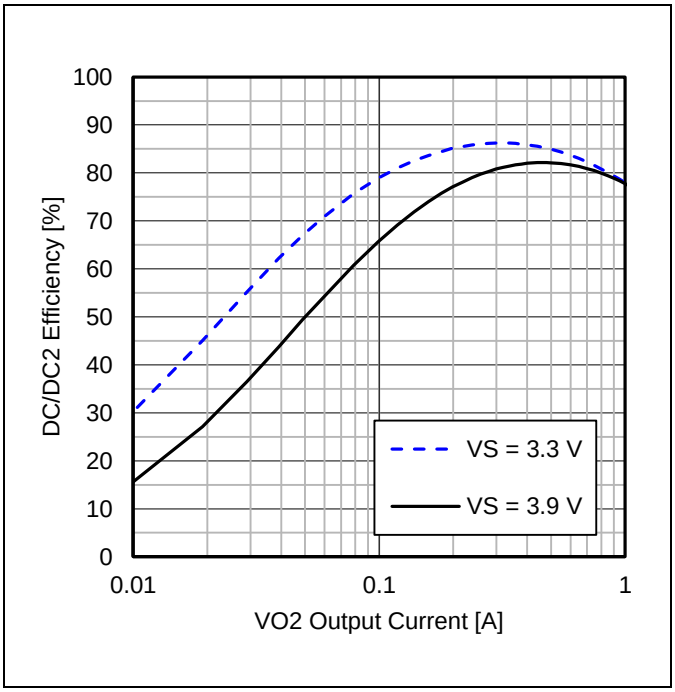


Figure 10. DC/DC2 Efficiency vs VO2 Output Current
(VO2 = 1.2 V)

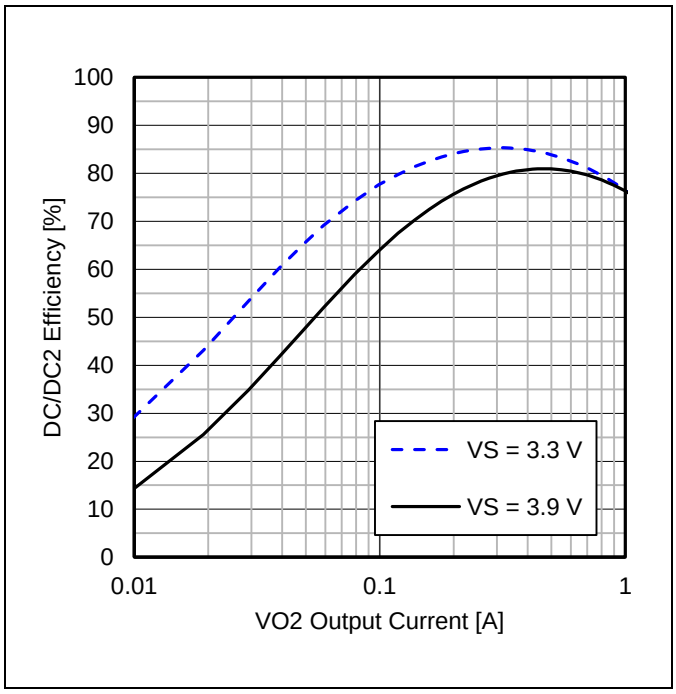


Figure 11. DC/DC2 Efficiency vs VO2 Output Current
(VO2 = 1.1 V)

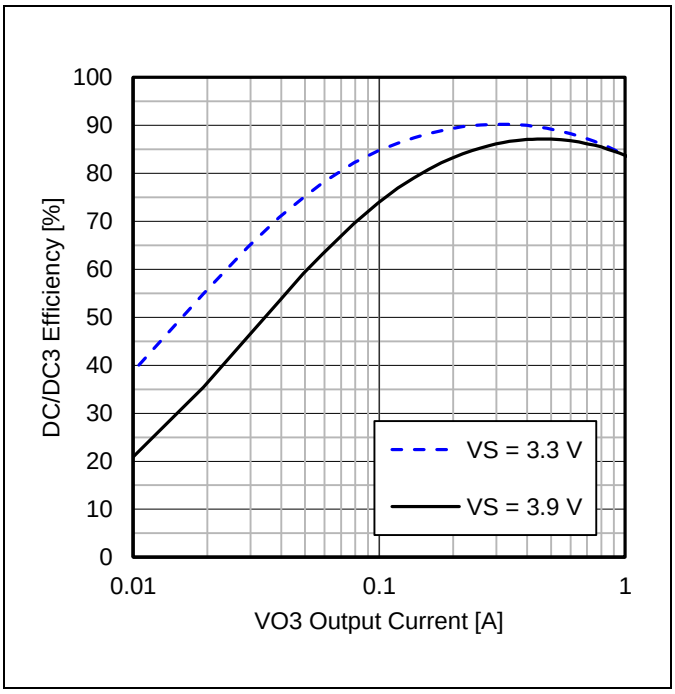


Figure 12. DC/DC3 Efficiency vs VO3 Output Current
(VO3 = 1.8 V)

Typical Performance Curves – continued

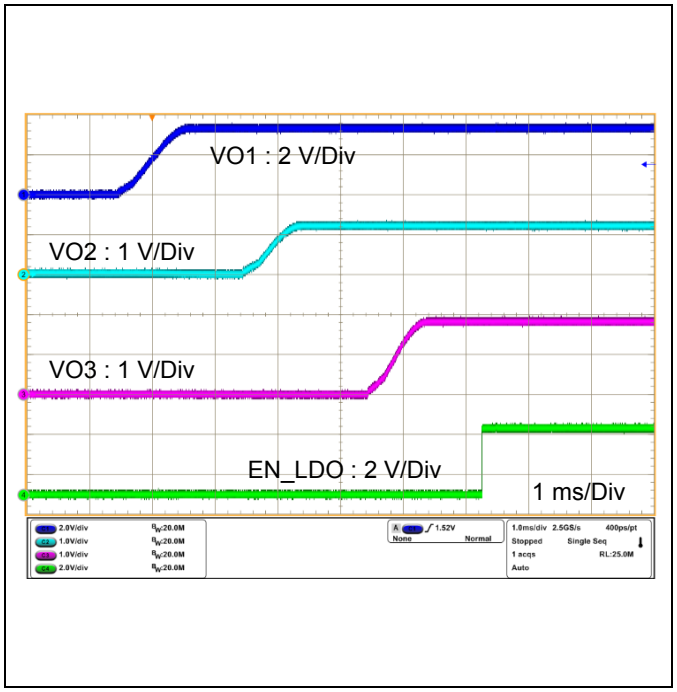


Figure 13. Start-up Waveform
(A-MODE)

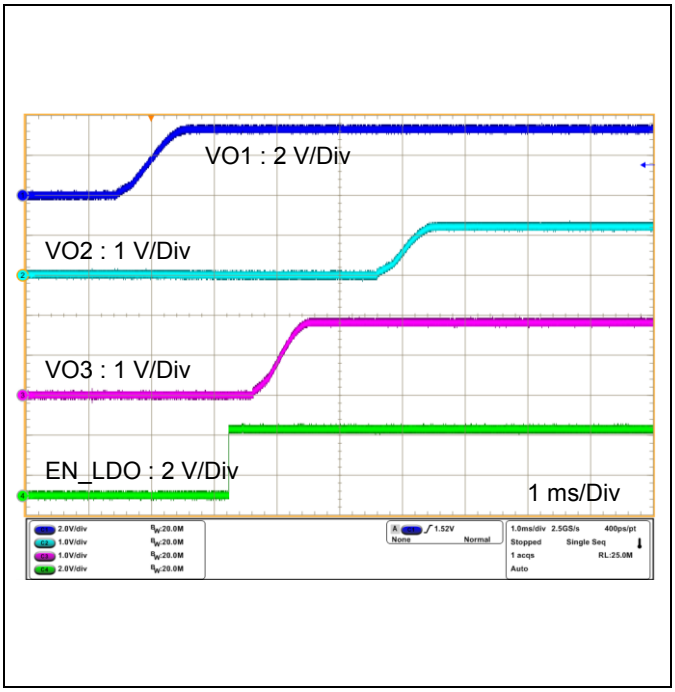


Figure 14. Start-up Waveform
(B-MODE)

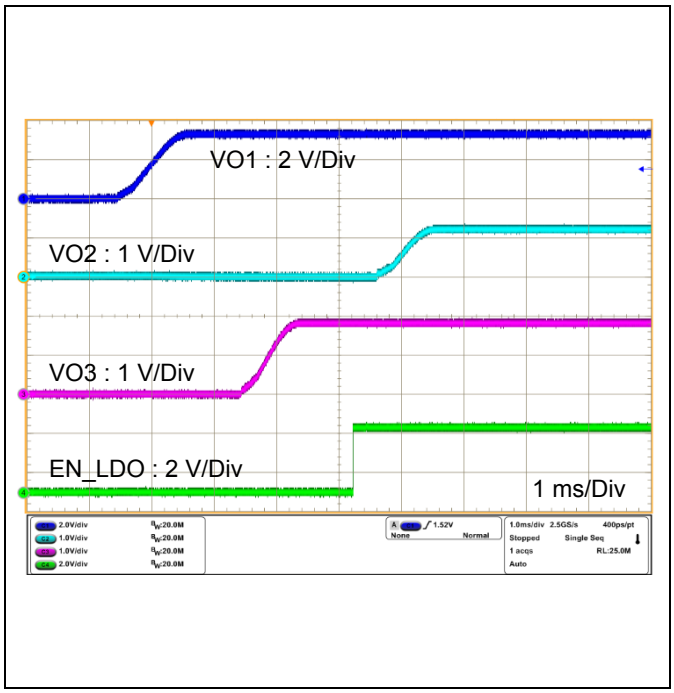


Figure 15. Start-up Waveform
(G-MODE)

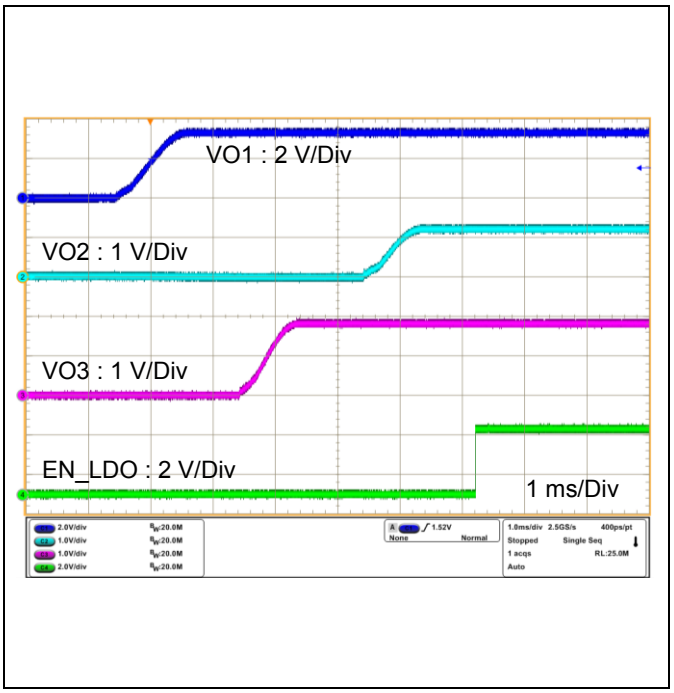


Figure 16. Start-up Waveform
(H-MODE)

Function Explanations

Timing Chart of Start and Stop using EN (A, C, D, E, F-mode)

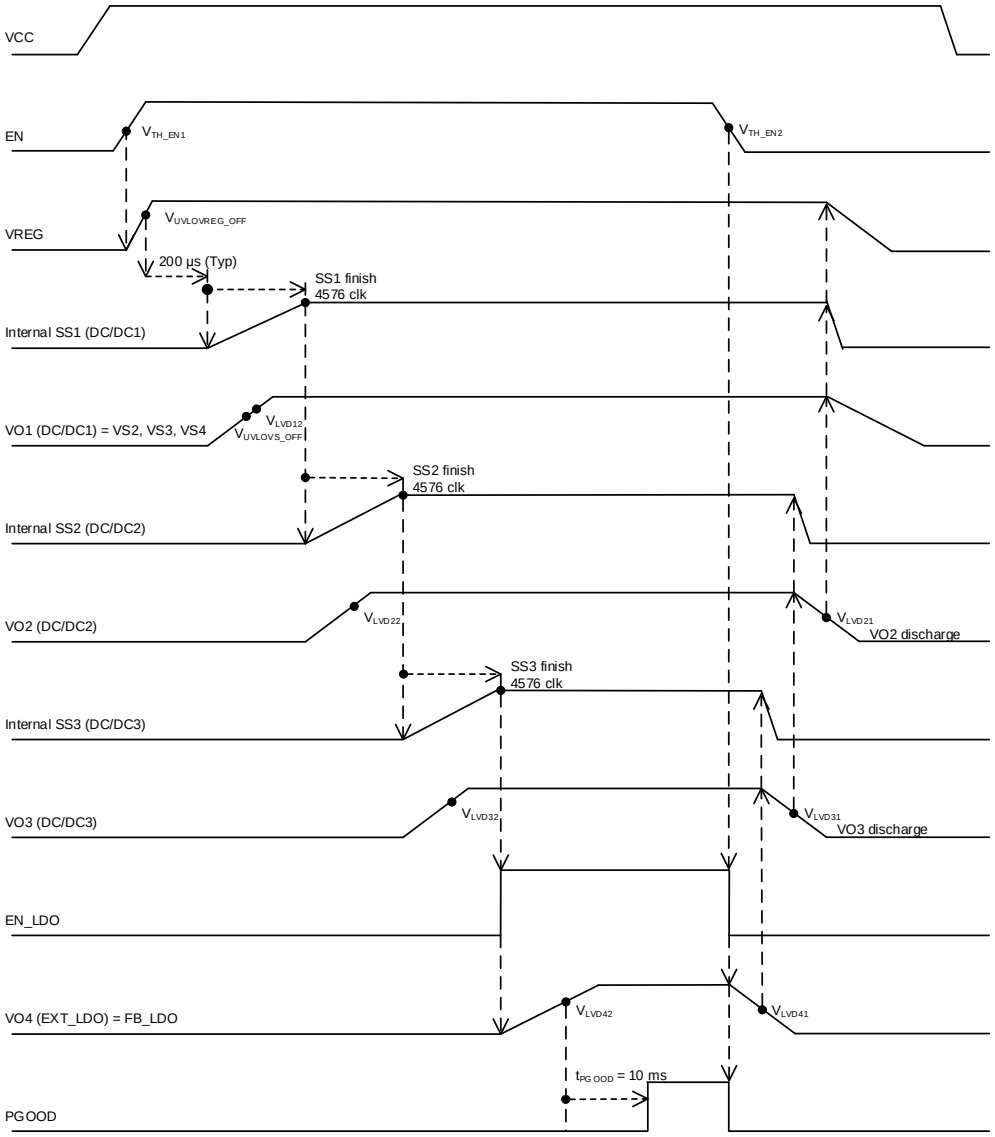


Figure 17. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
4. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
5. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
6. Wait 10 ms (Typ) -> PGOOD is up (released). The “10 ms” time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low and EN_LDO low -> VO4 (External LDO) falls.
2. LVD4 power bad or 10 ms (Typ) after EN low input -> stop VO3 (DC/DC3) operation and start discharging VO3.
3. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO2 (DC/DC2) operation and start discharging VO2.
4. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The “10 ms” time depends on f_{OSC2}.

Function Explanations – continued

Timing Chart of Start and Stop using VCC ULVO (A, C, D, E, F-mode)

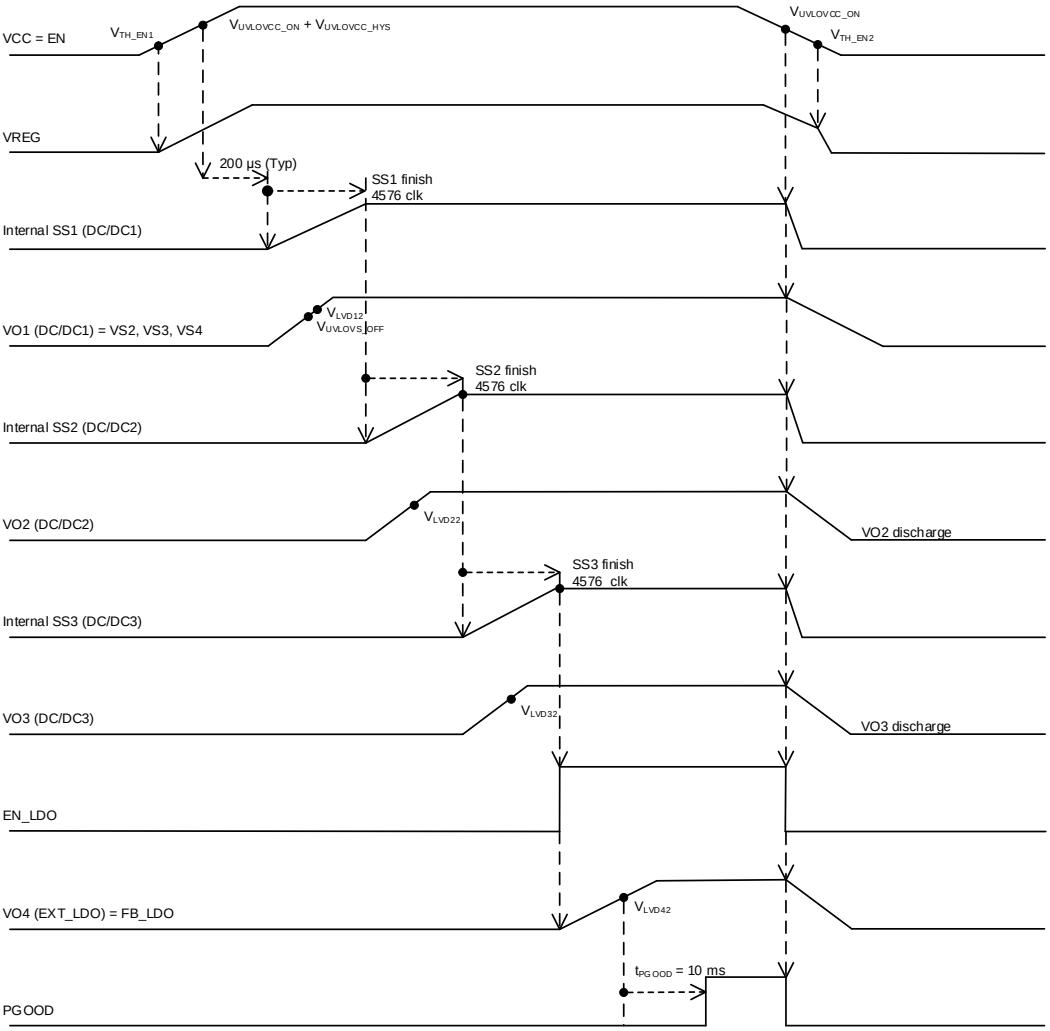


Figure 18 .Timing Chart (using VCC UVLO)

Output power up sequence

1. VCC (EN) reaches its UVLO threshold -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
4. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
5. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
6. Wait 10 ms (Typ) -> PGOOD is up (released). The “10 ms” time depends on f_{OSC2}.
7. PGOOD operation is dependent on conditions of LVD1 to 4.

Output power down sequence

1. VCC (EN) falls and crosses its falling UVLO threshold
2. PGOOD becomes low and stops operation of all outputs (VO1 to VO4) including the internal regulator (VREG).
3. Start discharging VO2 and VO3.

Function Explanations – continued

Timing Chart of Start and Stop using EN (B-mode)

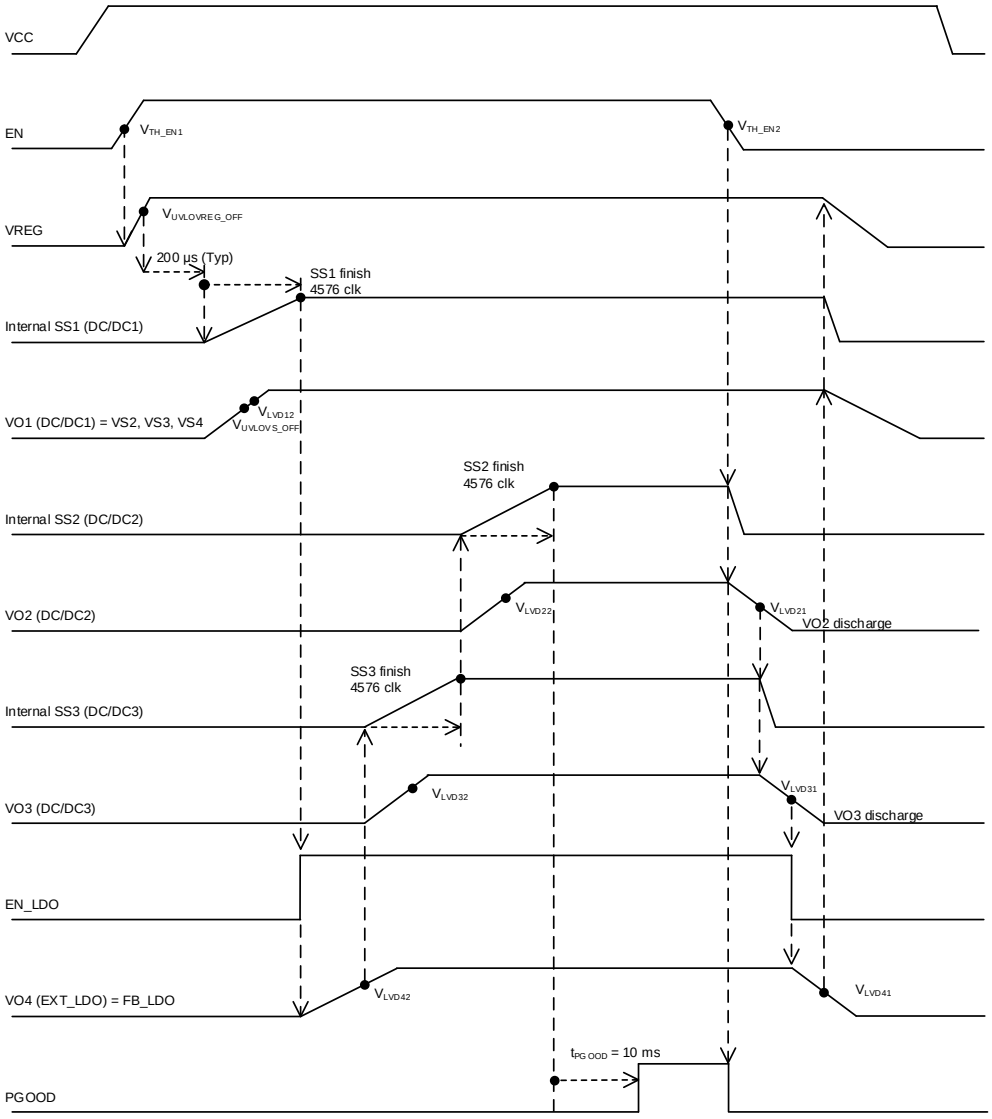


Figure 19. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
4. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
5. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
6. Wait 10 ms (Typ) -> PGOOD is up (released). The “10 ms” time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low -> stop VO2 (DC/DC2) operation and discharging VO2.
2. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO3 (DC/DC3) operation and start discharging VO3.
3. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> VO4 (External LDO) falls.
4. LVD4 power bad or 10 ms (Typ) after EN_LDO low -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The “10 ms” time depends on f_{OSC2}.

Function Explanations – continued

Timing Chart of Start and Stop using EN (G-mode)

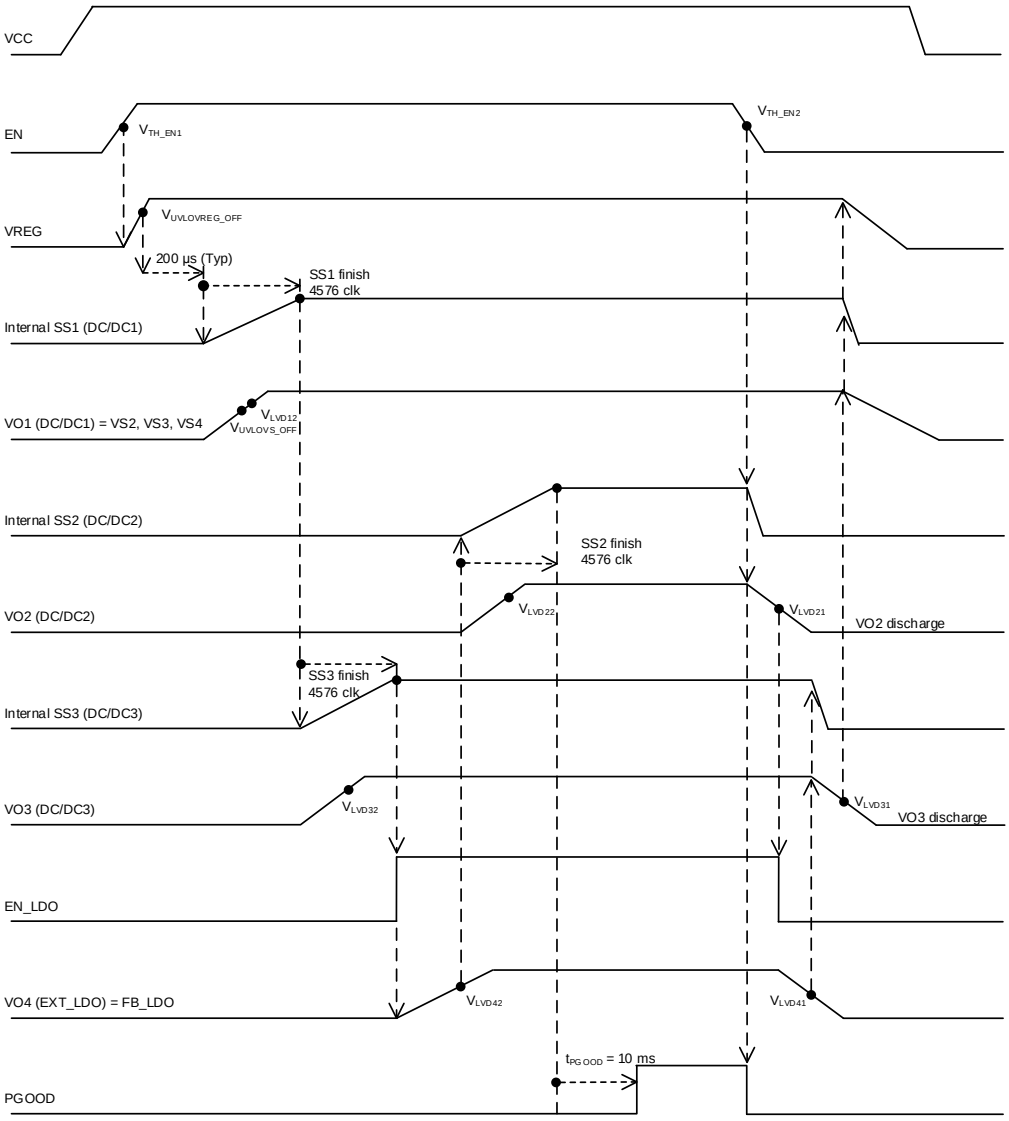


Figure 20. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
4. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
5. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
6. Wait 10 ms (Typ) -> PGOOD is up (released). The “10 ms” time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low -> stop VO2 (DC/DC2) operation and discharging VO2.
2. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> VO4 (External LDO) falls.
3. LVD4 power bad or 10 ms (Typ) after EN_LDO low -> stop VO3 (DC/DC3) operation and start discharging VO3.
4. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The “10 ms” time depends on f_{OSC2}.

Function Explanations – continued

Timing Chart of Start and Stop using EN (H-mode)

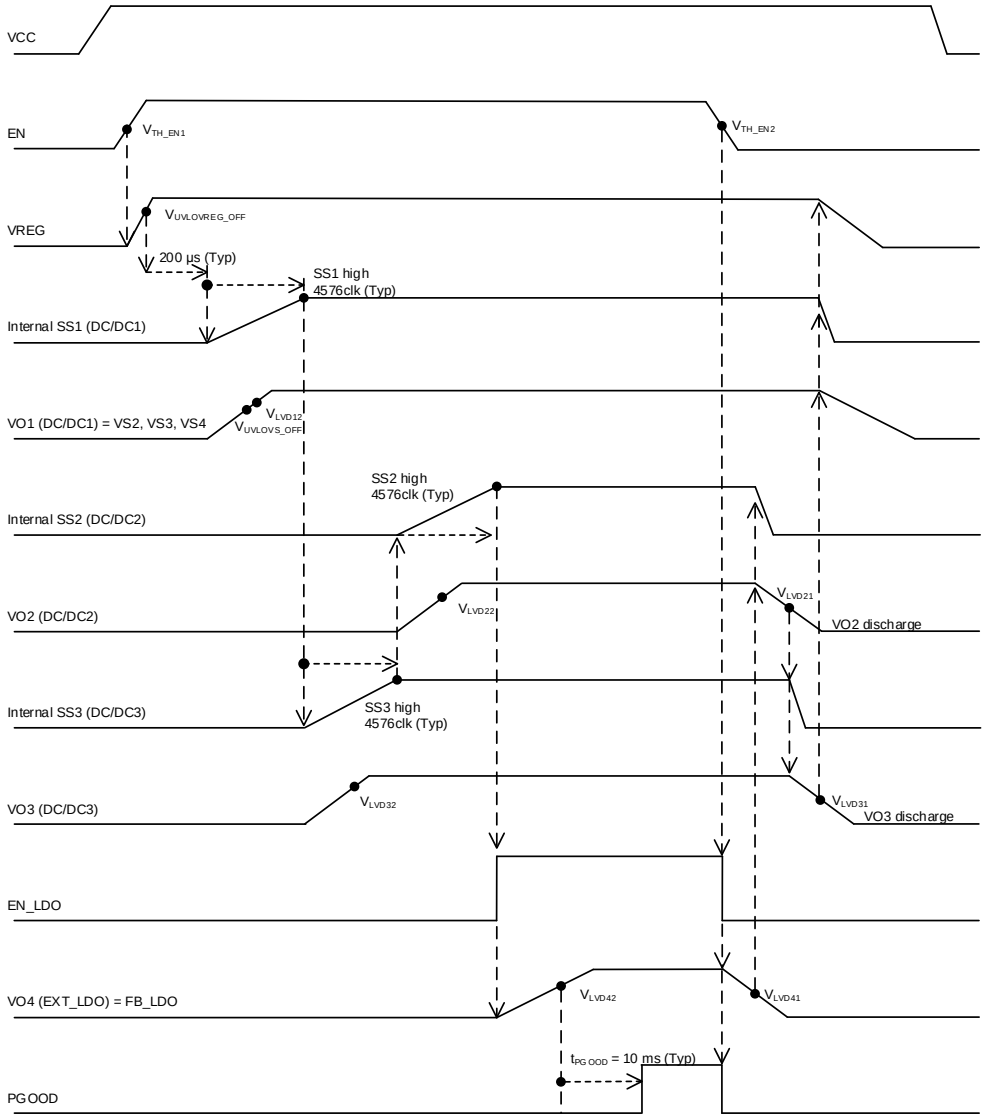


Figure 21. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
4. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
5. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
6. Wait 10 ms (Typ) -> PGOOD is up (released). The “10 ms” time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low and EN_LDO low -> VO4 (External LDO) falls.
2. LVD4 power bad or 10 ms (Typ) after EN low input -> stop VO2 (DC/DC2) operation and start discharging VO2.
3. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO3 (DC/DC3) operation and start discharging VO3.
4. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The “10 ms” time depends on f_{OSC2}.

Application Examples

1. Caution on PCB Layout

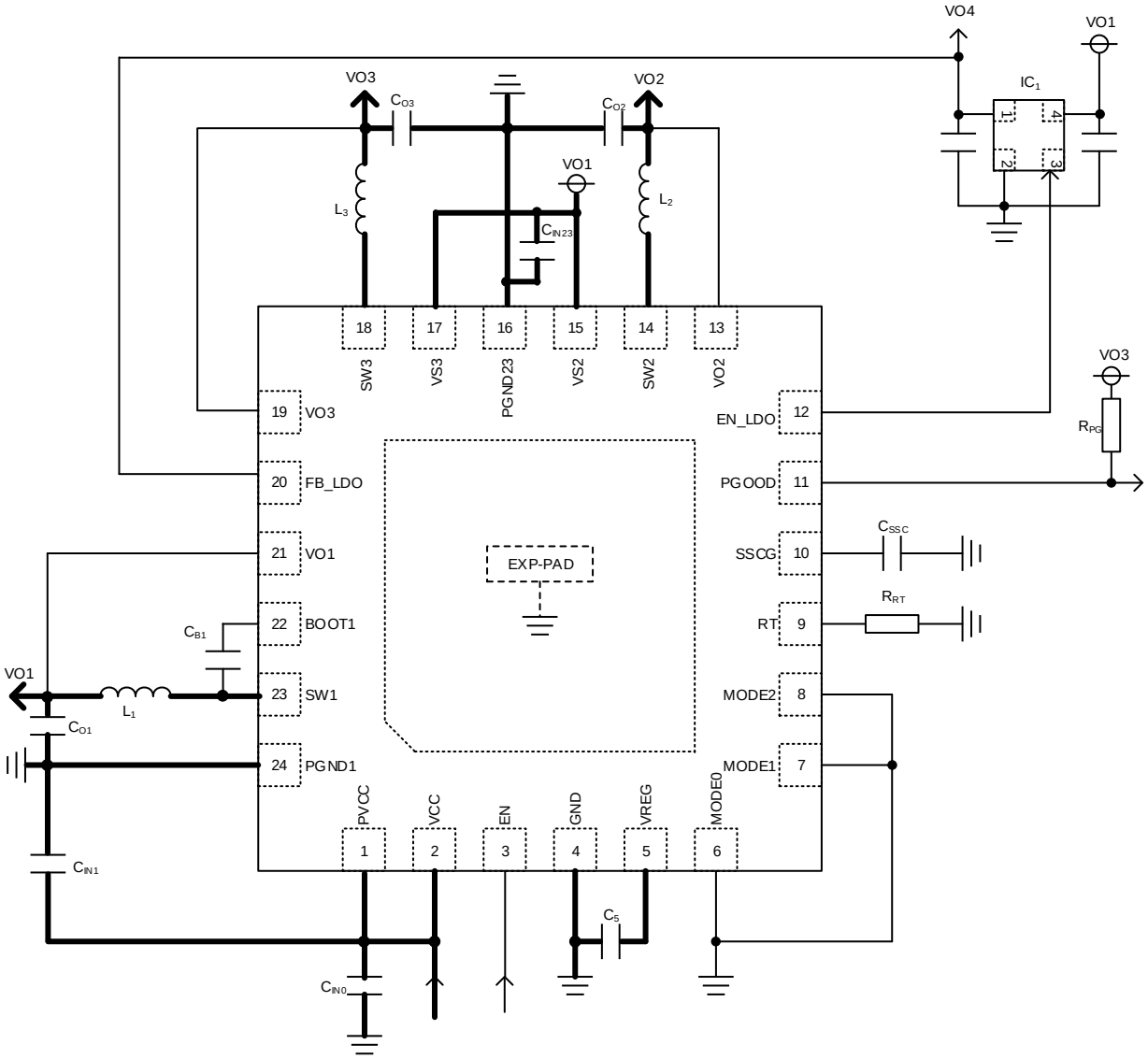
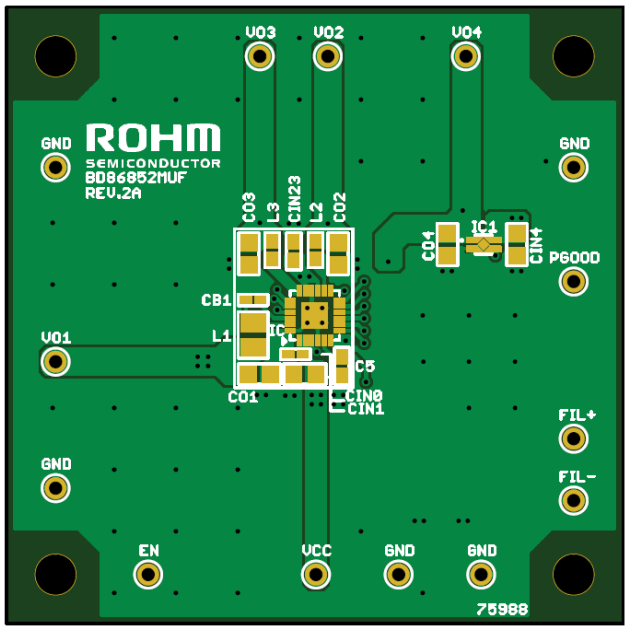


Figure 22.Circuits Example

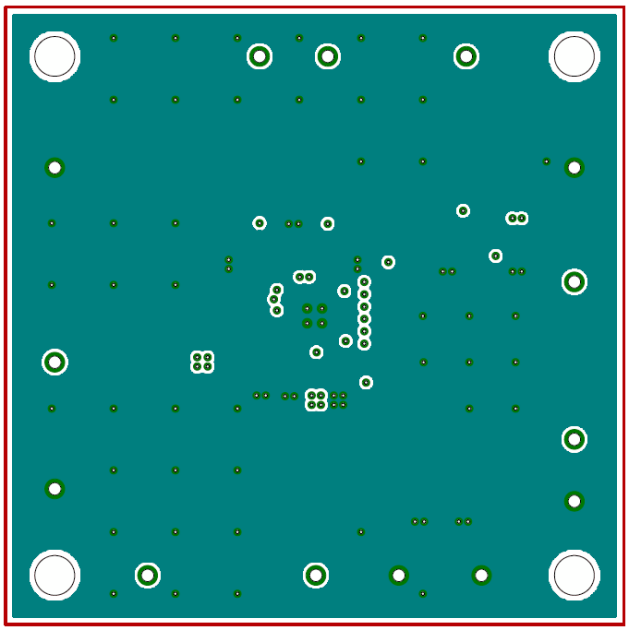
I. Connect line in bold as short as possible with wide pattern.
II. Place input capacitor C_{IN0}, C_{IN1}, C_{IN23} and C_5 close to IC as much as possible.
Especially distance between C_{IN0} and IC must be connected in top layer not through via.
III. Place C_{SSC} and R_{RT} near IC as much as possible.
IV. Sense line of VO1, VO2, VO3 and FB_LDO must be placed far from L_1, L_2 and L_3 as much as possible.
V. Connect all GND pin (GND, PGND1 and PGND23) and EXP-PAD as short as possible in top layer.
VI. Connect EXP-PAD directly to the GND pin.

1. **Caution on PCB Layout – continued**

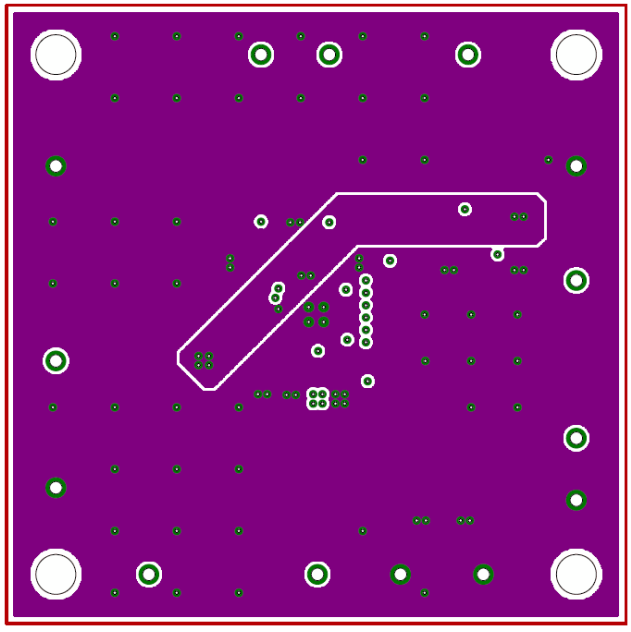
Top Layer



2nd Layer



3rd Layer



Bottom Layer

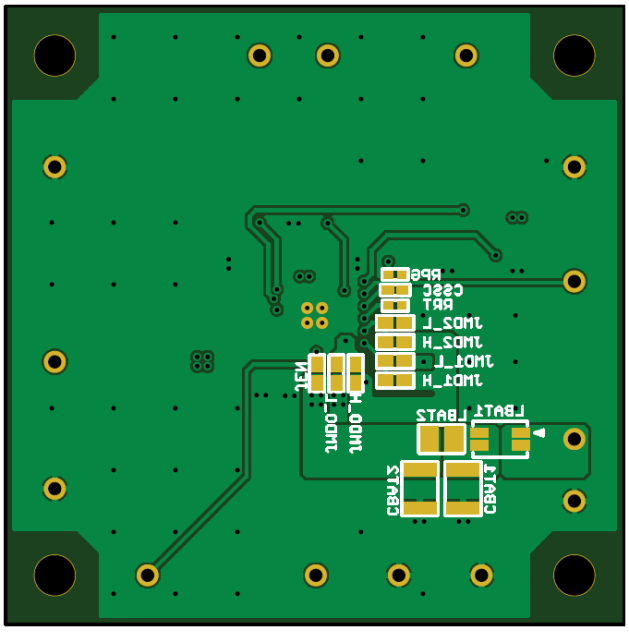


Figure 23. Recommendation Layout Pattern

Application Examples – continued

2. Selection of Components Externally Connected

2.1 Selection of the Inductor L (L_1, L_2 and L_3)

When the switching regulator supplies current continuously to the load, the LC filter is necessary to smooth the output voltage. The inductor ripple current ΔIL that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple also becomes small.
Refer to "Circuit Example" for the recommended inductors.
Maximum ΔI_L is shown in the following equation.

$$\Delta I_L = \frac{\left(V_{VCC(MAX)} - V_{VO}\right) \times V_{VO}}{L \times V_{VCC(MAX)} \times f_{SW}} \text{ [A]}$$

Where:
$V_{VCC(MAX)}$ is the maximum input voltage. DC/DC1 is PVCC, DC/DC2 is VS2, and DC/DC3 is VS3.
f_{SW} is switching frequency.
L is the value of inductor.

It contributes to the miniaturization of the application if the inductance value is small. The disadvantages are the increase in the voltage of output ripple. It contributes to the small voltage of the output ripple if the inductance value is large. The disadvantages are the increase in the size of inductor.

The maximum output electric current is limited to the overcurrent protection working current as shown in the following equation.

$$I_{o(MAX)} = I_{SW(MAX)} + \frac{\Delta I_L}{2} \text{ [A]}$$

Where:
$I_{O(MAX)}$ is the maximum output current.
$I_{SW(MAX)}$ is the maximum SW load current.

2.2 Selection of the Output Capacitor CO (C_{O1}, C_{O2}, C_{O3})

The voltage of output ripple ΔVPP is shown in the following equation.

$$\Delta V_{PP} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_O \times f_{SW}}\right) \text{ [V]}$$

Where:
R_{ESR} is the equivalent series resistance of output capacitor.
C_O is the value of output capacitor.

ΔVPP can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. Confirm frequency characteristic of ESR from the datasheet of the manufacturer, and consider ESR value to be low in the switching frequency being used. It is necessary to consider the ceramic capacitor, because the DC biasing characteristic is remarkable. By selecting these high voltage ratings, it is possible to reduce the influence of DC bias characteristics.
Refer to "Circuit Example" for the recommended output capacitors.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation must not exceed the ratings ripple current.

$$I_{(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \text{ [A]}$$

Where :
R_{ESR} is the equivalent series resistance of output capacitor.
C_O is the value of output capacitor.

2. Selection of Components Externally Connected – continued

2.3 Selection of the Output Capacitor C_5

A ceramic capacitor is needed for the internal regulator VREG pin. Moreover, in order to maintain good temperature characteristics, the one with the X7R characteristic or better is recommended. The voltage rating is recommended to 3 times or more the output voltage. Refer to "Circuit Example" for the recommended output capacitor.

2.4 Selection of Input Capacitor C_{IN} (C_{IN0}, C_{IN1}, C_{IN23})

The input capacitor is usually required for two types of decoupling capacitors, the C_{IN} and the bulk capacitors. Ceramic capacitors are effective by being placed as close as possible to the VCC (PVCC, VS2 and VS3) pin and the GND (PGND1 and PGND23) pin. Voltage rating is recommended to 1.2 times or more the maximum input voltage.
Refer to "Circuit Example" for the recommended input capacitors. Also, the IC might not function properly when the PCB layout or the position of the capacitor is not good. Refer to "Caution on PCB Layout".

The bulk capacitor is an option. The bulk capacitor prevents the decrease in the line voltage and serves a backup power supply to keep the input potential constant. The RMS value of the input ripple electric current is obtained in the following equation. In that case, consider not to exceed the rated ripple current of the capacitor. The RMS value of the input ripple electric current is obtained in the following equation.

$$I_{VCC(RMS)} = \sqrt{\frac{V_{VO}}{V_{VCC}} \times \left\{ I_O^2 \times \left(1 - \frac{V_{VO}}{V_{VCC}}\right) + \frac{\Delta I_L^2}{12} \right\}} \text{ [A]}$$

Where:
$I_{VCC(RMS)}$ is the RMS value of the input ripple electric current.
V_{VCC} is the input voltage. DC/DC1 is PVCC, DC/DC2 is VS2, and DC/DC3 is VS3.
V_{VO} is the output voltage. DC/DC1 is VO1, DC/DC2 is VO2, and DC/DC3 is VO3.

2.5 Selection of Capacitor C_{B1}

The C_{B1} is the capacitor between the BOOT1 pin and the SW1 pin for bootstrapping. The voltage of the C_{B1} and SW1 is same as VREG. The recommended capacitor type is a ceramic capacitor. The CB1 must be set to 47 nF. Moreover, the X7R or better capacitor is recommended.

2.6 Selection of Resistor at the EN Pin

The EN pin node potentially have unexpected short to VCC or GND on the assumption of accidental foreign objects that physically shorts pin-to-pin. The resistor in series to the EN pin can minimize the fatal damage for the external components. If the destructive damage is expected by the external components, use the resistor in series to the EN pin to limit the current. The resistance is 20 kΩ or less.

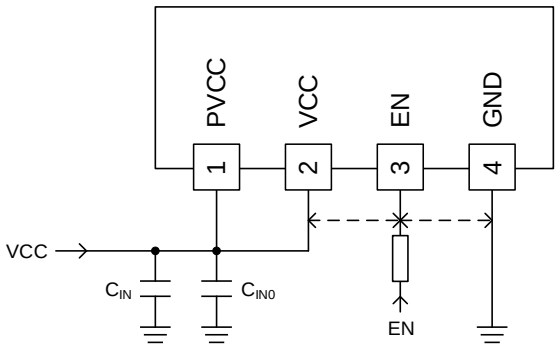


Figure 24. EN Pin Resistance

2. Selection of Components Externally Connected – continued

2.7 Selection of SSCG Pin Capacitor

The SSCG pin must be short to GND, if the spread spectrum feature is not used. The capacitor (CSSC) is necessary to SSCG pin, if the spread spectrum feature is used. Use 3300 pF for f_{m_SSCG} = 2.5 kHz (Typ) modulation. (No other options)

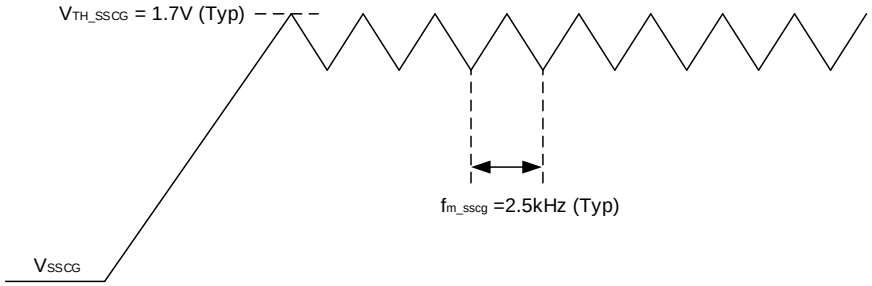


Figure 25. SSCG pin function

2.8 Selection of Resistor at RT Pin

Switching frequency depends on resistor value connected to the RT pin. RT resister must be set to 27 kΩ. The resistor tolerance must be ±1 % or less. (No other options)

2.9 Selection of External LDO

External LDO (IC_1) recommends BUxxJA2MNVX-C a miniature package. Please select external LDO by referring to "Mode Setting Description". If output current of VO4 exceed the following table value, adjust VO1 voltage to secure input/output voltage differences, or selecting LDO with better drop out voltage characteristic is recommended. Please refer Application circuit example (Using the VO1 resistance) for the method to adjust VO1 voltage.

External LDO	VO1 Voltage (typ.)	VO4 Voltage (typ.)	VO4 output current
BU28JA2MNVX-C	3.3 V	2.8 V	≤ 120 mA
BU29JA2MNVX-C	3.3 V	2.9 V	≤ 90 mA
BU33JA2MNVX-C	3.9 V	3.3 V	≤ 140 mA

Application Examples – continued

3. Circuit Example

3.1 Parts Functional Description

Item	Note	Item	Note
IC_1	External LDO	C_{SSC}	Setting to spread spectrum ratio
R_{RT}	Setting to switching frequency resistor	C_{IN1}	VO1 input capacitor
R_{PG}	PGOOD pull-up resistor	C_{O1}	VO1 output capacitor
L_1	VO1 output coil	C_{B1}	VO1 boot strap capacitor
L_2	VO2 output coil	C_{IN23}	VO2 and VO3 input (VO1 output) capacitor
L_3	VO3 output coil	C_{O2}	VO2 output capacitor
C_{IN0}	VCC input capacitor	C_{O3}	VO3 output capacitor
C_5	VREG output capacitor	-	-

3.2 Circuit Diagram

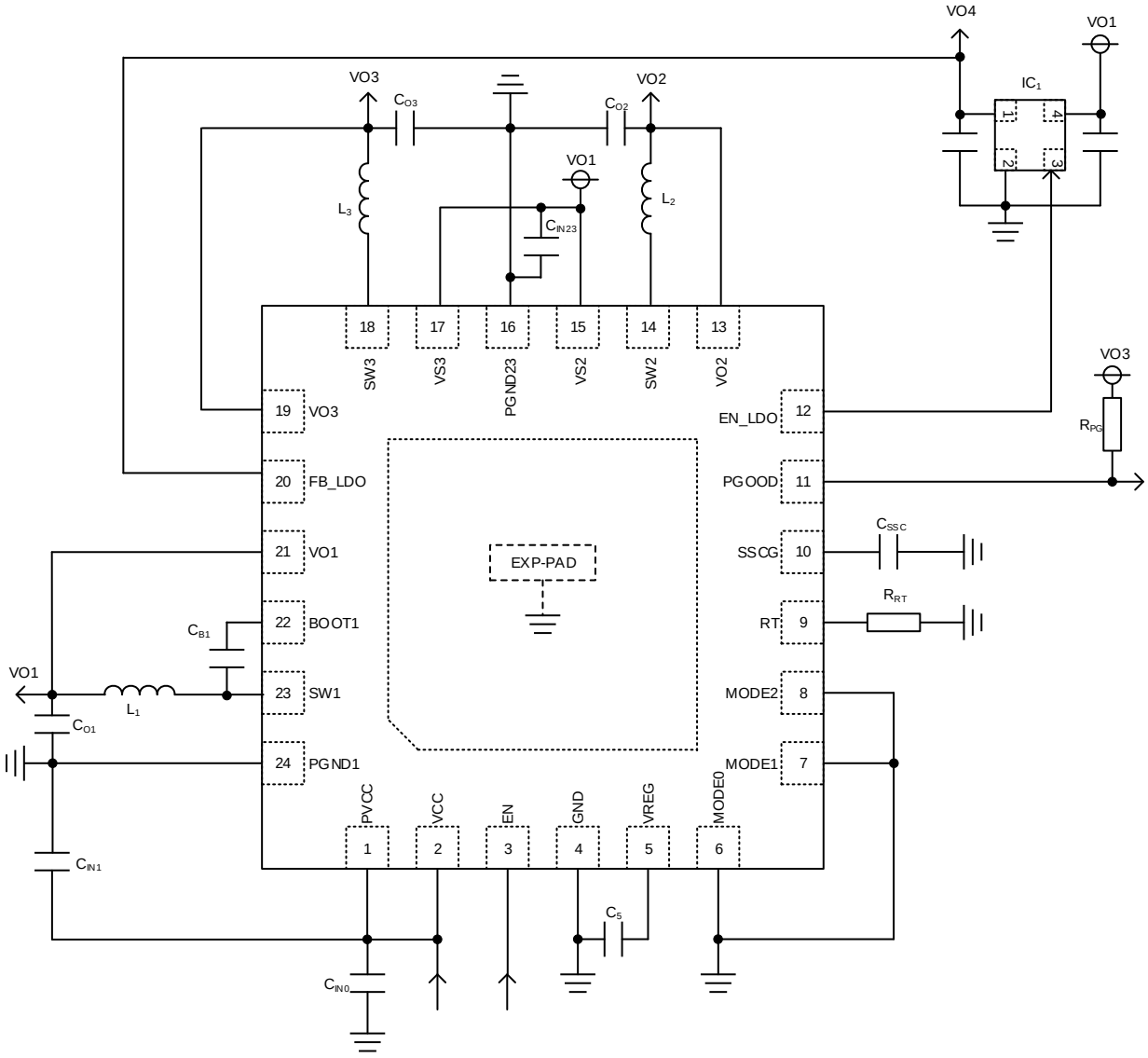


Figure 26. Application Circuits Example

3. Circuit Example - continued

3.3 Component Coefficient (No.1)

Case1 (Light load model)		Output Current
V_{VCC}	4.0 V to 18 V	-
VO1	3.3 V	≤ 0.3 A *(Note 1)*
VO2	1.1 V or 1.2 V	≤ 0.25 A
VO3	1.8 V	≤ 0.25 A

(Note 1) Include VO2, VO3 and VO4 current.

Case2 (Light load model)		Output Current
V_{VCC}	5.0 V to 18 V	-
VO1	3.9 V	≤ 0.3 A *(Note 1)*
VO2	1.2 V	≤ 0.25 A
VO3	1.8 V	≤ 0.25A

(Note 1) Include VO2, VO3 and VO4 current.

Item	Value			UNIT	Parts No.	Size	Maker
	Min *(Note 1)*	Typ	Max *(Note 2)*				
IC	-	-	-	-	BD86852MUF-C	4.0 mm x 4.0 mm	ROHM
IC_1	-	-	-	-	BUxxJA2MNVX-C	1.0 mm x 1.0 mm	
R_{RT}	26.4	27.0	27.6	kΩ	MCR01MZPF2702	1005	
R_{PG}	9	10	11	kΩ	MCR01MZPJ103	1005	
C_{IN0}	0.05	0.10	0.15	µF	CGA2B3X7R1E104K	1005	TDK
C_5	0.5	1.0	3.3	µF	CGA3E1X7R1C105K	1608	
C_{IN1}	2.0	4.7	15.0	µF	CGA4J1X7R1E475K	2012	
C_{SSC}	2300	3300	4400	pF	CGA2B2X7R1H332K	1005	
C_{O1} *(Note 3)*	5	10	21	µF	CGA4J1X7R0J106K	2012	
C_{B1}	22	47	70	nF	CGA2B2X7R1C473K	1005	
C_{IN23} *(Note 3)*	1.2	2.2	6.0	µF	CGA4J3X7R1C225K	2012	
C_{O2}	5	10	35	µF	CGA4J1X7R0J106K	2012	
C_{O3}	5	10	35	µF	CGA4J1X7R0J106K	2012	
L_1	- *(Note 4)*	3.3	4.2	µH	MLD2016S3R3MTD25	2016	
L_2	- *(Note 5)*	1.5	3.0	µH	TFM201610ALMA1R5M	2016	
L_3	- *(Note 5)*	1.5	3.0	µH	TFM201610ALMA1R5M	2016	

(Note 1) Consider tolerance, temperature characteristic and DC bias properties not to become less than the minimum
(Note 2) Consider tolerance and temperature characteristic not to become bigger than the maximum.
(Note 3) Total capacity attached to VO1 node must not exceed 40 uF.
(Note 4) Choose an inductor of 3.3 µH (Typ). It must not become less than 2.0 µH including tolerance, temperature characteristic and DC superposition characteristics.
(Note 5) Choose an inductor of 1.5 µH (Typ) or 2.2 µH (Typ). It must not become less than 1.0 µH including tolerance, temperature characteristic and DC superposition characteristics.

3. Circuit Example - continued

3.4 Component Coefficient (No.2)

Case3 (Middle load model)		Output Current
V_{VCC}	4.5 V to 18 V	-
VO1	3.3 V	≤ 1.0 A *(Note 1)*
VO2	1.1 V or 1.2 V	≤ 0.7 A
VO3	1.8 V	≤ 0.5 A

(Note 1) Include VO2, VO3 and VO4 current.

Case4 (Middle load model)		Output Current
V_{VCC}	5.5 V to 18 V	-
VO1	3.9 V	≤ 1.0 A *(Note 1)*
VO2	1.2 V	≤ 0.7 A
VO3	1.8 V	≤ 0.5 A

(Note 1) Include VO2, VO3 and VO4 current.

Case5 (Heavy load model)		Output Current
V_{VCC}	5.0 V to 18 V	-
VO1	3.3 V	≤ 2.0 A *(Note 1)*
VO2	1.1 V or 1.2 V	≤ 1.0 A
VO3	1.8 V	≤ 1.0 A

(Note 1) Include VO2, VO3 and VO4 current.

Case6 (Heavy load model)		Output Current
V_{VCC}	6.0 V to 18 V	-
VO1	3.9 V	≤ 2.0 A *(Note 1)*
VO2	1.2 V	≤ 1.0 A
VO3	1.8 V	≤ 1.0 A

(Note 1) Include VO2, VO3 and VO4 current.

Item	Value			UNIT	Parts No.	Size	Maker
	Min *(Note 1)*	Typ	Max *(Note 2)*				
IC	-	-	-	-	BD86852MUF-C	4.0 mm x 4.0 mm	ROHM
IC_1	-	-	-	-	BUxxJA2MNVX-C	1.0 mm x 1.0 mm	
R_{RT}	26.4	27.0	27.6	kΩ	MCR01MZPF2702	1005	
R_{PG}	9	10	11	kΩ	MCR01MZPJ103	1005	
C_{IN0}	0.05	0.10	0.15	µF	CGA2B3X7R1E104K	1005	TDK
C_5	0.5	1.0	3.3	µF	CGA3E1X7R1C105K	1608	
C_{IN1}	2.0	4.7	15.0	µF	CGA4J1X7R1E475K	2012	
C_{SSC}	2300	3300	4400	pF	CGA2B2X7R1H332K	1005	
C_{O1} *(Note 3)*	5	10	21	µF	CGA4J1X7R0J106K	2012	
C_{B1}	22	47	70	nF	CGA2B2X7R1C473K	1005	
C_{IN23} *(Note 3)*	1.2	2.2	6.0	µF	CGA4J3X7R1C225K	2012	
C_{O2}	5	10	35	µF	CGA4J1X7R0J106K	2012	
C_{O3}	5	10	35	µF	CGA4J1X7R0J106K	2012	
L_1	- *(Note 4)*	3.3	4.2	µH	TFM252012ALMA3R3M	2520	
L_2	- *(Note 5)*	1.5	3.0	µH	TFM201610ALMA1R5M	2016	
L_3	- *(Note 5)*	1.5	3.0	µH	TFM201610ALMA1R5M	2016	

(Note 1) Consider tolerance, temperature characteristic and DC bias properties not to become less than the minimum
(Note 2) Consider tolerance and temperature characteristic not to become bigger than the maximum.
(Note 3) Total capacity attached to VO1 node must not exceed 40 uF.
(Note 4) Choose an inductor of 3.3 µH (Typ). It must not become less than 2.0 µH including tolerance, temperature characteristic and DC superposition characteristics.
(Note 5) Choose an inductor of 1.5 µH (Typ) or 2.2 µH (Typ). It must not become less than 1.0 µH including tolerance, temperature characteristic and DC superposition characteristics.

3. Circuit Example - continued

3.5 Application Circuit Example (FB_LDO and EN_LDO Not Connect)

When FB_LDO and EN_LDO are not connected to external LDO, connect FB_LDO to EN_LDO.
In this case, LVD and OVD of VO4 are not detected. And sequence of VO4 cannot be controlled.

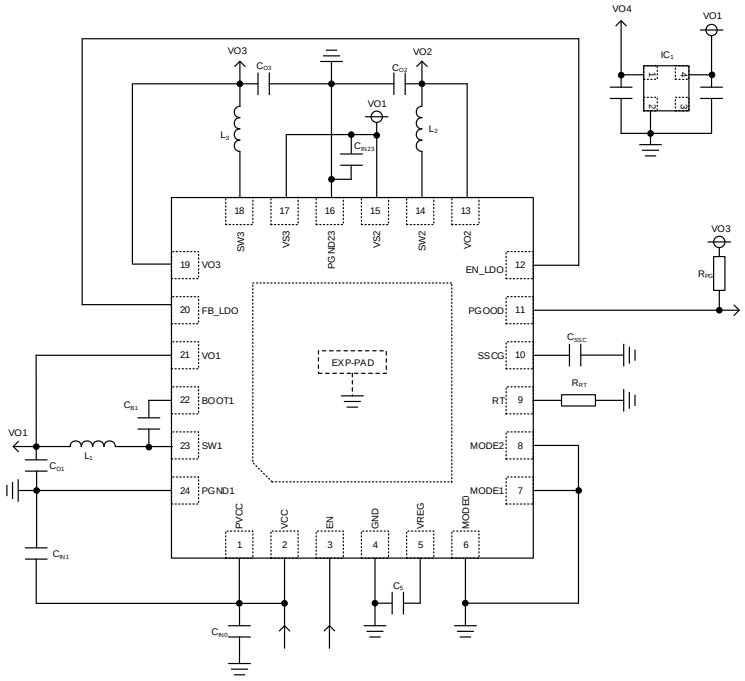


Figure 27. Application Circuit Example (FB_LDO and EN_LDO not connect)

3.6 Application Circuit Example (FB_LDO Not Connect)

When FB_LDO is not connected to external LDO, connect FB_LDO to EN_LDO.
In this case, LVD and OVD of VO4 are not detected.

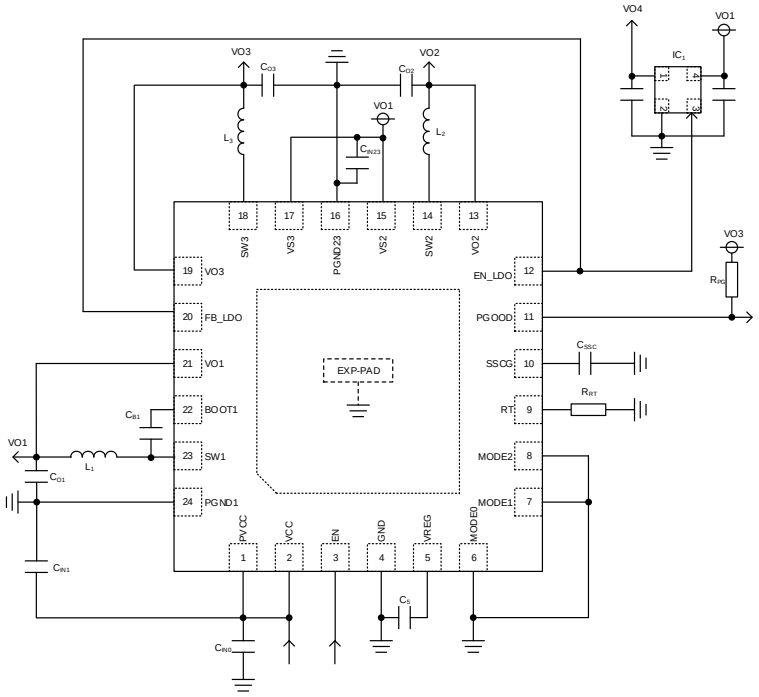


Figure 28. Application Circuit Example (FB_LDO not connect)

3. Circuit Example - continued

3.7 Application Circuit Example (EN_LDO Not Connect)

When EN_LDO is not connected to external LDO, open EN_LDO pin.
In this case, sequence of VO4 cannot be controlled.

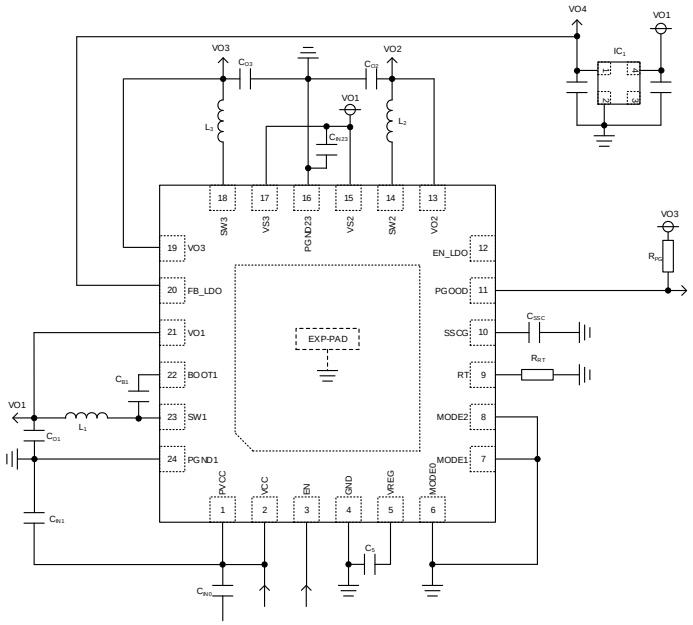


Figure 29. Application Circuit Example (EN_LDO not connect)

3. Circuit Example - continued

3.8 Application Circuit Example (Using the EN Resistance)

When VCC input voltage is high enough, by using resistance division resistance (R_{EN1}, R_{EN2}) of VCC, it's possible to turn off the output voltage in turn without externally controlling the EN pin.

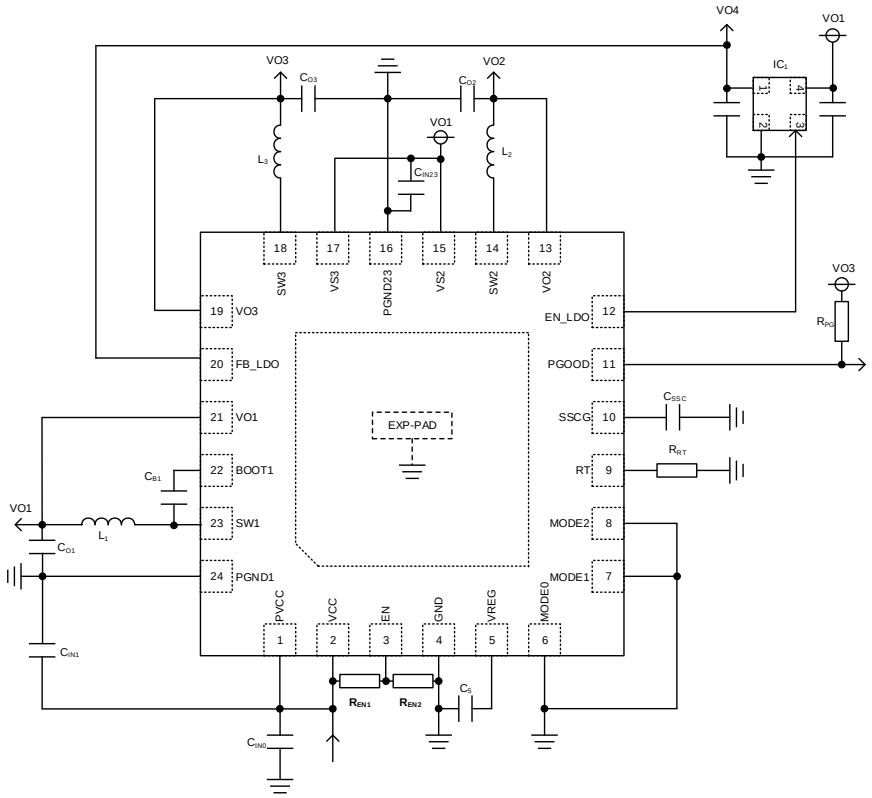


Figure 30. Application Circuit Example (Using the EN resistance)

It is necessary to make V_{EN} more than V_{TH_EN1} at power up sequence, and less than V_{TH_EN2} before $V_{UVLOVCC}$ turns ON at power down sequence.
Please choose R_{EN1}, R_{EN2} to satisfy the following expressions.

$$V_{EN} = \frac{\left(V_{VCC(MIN)} \times R_{EN2} \quad - \quad R_{EN1} \times R_{EN2} \times I_{EN(MAX)}\right)}{R_{EN1} + R_{EN2}} \quad \geq V_{TH\_EN1(MAX)}$$

$$V_{EN} = \frac{\left(V_{UVLOVCC\_ON(MAX)} \times R_{EN2} \quad - \quad R_{EN1} \times R_{EN2} \times I_{EN(MIN)}\right)}{R_{EN1} + R_{EN2}} \quad \leq V_{TH\_EN2(MIN)}$$

Where:

$V_{VCC(MIN)}$ is the minimum input voltage.
$I_{EN(MAX)}$: 45 µA
$V_{TH\_EN1(MAX)}$: 2.6 V
$V_{UVLOVCC\_ON(MAX)}$: 3.6 V
$I_{EN(MIN)}$: 5 µA
$V_{TH\_EN2(MIN)}$: 1.5 V

3.8 Application Circuit Example (Using the EN Resistance) - continued

It is necessary that each output voltage is OFF before $V_{UVLOVCC}$ turns ON to make outputs sequentially OFF. Discharge time after each output turns OFF to LVD starts can be calculated by the following expressions.

$$t_i = -C_{Oi} \times R_{VOiDIS} \;//\; R_{LOADi} \times \ln\left(\frac{V_{LVDi}}{V_{Oi}}\right)$$

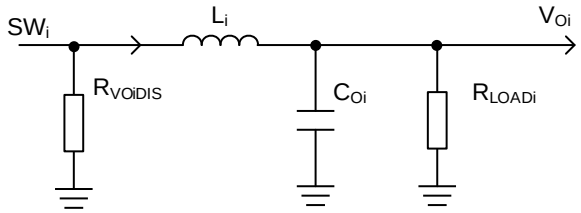


Figure 31. Discharge Resister

Where:

R_{VOiDIS}: Discharge resistor (DCDC2, DCDC3)
V_{LVDi}: LVD Operating Voltage
R_{LOADi}: Load resistor
C_o: Output capacitor
V_o: Output Voltage
DCR of Li is not considered

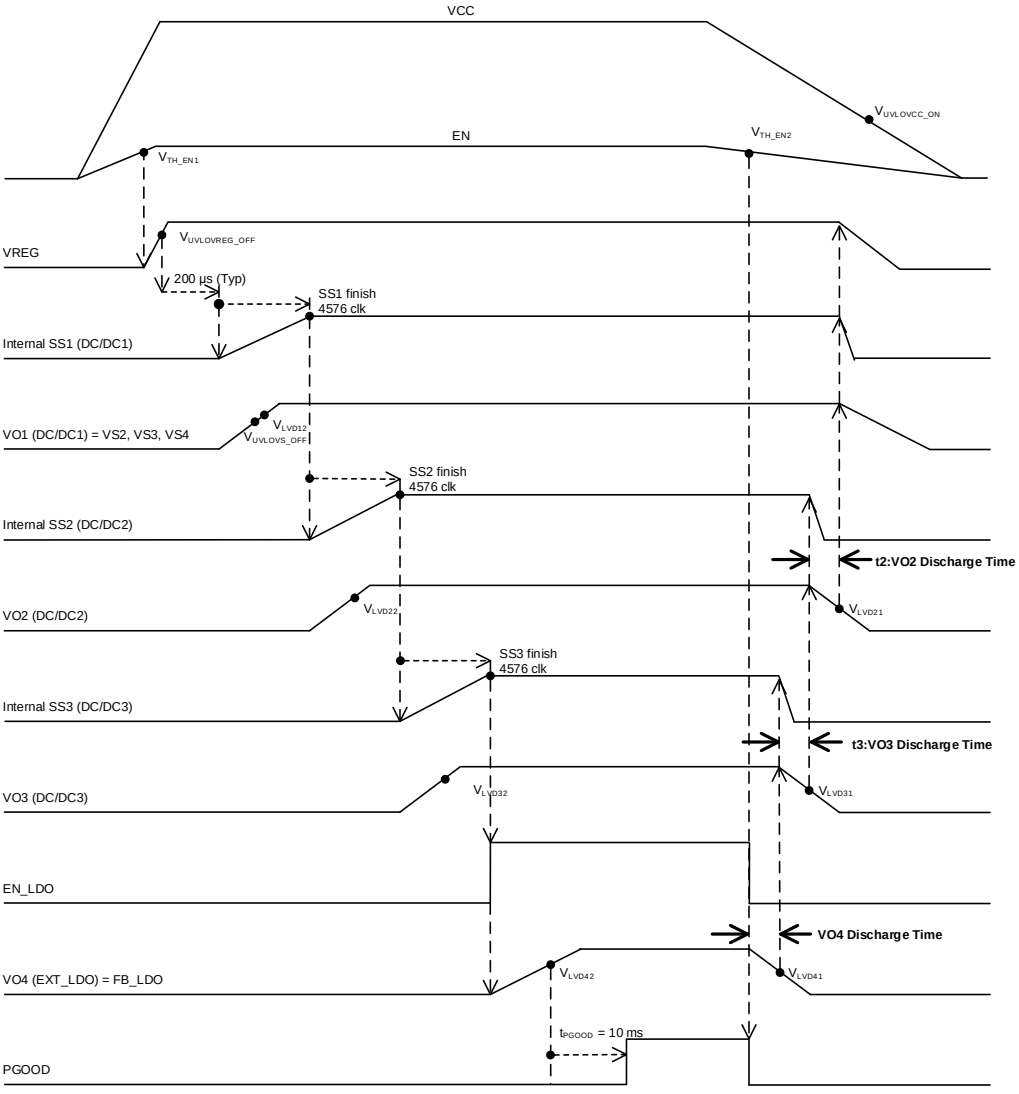


Figure 32. Output Timing Chart (Using the EN Resistance)

3. Circuit Example - continued

3.9 Application Circuit Example (Using the VO1 Resistance)

It's possible to adjust input voltage of DCDC2, DCDC3 and Ext LDO (V_{VO1_adj}) by the following dividing resistance (R_{VO1A}, R_{VO1B}).

$$V_{VO1\_adj} = \frac{(R_{VO1A} + R_{VO1B})}{R_{VO1B}} \times (V_{VO1} + R_{VO1A} \times I_{VO1\_CUR})$$

Where:

R_{VO1A}: Please select resistance value less than 5 kΩ.
I_{VO1_CUR}: VO1 Input current

Please choose R_{VO1A} and R_{VO1B} so that V_{VO1_adj} does not exceed 4.0 V.

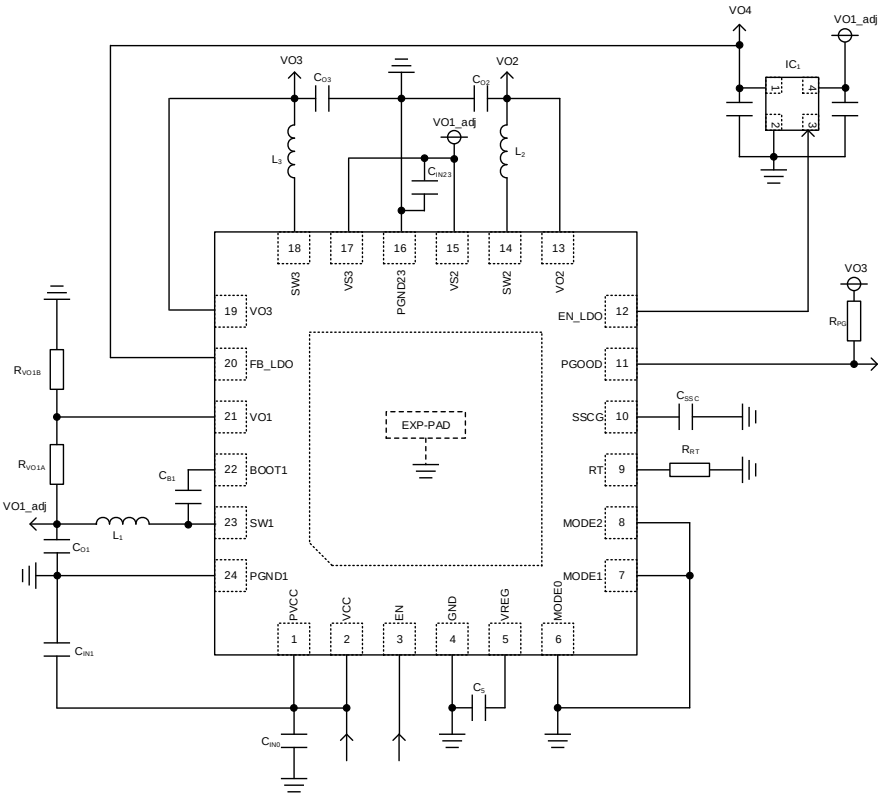


Figure 33. Application Circuit Example (Using the VO1 Resistance)

Power Loss

Use good margin to keep the Ta and Tj operating range in the thermal design below.
Do not exceed the temperature specification of Ta and Tj at any time by design.

1. Ambient temperature Ta < 125 °C
2. Chip junction temperature Tj < 150 °C

Chip junction temperature Tj can be estimated by the following two ways.

I. Estimate Tj based on the package top center temperature Tt in actual usage.

$$Tj = Tt + \psi_{JT} \times W$$

II. Estimate Tj based on the ambient temperature Ta.

$$Tj = Ta + \theta ja \times W$$

Power dissipation W of the IC is calculated by the following equation.

$$W = I_{CC} \times V_{CC} + W_1 + W_2 + W_3$$

Where:
I_{CC} is circuit current.
VCC is input voltage.
W_1 is power dissipation of DC/DC1.
W_2 is power dissipation of DC/DC2.
W_3 is power dissipation of DC/DC3.

Power loss of DC/DC W_1 to W_3

I. Loss of Tr $\frac{1}{2} T_r \times V_S \times I_O \times f_{req}$

II. Loss of High Side FET ON resistance $R_{ONH} \times {I_O}^2 \times \frac{V_O}{V_S}$

III. Loss of Tf $\frac{1}{2} T_f \times V_S \times I_O \times f_{req}$

IV. Loss of body diode $V_F \times I_O \times 2 \times t_{OFF} \times f_{req}$
(When using external SBD, loss will not be included in IC.)

V. Loss of Low Side FET ON resistance $R_{ONL} \times {I_O}^2 \times \left(\frac{V_S - V_O}{V_S} - 2 \times t_{OFF} \times f_{req}\right)$

Where:
V_S is input voltage.
V_O is output voltage.
I_O is output current.
Tr/Tf is the rising/falling time of the switching voltage transition.
Freq is oscillation frequency.
R_{ONH} is RON of high side FET.
R_{ONL} is RON of low side FET.
V_F is body diode of low side FET.
t_{OFF} is dead time.

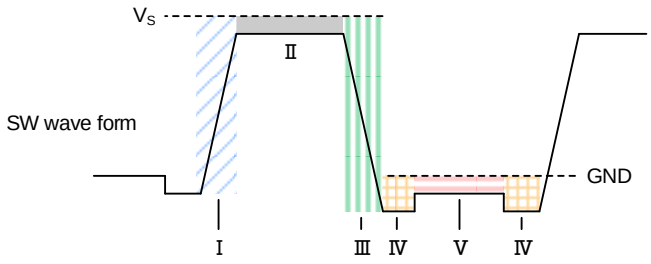


Figure 34. Power Loss of DC/DC

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

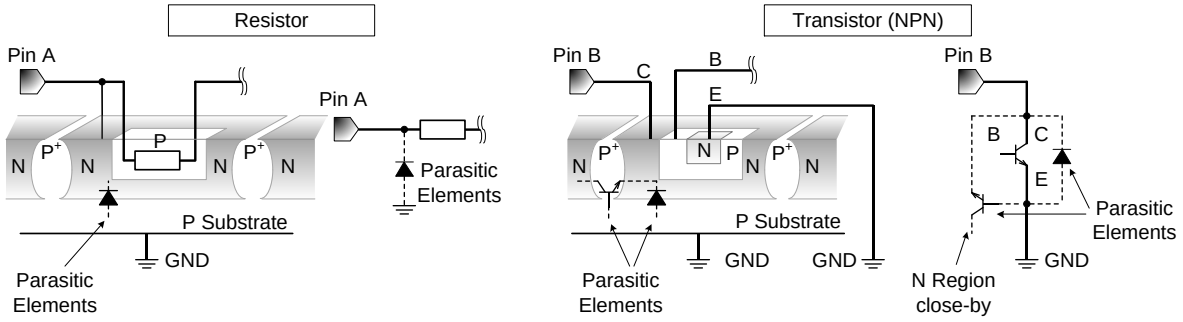


Figure 35. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Operational Notes – continued

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

15. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

(Note) "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

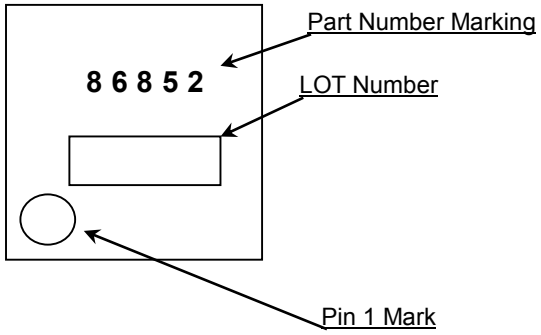
B	D	8	6	8	5	2	M	U	F	-	CE 2

Package
MUF: VQFN24FV4040

Packaging and forming specification
C: for Automotive
E2: Embossed tape and reel

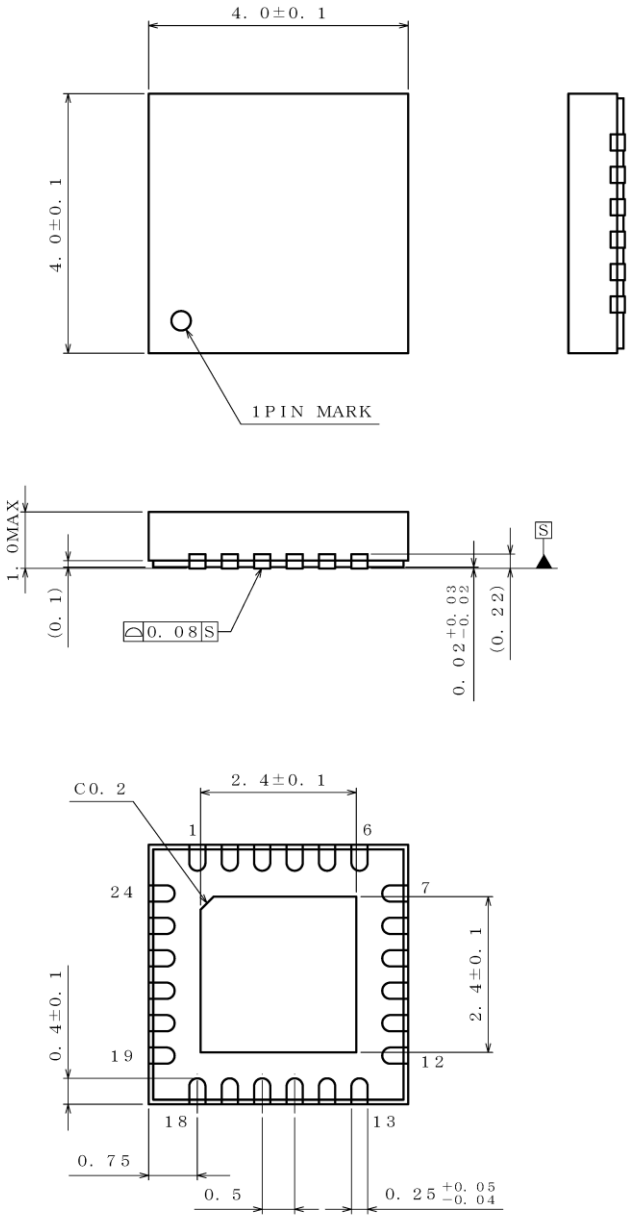
Marking Diagrams

VQFN24FV4040 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN24FV4040



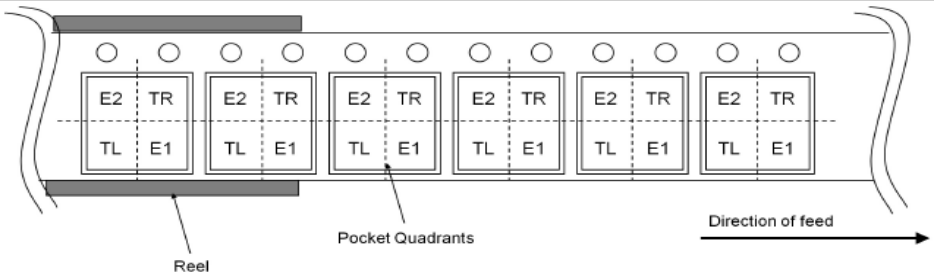
(UNIT : mm)

PKG : VQFN24FV4040
Drawing No. EX394−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
03.Mar.2020	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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General Precaution

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2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

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