*Click **here** to ask an associate for production status of specific part numbers.*

DS28E30

1-Wire ECDSA Secure Authenticator

General Description

The DS28E30 provides a highly secure and easily deployed turnkey authentication solution based on the FIPS-186 ECDSA standard. The secure authenticator combines ECDSA challenge and response authentication with secured EEPROM for the storage of the keys and user data.

The device provides a core set of cryptographic tools derived from integrated blocks including an asymmetric hardware engine, a true random number generator (TRNG), 3Kb of secure EEPROM, a decrement-only counter, and a unique 64-bit ROM identification number (ROM ID). The ECC public/private key capabilities operate from the NIST-defined P-256 curve to provide a FIPS 186-compliant ECDSA signature generation function to support a bidirectional asymmetric key authentication model. The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. In addition, authenticity of the chip can be verified with a Maxim-provided public key certificate. The device communicates over the single-contact 1-Wire® bus at overdrive speed. The communication follows the 1-Wire protocol with the ROM ID acting as a node address in the case of a multidevice 1-Wire network.

Applications

- Battery Authentication and Charge Cycle Tracking
- Medical Tools/Accessories Authentication and Calibration
- Accessory and Peripheral Secure Authentication

Request DS28E30 Security User Guide

Benefits and Features

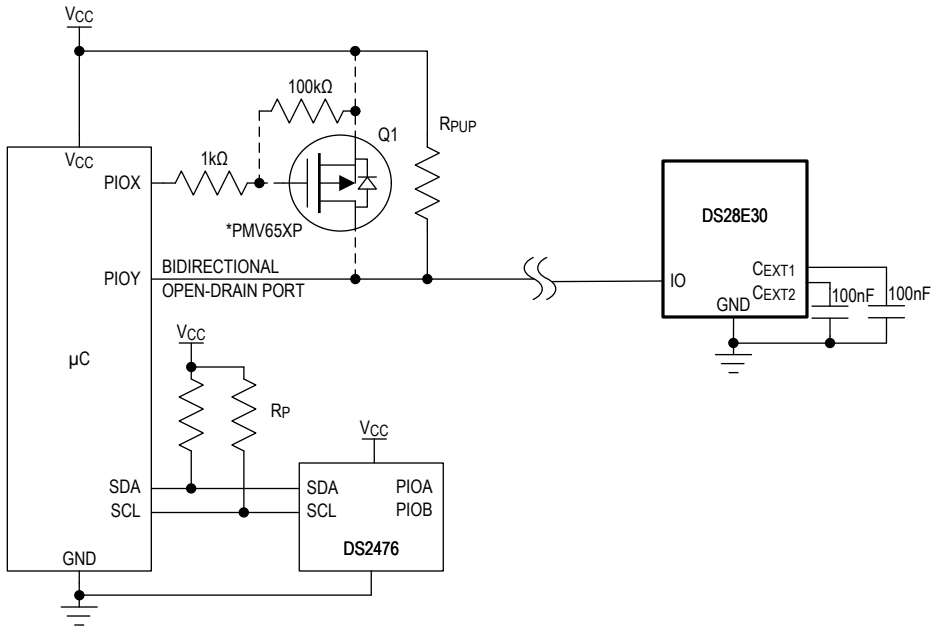
- Robust Countermeasures Protect Against Security Attacks
  - All Stored Data Cryptographically Protected from Discovery
- ECC P-256 Secure Compute Engine
  - Preprogrammed and Write-Protected ECC P-256 Key Pair
  - FIPS 186-4 Compliant ECDSA for Strong Challenge/Response Authentication
  - ECDSA Authenticated R/W of Configurable Memory
- SP800-90B TRNG Used for Secure ECDSA Nonces
- Supplemental Features Enable Easy Integration into End Applications
  - 17-Bit, One-Time Settable, Nonvolatile Decrement-Only Counter with Authenticated Read
  - 3Kb of Secure EEPROM for User Data, Keys, Certificate, and Secure Counter
  - Unique and Unalterable Factory-Programmed, 64-Bit Identification Number (ROM ID)
  - Authenticity Verification with ECDSA Using Preprogrammed Maxim Certificate
  - Advanced 1-Wire Protocol Minimizes Interface to Single Contact
  - Full-Time Overdrive Communication Speed
  - Operating Range: -40°C to +85°C, 1.62V to 5V
  - 4-Bump WLP
  - 3.5µA (typ) Input Load Current
  - High ESD Immunity of 1-Wire Pin: ±8kV Human Body Model (HBM), typ

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Ordering Information appears at end of data sheet.

19-101194; Rev 1; 2/22

Typical Application Circuit



*NOTE: OPTIONAL Q1 LOW-IMPEDANCE BYPASS OR EQUALLY DRIVE LOGIC '1' WITH PIOY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

V_{DD} to GND ..... -0.5V to 5.5V
Any Pin to GND except V_{DD} (Any Pin to GND except V_{DD}) -0.3V to V_{DD} + 0.3V
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

4 WLP

Package Code	Z41A1+1
Outline Number	**21-100548**
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	System requirement	1.62		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(*Note 1*)	300		750	Ω
Input Capacitance	C_{IO}	(*Note 1*, *Note 2*)		0.1 + C_{CEXT1}		nF
Capacitor External 1	C_{EXT1}		100			nF
Capacitor External 2	C_{EXT2}		100			nF
Input Load Current	I_L	IO pin at V_{PUP}		3.5	11	µA
High-to-Low Switching Threshold	V_{TL}	(*Note 3*, *Note 4*)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(*Note 5*)			0.18 x V_{PUP}	mV
Low-to-High Switching Threshold	V_{TH}	(*Note 3*, *Note 6*)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(*Note 3*, *Note 7*)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA (*Note 8*)			0.4	V
IO PIN: 1-Wire INTERFACE						
Recovery Time (*Note 9*)	t_{REC}		5			µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot Duration (*Note 10*)	t_{SLOT}		11			µs
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time	t_{RSTL}	System requirement	48		80	µs
Reset High Time (*Note 11*)	t_{RSTH}		48			µs
Presence-Detect Sample Time (*Note 12*)	t_{MSP}		7		10	µs
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (*Note 13*)	t_{W0L}		6		16	µs
Write-One Low Time (*Note 13*)	t_{W1L}		0.25		2	µs
IO PIN: 1-Wire READ						
Read Low Time (*Note 14*)	t_{RL}		0.25		2 - δ	µs
Read Sample Time (*Note 14*)	t_{MSR}		t_{RL} + δ		2	µs
Strong Pullup Operation						
Strong Pullup Current	I_{SPU}	(*Note 15*)			6	mA
Strong Pullup Voltage	V_{SPU}	(*Note 15*)	1.62			V
Read Memory Time	t_{RM}	(*Note 16*)		75		ms
Write Memory Time	t_{WM}	(*Note 16*)		100		ms
Generate ECDSA Signature	t_{GES}	(*Note 16*)		205		ms
Verify ECDSA Signature	t_{VES}	(*Note 16*)		250		ms
EEPROM						
Write/Erase Cycles (Endurance)	N_{CY}	(*Note 17*)	100k			
Data Retention	t_{DR}	T_A = +85°C (*Note 18*)	10			years
POWER-UP						
Power-Up Time	t_{OSCWUP}	System requirement (*Note 19*)			10	ms

Note 1: System requirement. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

Note 2: Value represents the typical parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

Note 3: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 4: Voltage below which, during a falling edge on IO, a logic-zero is detected.

Note 5: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.

Note 6: Voltage above which, during a rising edge on IO, a logic-one is detected.

Note 7: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.

Note 8: The I-V characteristic is linear for voltages less than 1V.

Note 9: System requirement. Applies to a single device attached to a 1-Wire line.

Note 10: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.

Note 11: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 12: System requirement. Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a device present. The power-up presence detect pulse could be outside this interval, but completes within 2ms after power-up.

Note 13: System requirement. ε in Figure 3 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.

Note 14: System requirement. δ in Figure 3 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 15: Current drawn from IO during a SPU operation interval. The pullup circuit on IO during the SPU operation interval should be such that the voltage at IO is greater than or equal to V_{SPUMIN}. A low-impedance bypass of R_{PUP} activated during the SPU operation is the recommended way to meet this requirement.

Note 16: Guaranteed by design and/or characterization only. Not production tested.

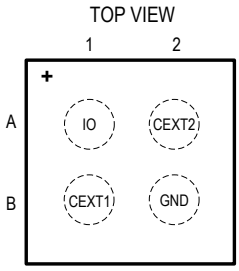
Note 17: Write-cycle endurance is tested in compliance with JESD47H.

Note 18: Data retention is tested in compliance with JESD47H.

Note 19: 1-Wire communication should not take place for at least t_{OSCWUP} after V_{PUP} reaches V_{PUP} (min).

Pin Configuration

4 WLP

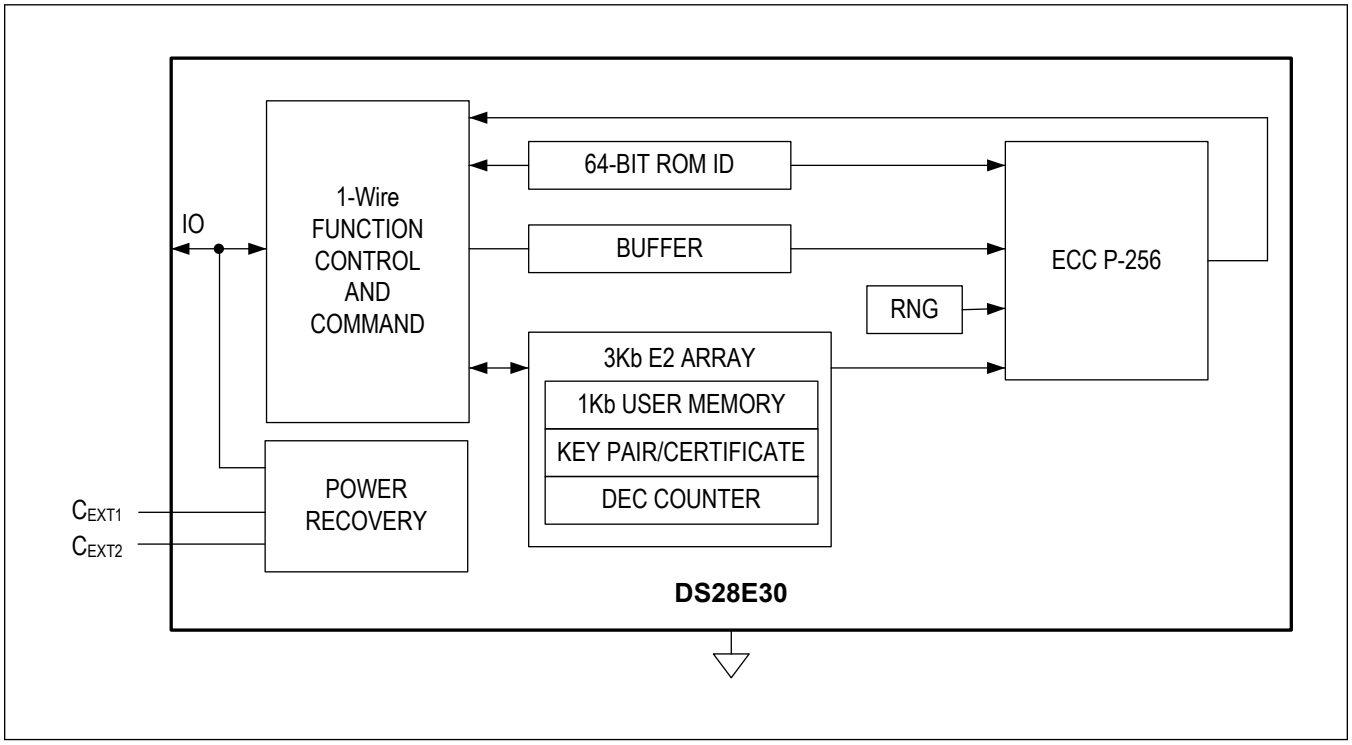


WLP

Pin Description

PIN	NAME	FUNCTION
A1	IO	1-Wire I/O
B2	GND	Ground Reference. Connect directly to the ground plane.
B1	CEXT1	Input for External Capacitor
A2	CEXT2	Input for External Capacitor

Functional Diagram



Detailed Description

The DS28E30 integrates Maxim-proprietary techniques to protect all device stored data from invasive or noninvasive discovery. The circuit design combined with cryptographic methods, both inherited from Maxim's financial terminal security experience, protect against die-level data extraction attacks.

In addition to the secure ECDSA engine for signatures, the device integrates a high-quality TRNG, a SHA-256 engine, 1Kb EEPROM for user memory, plus additional EEPROM space for one ECDSA P-256 private key, one ECDSA P-256 public key certificate, one 17-bit decrement counter, and control registers. The device operates from a 1-Wire interface with a parasitic supply by way of an external capacitor (CEXT1) and an additional capacitor (CEXT2) for the internal voltage regulator. The *Functional Diagram* shows the relationships between the circuit elements of the DS28E30.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS28E30 is a slave device. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus can drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E30 is open drain with an internal circuit equivalent.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E30 supports overdrive communication speed of 90.9kbps (max). The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E30 requires a pullup resistor of 750Ω (max).

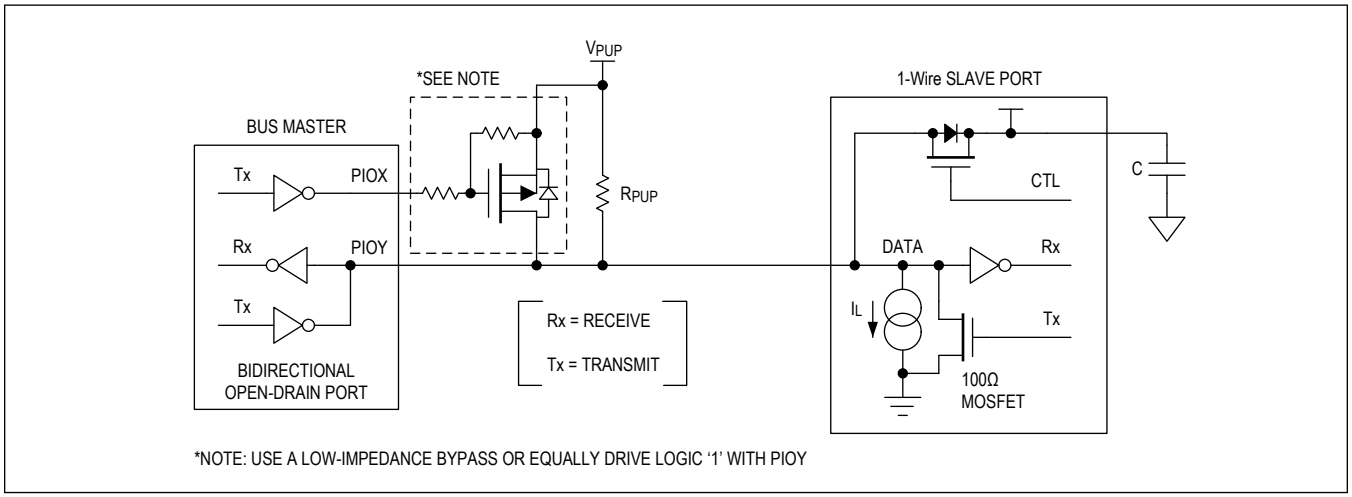


Figure 1. Hardware Configuration

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs, one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E30 through the 1-Wire port is as follows:

- Initialization
- ROM function command

- Device function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E30 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling and Timing* section.

1-Wire Signaling and Timing

The DS28E30 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 2 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E30 when determining a logical level, not when triggering any events.

Figure 2 shows the initialization sequence required to begin any communication with the DS28E30. A reset pulse followed by a presence pulse indicates that the DS28E30 is ready to receive data, given the correct ROM and device function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge.

After the bus master has released the line, it goes into receive mode. Now, the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. When the threshold V_{TH} is crossed, the DS28E30 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

Immediately after t_{RSTH} has expired, the DS28E30 is ready for data communication.

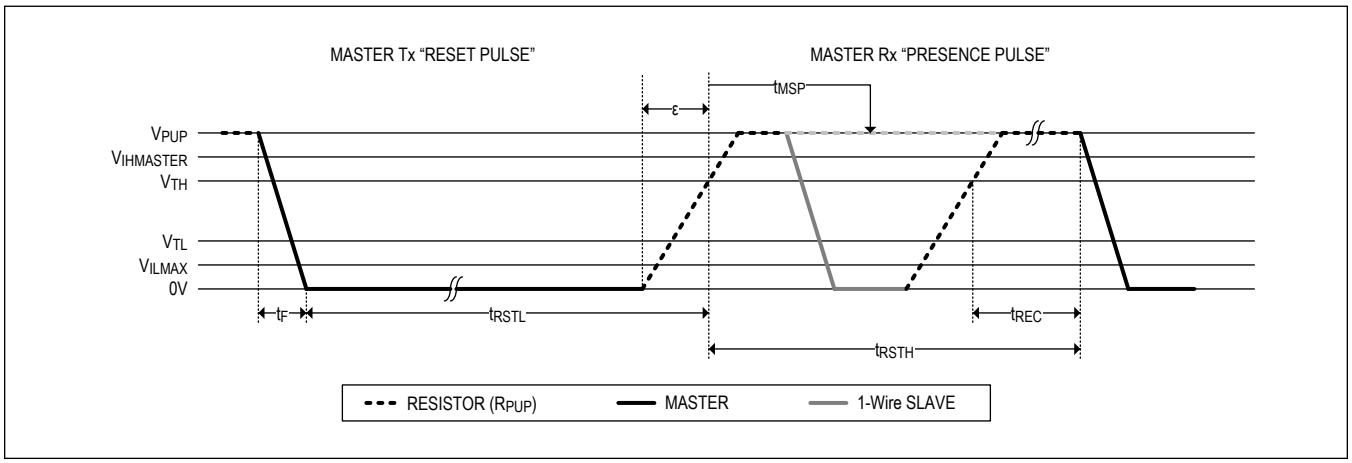


Figure 2. Initialization Procedure: Reset and Presence Pulse

Read/Write Time Slots

Data communication with the DS28E30 takes place in time slots that carry a single bit each. Write time slots transport data from the bus master to the slave. Read time slots transfer data from the slave to the master. Figure 3 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E30 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master to Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E30 needs recovery time t_{REC} before it is ready for the next time slot.

Slave to Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E30 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E30 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E30 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to, but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E30 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E30 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

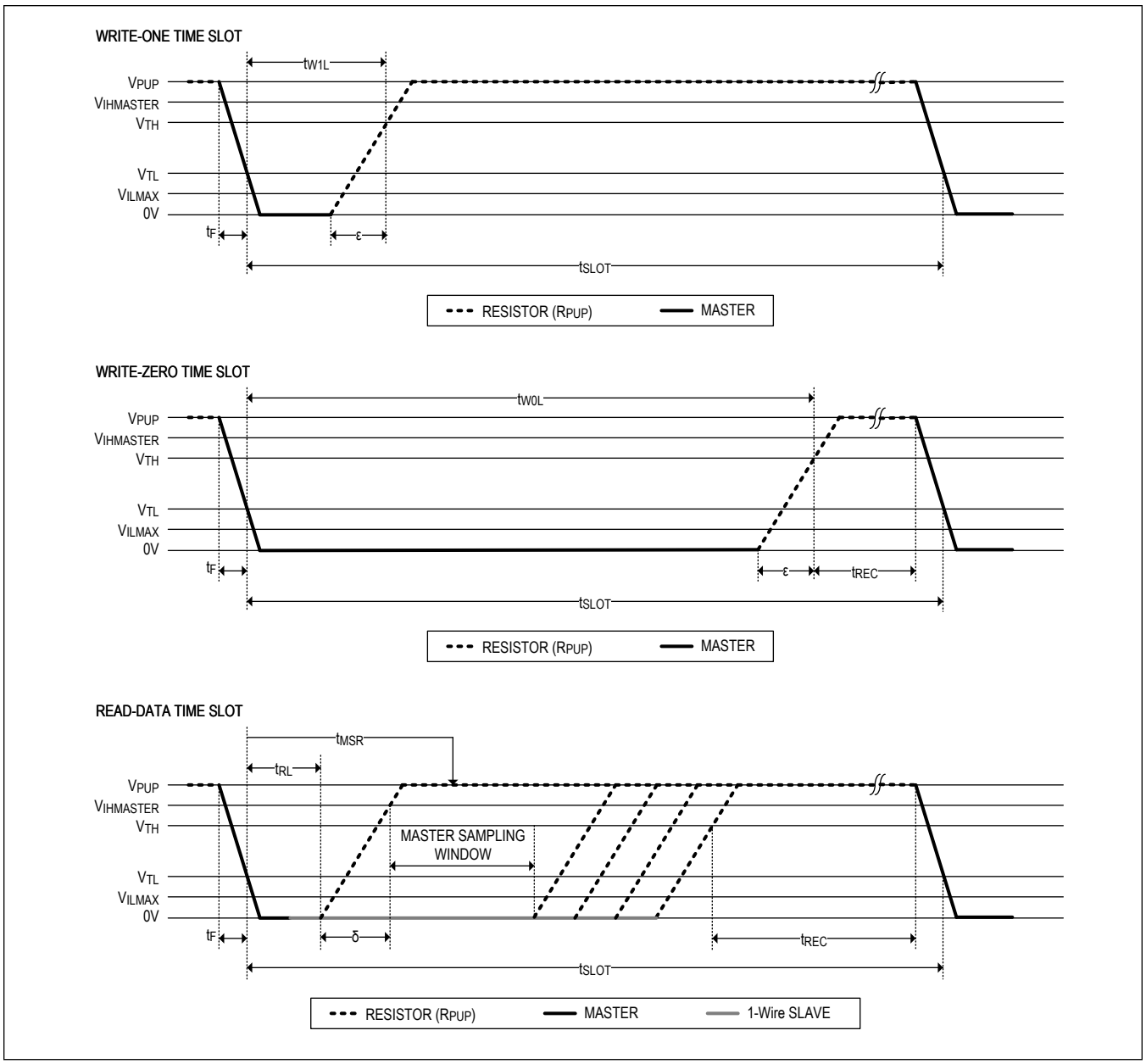


Figure 3. Read/Write Timing Diagrams

1-Wire ROM Commands

Once the bus master has detected a presence, it can issue one of the five ROM function commands that the DS28E30 supports. All ROM function commands are 8 bits long. For operational details, see Figure 4. A descriptive list of these ROM function commands follows in the subsequent sections, and the commands are summarized in Table 1.

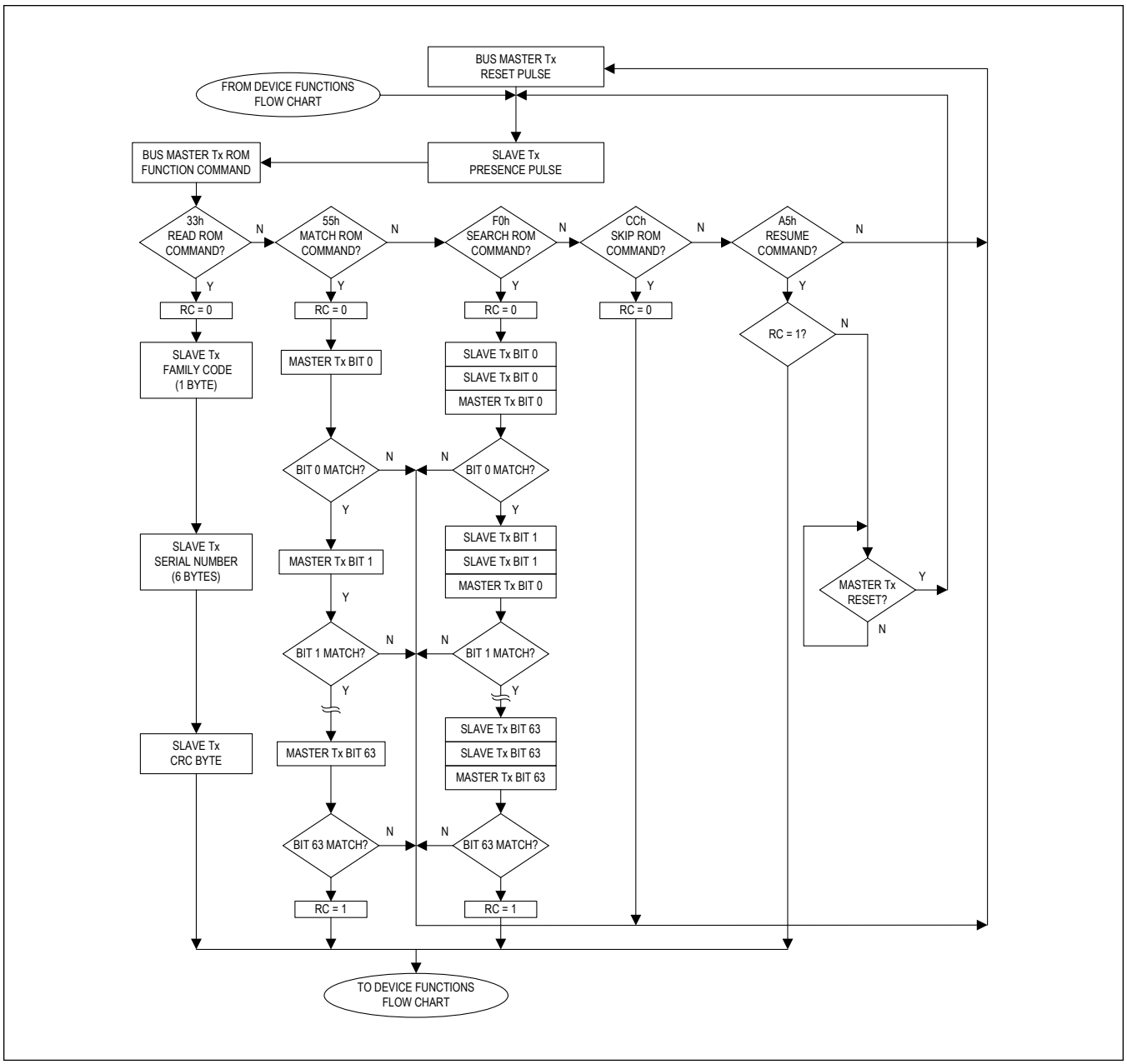


Figure 4. ROM Function Flow

Table 1. 1-Wire ROM Commands Summary

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Search ROM	F0h	Search for a device
Read ROM	33h	Read ROM from device (single drop)
Match ROM	55h	Select a device by ROM number
Skip ROM	CCh	Select only device on 1-Wire
Resume	A5h	Selected device with RC bit set

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit in the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E30's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E30 on a multidrop bus. Only the DS28E30 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the device functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the device function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM or Search ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Improved Network Behavior (Switch-Point Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E30 uses a 1-Wire front-end with built-in hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH}, but does not go below V_{TH} - V_{HY}, it is not recognized. See Figure 5.

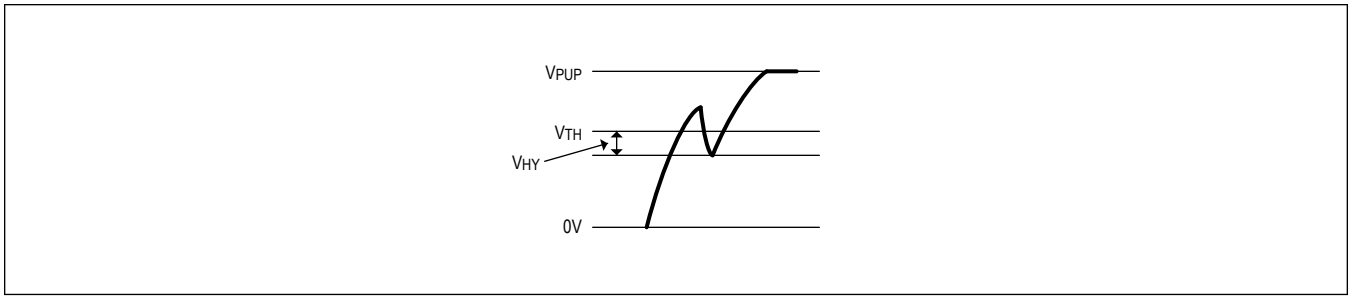


Figure 5. Noise Suppression Scheme

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
DS28E30X+T	-40°C to +85°C	4 WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—
1	2/22	Updated *Electrical Characteristics* (V_{PUP}, max), *Detailed Description*, and *Ordering Information* tables	3, 10, 17