RN5T5611-xx-E4 Series

AEC-Q100 Compliant

Programmable Power Management IC for Automotive Applications

No.EC-622-220627

OVERVIEW

The RN5T5611 is a power management IC (PMIC) for automotive applications. This IC provides two high-efficiency step-down DCDC converters, a low-noise regulator, an interrupt controller (INTC), and I²C-bus interface. Power-supply start and stop sequences can be customized to meet user-system. In addition to the basic power control, this IC provides various protection functions.

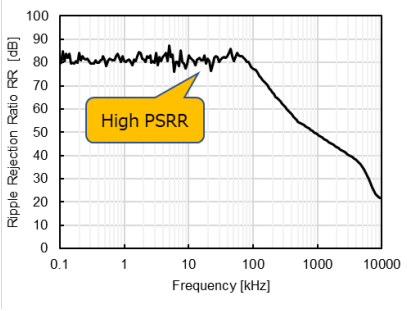
KEY BENEFITS

- Compliance with ASIL-D
- LDO regulator is provides low output noise, high ripple rejection and fast response characteristics.
- Flexible selection such as sequence and enable simplifies power sequence control.
- 2ch Step-down DCDC converters operate with 180° turn-on phase shift of the switching transistors.

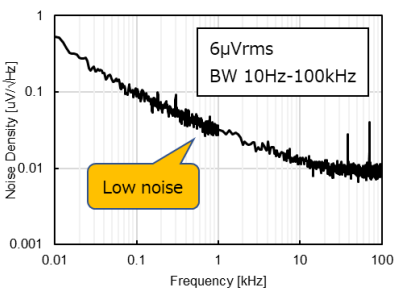
KEY SPECIFICATIONS

- Input Voltage Range (Maximum Ratings): 3.0 V to 5.5V(1) (6.5V)
- Operating Temperature Range: –40°C to 125°C
- High Efficiency Step-down DCDC Converters (REG1,2)
  - Output Range: 1.0 V to 3.3 V ±1% (Max. 1.0A)
  - Oscillator Frequency: 2.3MHz
  - Operating Mode: Forced PWM Mode
  - Overcurrent / Reverse Current Protection (Latch)
- Low Drop Voltage Regulator (REG3: Low Output Noise)
  - Output Range: 2.5 V to 3.5 V ±1% (Max. 200mA)
  - Output Noise: Typ. 6 μVrms (I_{OUT} = 100 mA)
  - PSRR: Typ. 80 dB (@1 kHz), Typ. 80 dB (@100 kHz)
  - Short Circuit Protection
- I²C-bus Interface: 1MHz and 400kHz
- Window Voltage Detector for Internal DCDC (REG1,2), LDO (REG3) and External pin
  - REG1/2DET: OV/UV 0.6V to 3.7V (12.5mV Step) ± 1% (2)
  - REG3DET: OV/UV 2.0V to 4.0V (12.5mV Step) ± 1%
  - EXTDET: OV/UV 0.6V to 3.7V (12.5mV Step) ± 1% (2)
- UVLO (Under Voltage Lock Out)
- Soft-start Circuit
- Auto-discharge
- Switching Phase Shift (DCDC)
- Flexible Setting (Output/Sequence/REG's Reaction to Errors)
- Status Monitoring by Built-in Registers
- Error Output by Interrupt Signal
- Forced Power Off by HRSTB pin
- Thermal Shutdown: Tj = 165°C

TYPICAL CHARACTERISTICS



PSRR (V_{IN} = 5.0 V, V_{OUT} = 2.9 V)



Output Noise (I_{OUT} = 100 mA)

PACKAGE

QFN0505-32-P7
(Wettable Flanks, Lead-less)
5.0mm x 5.0mm,
t = 0.75 mm

APPLICATIONS

- ADAS including Front sensing system, Camera monitoring system, Surround view, etc.

(1) The recommended operating voltage range is specified by the product code
(2) ± 1.3% at OV/UV < 1 V

SELECTION GUIDE

Selection Guide

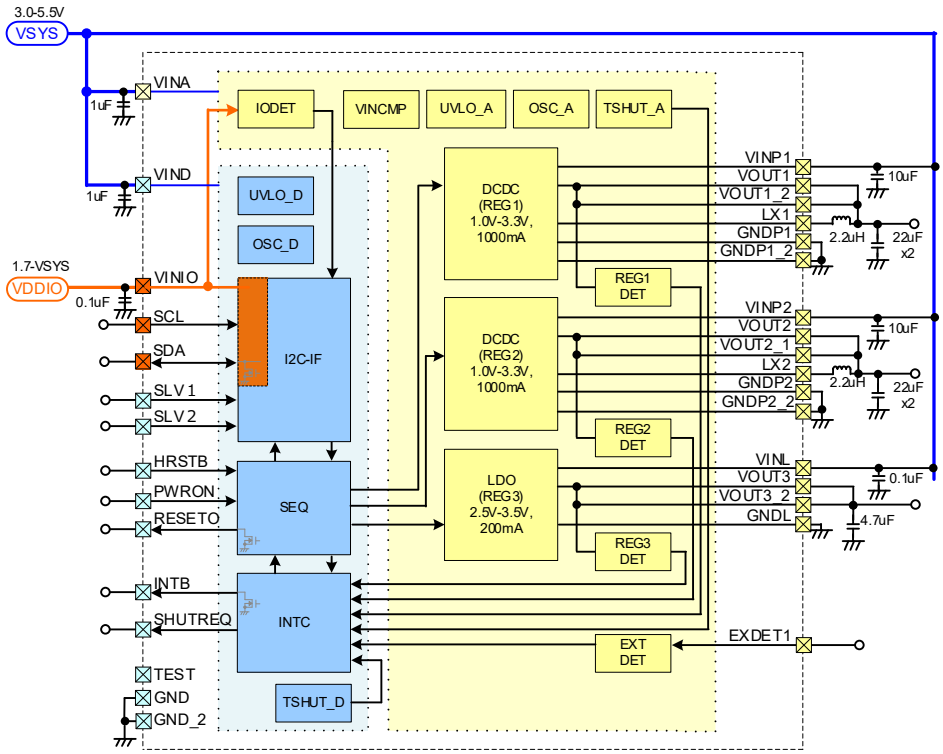
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RN5T5611-xx-E4-#E	QFN0505-32-P7	1,000 pcs	Yes	Yes

xx: Specify a product code. Refer to Appendix *"Product Code List"* for details.

#: Quality Class

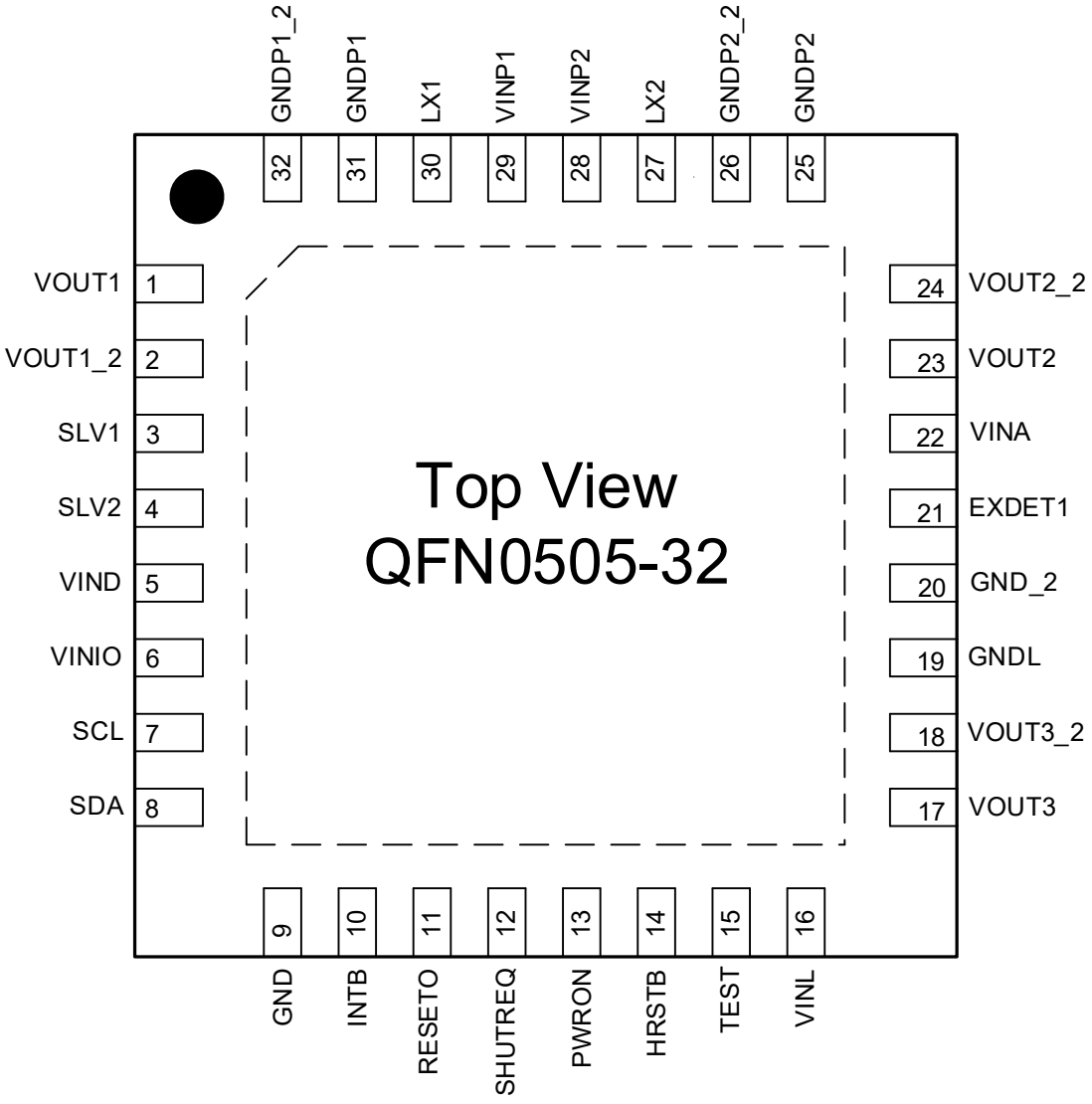
	Operating Temp. Range	Test Temp.
K	−40°C to 125°C	Low, 25°C, High

BLOCK DIAGRAM



RN5T5611 Block Diagram

PIN DESCRIPTION



RN5T5611 Pin Configuration

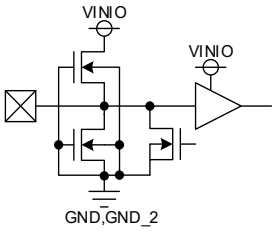
Pin Assignments

No.	Pin Name	Function	I/O(1)	D/A(2)	Reset State(3)		Note
					I/O	Level	
1	VOUT1	REG1 output pin	I/O	A	-	-	
2	VOUT1_2						
3	SLV1	I²C-bus slave address [1(LSB)] select pin	I	D	I	-	CMOS Schmitt
4	SLV2	I²C-bus slave address [2] select pin	I	D	I	-	CMOS Schmitt
5	VIND	Power supply for Digital	-	P	-	-	
6	VINIO	Power supply for I²C-bus interface I/O	-	P	-	-	
7	SCL	I²C-bus input clock pin	I	D	I	-	CMOS Schmitt
8	SDA	I²C bus data pin	I/O	D	I	Hi-z	CMOS Schmitt, Nch Open Drain
9	GND	GND for Analog and Digital circuits	-	G	-	-	
10	INTB	Interrupt pin	O	D	O	Hi-z	Nch Open Drain (4)
11	RESETO	reset output pin	I/O	D	O	Low	Nch Open Drain (4)
12	SHUTREQ	Shut down Request	O	D	O	Low	CMOS Output
13	PWRON	Power On pin	I	D	I	-	NMOS Schmitt (5)
14	HRSTB	Hardware reset input pin	I	D	I	-	NMOS Schmitt (5)
15	TEST	Test pin (Connect to GND)	I	D	I	-	CMOS Schmitt (5)
16	VINL	Power supply for REG3	-	P	-	-	
17	VOUT3	REG3 output pin	I/O	A	-	-	
18	VOUT3_2						
19	GNDL	GND for REG3	-	G	-	-	
20	GND_2	GND for Analog and Digital circuits	-	G	-	-	
21	EXDET1	External input voltage detector sense pin	I	A	-	-	
22	VINA	Power supply for Analog	-	P	-	-	
23	VOUT2	REG2 output pin	I/O	A	-	-	
24	VOUT2_2						
25	GNDP2	GND for REG2	-	G	-	-	
26	GNDP2_2						
27	LX2	REG2 switching pin	O	A	-	-	
28	VINP2	Power supply for REG2	-	P	-	-	
29	VINP1	Power supply for REG1	-	P	-	-	
30	LX1	REG1 switching pin	O	A	-	-	
31	GNDP1	GND for REG1	-	G	-	-	
32	GNDP1_2						

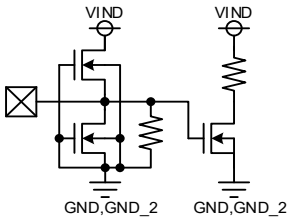
(1) I: Input, O: Output
(2) A: Analog, D: Digital, P: Power, G: Ground
(3) HRSTB pin is driven low.
(4) Require an external pull-up resistor of 10 kΩ to 100 kΩ.
(5) With a built-in pull-down resistor

Equivalent Circuits for the Individual Pins

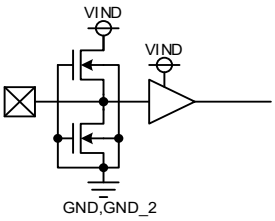
SDA, SCL



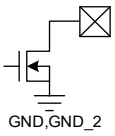
PWRON, HRSTB



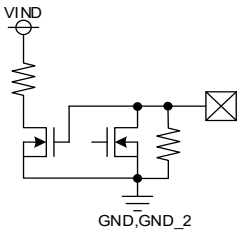
SLV1, SLV2



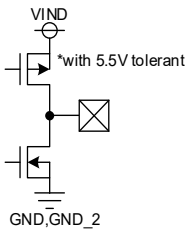
INTB



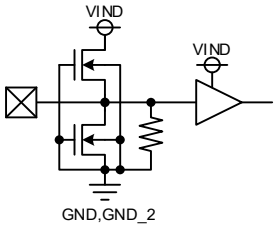
RESETO



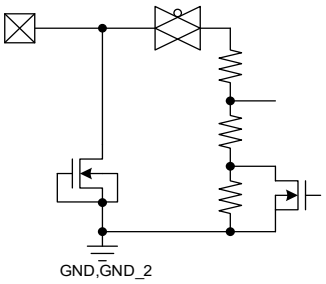
SHUTREQ



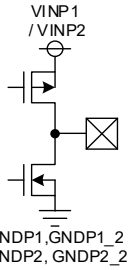
TEST



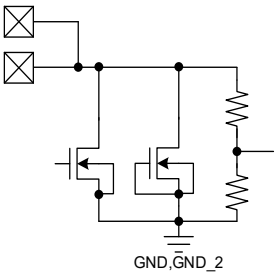
EXDET1



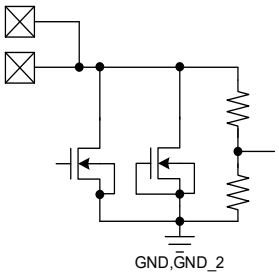
LX1, LX2



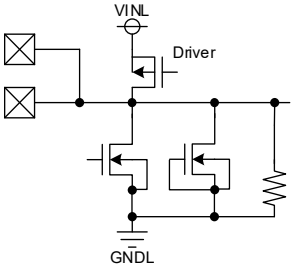
VOUT1, VOUT1_2



VOUT2, VOUT2_2



VOUT3, VOUT3_2



ABSOLUTE MAXIMUM RATINGS

(GNDs[1] = 0 V)

Symbol	Parameter	Condition	Rating	Unit
V_{PS}	Power Supply Voltage	VINA, VIND, VINIO, VINL and VINP1-2 pins	–0.3 to 6.5	V
V_{INPUT}	Input Voltage Range	EXDET1 pin	–0.3 to V_{INA} + 0.3	V
		PWRON, HRSTB and SLV1-2 pins	–0.3 to V_{IND} + 0.3	V
		SDA and SCL pins	–0.3 to 6.5	V
V_{OUTPUT}	Output Voltage Range	SHUTREQ, INTB and RESETO pins	–0.3 to V_{IND} + 0.3	V
Tj	Junction Temperature	-	–40 to 150	°C
Tstg	Storage Temperature	-	–55 to 150	°C
P_D	Package Dissipation	Refer to Appendix “Power Dissipation”		

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{SYS}	Power Supply Voltage	VIN∗ pins [2]	× 0.9	V_{SYS_TYP} [4]	× 1.1	V
V_{DDIO}	Power Supply Voltage	VINIO pin [3]	1.7	1.8	V_{IND}	V
GND	Ground	GNDs [1]		0		V
Ta	Temperature of Operation	-	–40		125	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating ratings. The semiconductor devices cannot operate normally over the recommended operating ratings, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating ratings.

[1] GNDs: GND signals including GND, GND_2, GNDL, GNDP1, and GNDP2.
[2] VINP1-2, VINL and VIND must be equal to VINA.
[3] VINIO must be less than or equal to VIND.
[4] V_{SYS_TYP} is Specify the Product Code. Refer to “Product Code List” for details.

ELECTRICAL CHARACTERISTICS

I/O Electrical Characteristics

(–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIND NMOS Input Pin (NMOS Schmitt): PWRON, HRSTB						
V_{IL}	Low level input voltage				0.4	V
V_{IH}	High level input voltage		1.6		V_{IND}	V
I_{PD}	Pull down current	VIN = VIND			2	µA
I_{IL}	Input Leakage Current	VIN = 0V	–1		1	µA
VIND CMOS Input Pin (CMOS Schmitt): SLV1,2						
V_{IL}	Low level input voltage				V_{IND} × 0.3	V
V_{IH}	High level input voltage		V_{IND} × 0.7		V_{IND}	V
VIND Nch Open-drain Output Pin: INTB, RESETO						
V_{OL}	Low level output voltage	I_{OUT} = 2mA			0.4	V
V_{TO}	Tolerant				V_{IND}	V
VIND CMOS Output Pin: SHUTREQ						
V_{OL}	Low-level Output Voltage	I_{OUT} = 2mA			0.4	V
V_{OH}	High-level Output Voltage	I_{OUT} = –2mA	V_{IND} – 0.4			V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VINIO CMOS Input Pin (Schmitt Input): SCL						
V_{IL}	Low level input voltage				V_{INIO} × 0.3	V
V_{IH}	High level input voltage		V_{INIO} × 0.7		V_{INIO}	V
VINIO CMOS Input / Output Pin (Schmitt Input / Nch Open-drain Output): SDA						
V_{IL}	Low level input voltage				V_{INIO} × 0.3	V
V_{IH}	High level input voltage		V_{INIO} × 0.7		V_{INIO}	V
V_{OL}	Low level output voltage	I_{OUT} = 20mA			0.4	V

Consumption Current[1]

(–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition (Device State)	Min.	Typ.	Max.	Unit
I_{RT}	Reset current	Reset			40	µA
I_{ST}	Standby current	Ready			0.8	mA

[1] V_{SYS} = V_{SYS_TYP} at No-load, unless otherwise specified.

THEORY OF OPERATION

Power Control

This IC has the start and stop sequences for the power supply.

State Machine Diagram

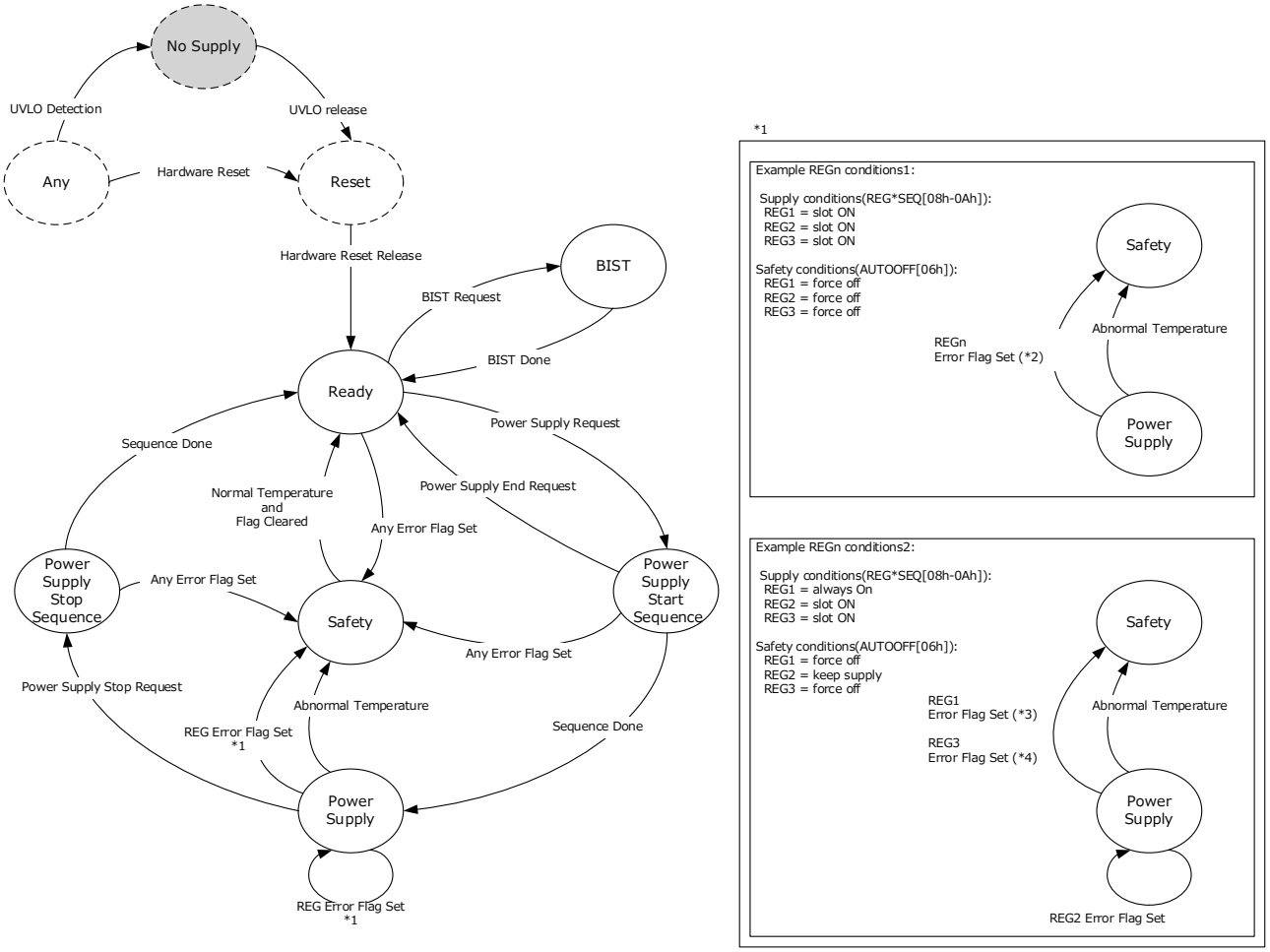


Figure 1 State Machine Diagram

*1 The transition after detecting an error is programmable.
*2 All REGs are turned off.
*3 All REGs are turned off.
*4 REG2 and REG3 are turned off. REG1 remains on.

State Machine Description

The state machine steps through the following states:

No Supply

This IC receives no power supply.

Transfer Conditions:

- If this IC detects a UVLO release, the state transitions to the Reset state.

Reset

Makes all regulators turn-off.
Initializes all register settings and makes it impossible to access through the I²C-bus interface.

Transfer Conditions:

- If the HRSTB pin is high, the state transitions to the Ready state.

Ready

Makes all regulators ready for power supply.
Makes always-on regulator turn-on and the other regulators turn-off.
Makes it possible to access to the registers through the I²C-bus interface. (1)

Transfer Conditions:

- REGn voltage of always-on regulator reaches a target voltage.
- If the BISTEN bit is “1”, the state transitions to the BIST state.
- If the Safety Mechanism (SM) detects an error, the state transitions to the Safety state.
- If the PWRON pin is “High”, the state transitions to the PS Start Sequence state.

BIST (Built-in self-test).

Executes Analog and Logic BIST and sets the results to registers.

Transfer Conditions:

- If the BISTEN bit becomes “0” by BIST, the state transitions to the Ready state.

Power Supply Start Sequence

Makes each regulator turn-on sequentially.

Transfer Conditions:

- If the SM detects an error, the state transitions to the Safety state.
- If each regulator is turned off immediately after the PWRON pin of “Low”, the state transitions to the Ready state.
- If the sequence is finished, the state transitions to the Power Supply state.

(1) The VINIO power input is required to access through the I²C-bus interface.

Power Supply

Makes each regulator turn-on.

Makes it possible to access to the registers through the I²C-bus interface. (1)

Transfer Conditions:

- If the TSHUT detects an abnormal temperature, the state transitions to the Safety state.
- If the SM detects the regulator's overcurrent / reverse current, the state transitions to the Safety state.
- If the SM detects any regulator's under/over-voltage error, the state transitions to the Safety state in a case where the DISnAUTOOFF bits are all "0", the state transition remains in a case where the DISnAUTOOFF bits are all "1".

Power Supply Stop Sequence

Makes each regulator turn-off sequentially.

Transfer Conditions:

- If the SM detects an error, the state transitions to the Safety state.
- If the sequence is finished, the state transitions to the Ready state.

Safety

Makes all regulators turn-off when the SM detects an error. But, if the always-on regulator only has not any errors, remains its regulator on. (2)

Makes it possible to access to the registers through the I²C-bus interface. It becomes able to read and clear the error flags.

Transfer Conditions:

When the number of the error detection is less than the number of the auto-restoration,

- the error flag is cleared automatically and the state transitions to the Ready state.

When the number of the error detection is more than the number of the auto-restoration,

- the state transitions to the Ready state by clearing the error flag.

Any

Any state as shown above.

Transfer Conditions:

- If this IC detects UVLO, the state transitions to the No Supply state.
- If the HRSTB pin is "Low", the state transitions to the Reset state.

(1) The VINIO power input is required to access through the I²C-bus interface.

(2) SM detects the errors as shown below. For further details of SM, refer to "Safety Mechanism".

- BIST check error
- Overcurrent / Reverse current Protection of DCDCs (REG1, REG2)
- Over-voltage of window voltage detection
- Under-voltage of window voltage detection
- Regulator's ON and OFF timeout
- Internal Clock frequency Error

Power Supply (PS) Start Sequence

By a power supply start request in the Power Supply state, each regulator is turned on sequentially.

[Power Supply Start Request]

PWRON: High-level input to the PWRON pin.

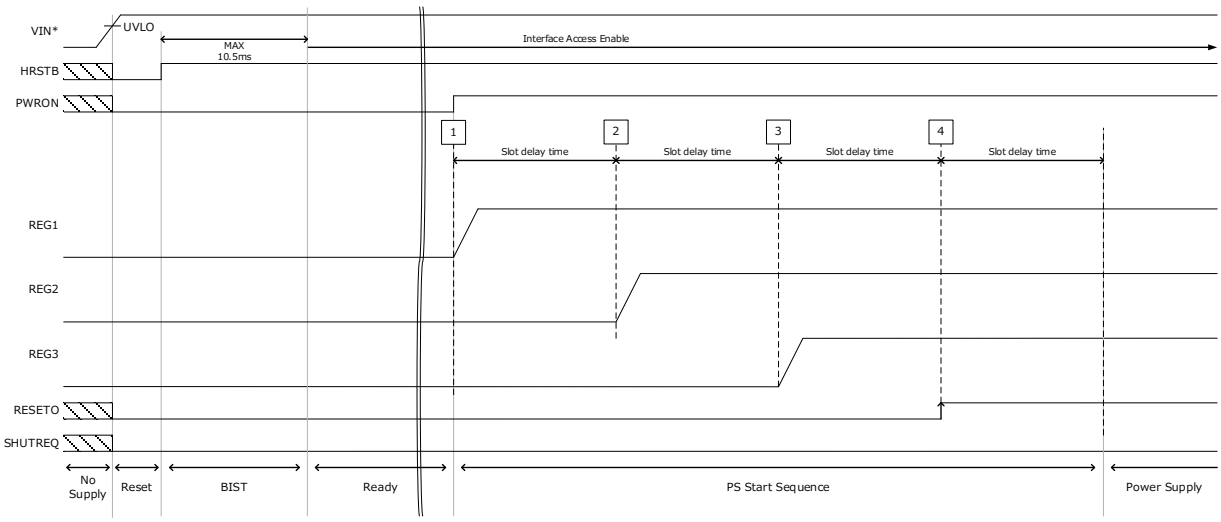


Figure 2 Example of PS Start Sequence

The turn-on sequence of regulators (hereinafter REGs) is programmable. Select the slot number for the on-timing of each REG in the range of 1 to 3. It is able to have a delay time after detection for the on-timing of each REG. The delay value is user-programmable from among 1.8ms, 3.6ms, 7.2ms or 14.4ms (Refer to *"Power Supply Start/Stop Slot Delay Time Setting Register"*).

The following conditions are provided for the example in Figure 2.

- REG1 : Start Slot Number = 1
- REG2 : Start Slot Number = 2
- REG3 : Start Slot Number = 3
- RESETO : Start Slot Number = 4

[Always-on Regulator Power Supply Start Request]

After the completion of BIST, the always-on regulator is turned on to start.

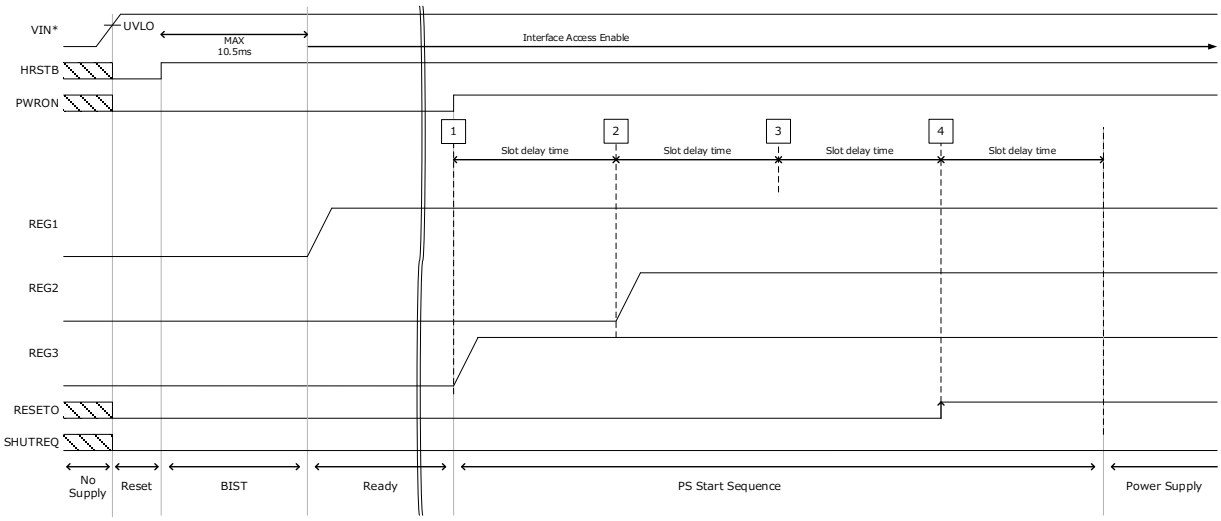


Figure 3 PS Example of Start Sequence with Always-on

Figure 3 is shown the turn-on timing of always-on regulator after the completion of the BIST.
The following conditions are provided for the example in Figure 3.

- REG1 : Always-on
- REG2 : Start Slot Number = 2
- REG3 : Start Slot Number = 1
- RESETO : Start Slot Number = 4

Power Supply (PS) Stop Sequence

By a power supply stop request in the Power Supply state, each regulator is turned off sequentially.

[Power Supply Stop Request]

PWRON: Low-level input to the PWRON pin.

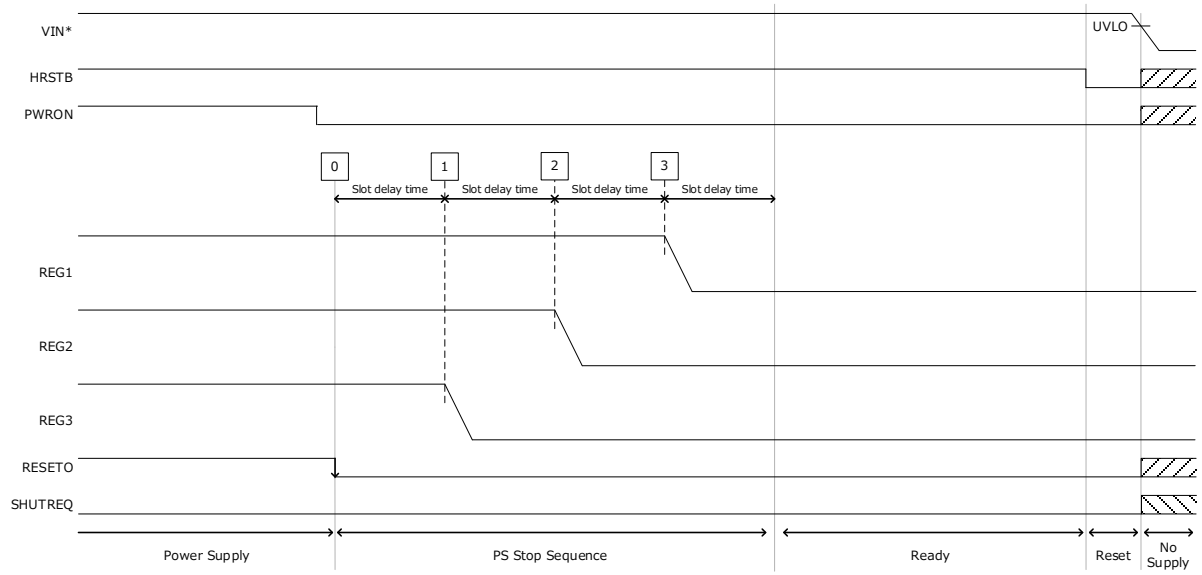


Figure 4 Example of PS Stop Sequence

The turn-off sequence of regulators is programmable. The off-timing of each REG can be delayed from the falling edge of PWRON and the delay value of each regulator is programmable. Select the number of slots for the off-timing of each regulator in the range of 1 to 4. The delay value of one slot is the same as PS Stop Sequence.

The following conditions are provided for the example in Figure 4.

- REG1: Stop Slot Number = 3
- REG2: Stop Slot Number = 2
- REG3: Stop Slot Number = 1

The RESETO pin becomes low-level at the timing of PWRON changed.

Repower Sequence

Once a repower request is detected in the Power Supply state, the state transitions to the PS Stop Sequence state and returns to the Power Supply state via the Ready and the PS Start Sequence states.

[Repower-on Request]

<SWREP>: CPU's writing to a dedicated register.

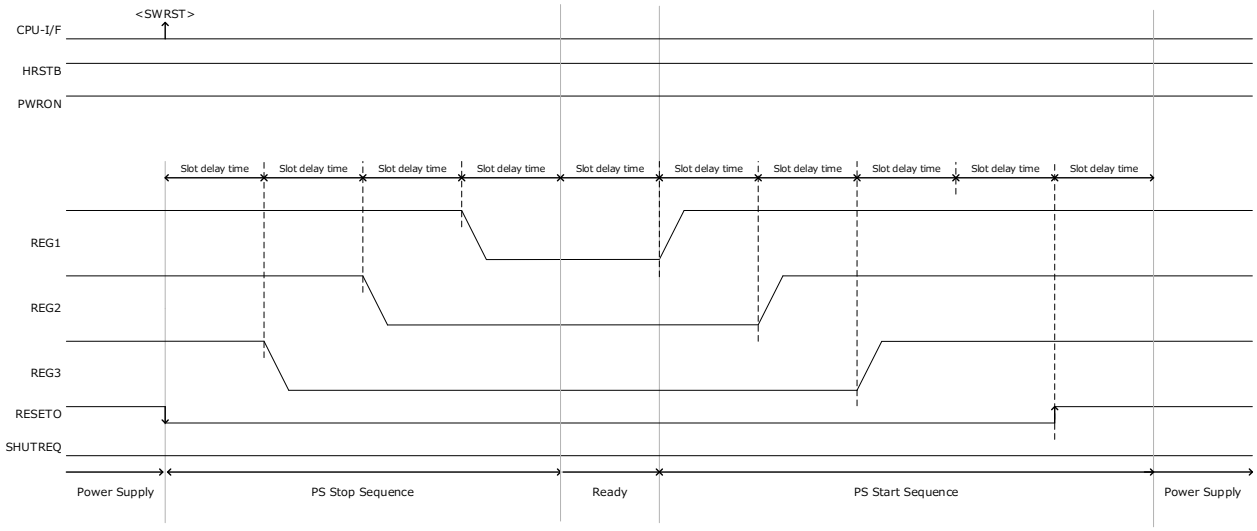


Figure 5 Example of Repower-on Sequence

The following conditions are provided for the example in Figure 5.

- REG1 : Stop Slot Number = 3
- REG2 : Stop Slot Number = 2
- REG3 : Stop Slot Number = 1
- REG1 : Start Slot Number = 1
- REG2 : Start Slot Number = 2
- REG3 : Start Slot Number = 3
- RESETO : Start Slot Number = 5

The RESETO pin becomes low-level at the timing of PWRON changed.

Hardware Reset

If a hardware reset request is detected in any state, the state transitions to the Reset state.

[Hardware Reset Request]

HRSTB: Low-level input to the HRSTB pin.

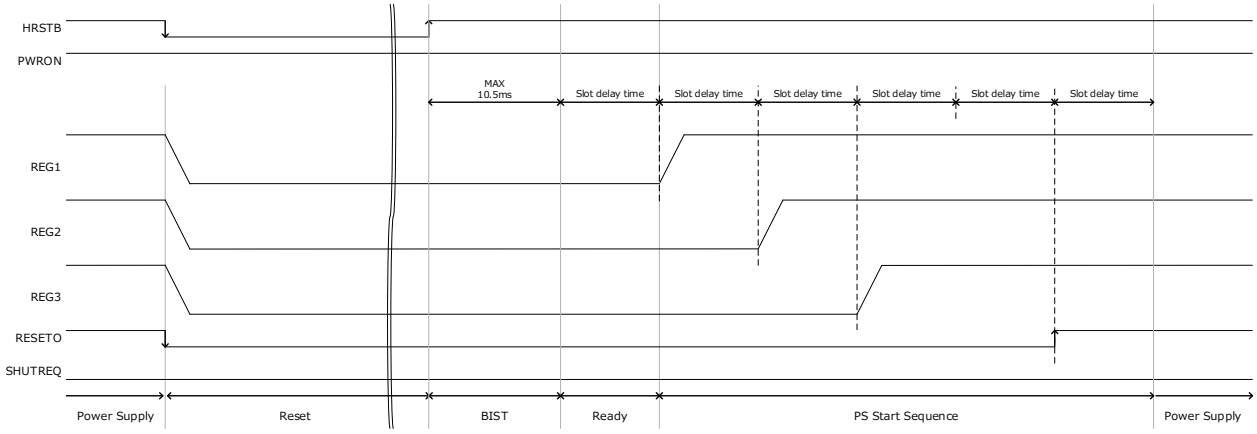


Figure 6 Example of Hardware Reset

The following conditions are provided for the example in Figure 6.

- REG1: Start Slot Number = 1
- REG2: Start Slot Number = 2
- REG3: Start Slot Number = 3

All REGs are turned off, the RESETO pin becomes low-level at the timing of HRSTB changed.

Built-In Self-Test (BIST)

This IC includes Built-in Self-test (BIST) that runs under the following conditions.

・Entering Ready state from Reset state.

・Entering Ready state from any state when register has the BIST request.

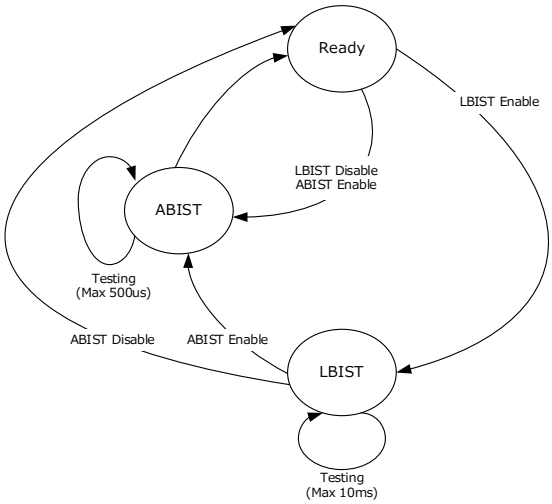


Figure 7 BIST Flow

In the order of the tests, first comes logic (LBIST) and then analog (ABIST). When detecting an error, the BIST generates an interrupt and stores the detected block information in the register.

The target block of analog BIST is as follows.

・EXTDET
・REG3DET
・REG2DET
・REG1DET
・REG3 (LDO)
・REG2 (DCDC)
・REG1 (DCDC)
・IODET
・UVLO_D
・UVLO_A
・VINCMP
・TRIMMING CELL

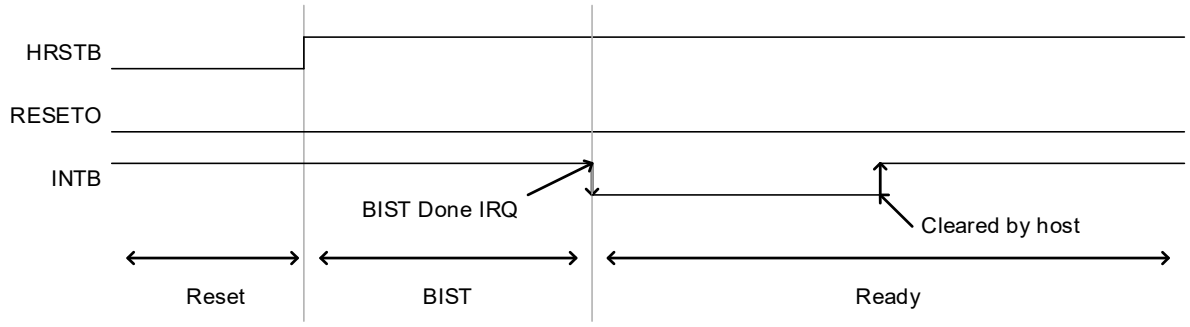


Figure 8 Example of BIST Done IRQ

An interrupt occurs at the completion of BIST. The interrupt can be masked by trimming.

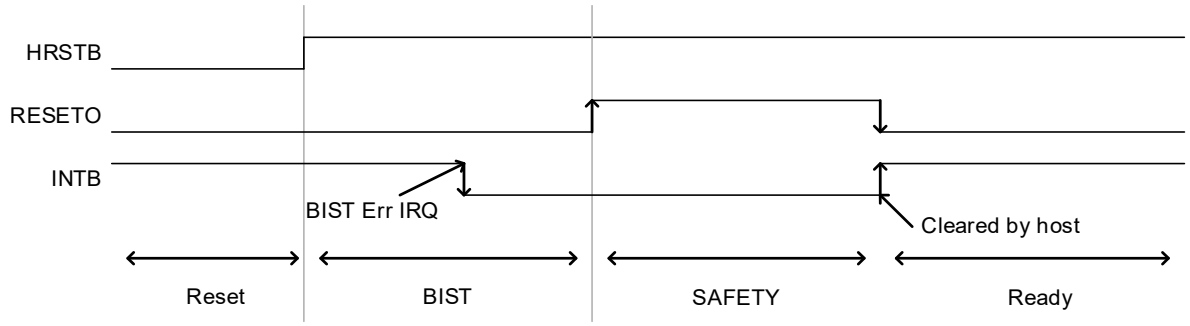


Figure 9 Example of BIST Error IRQ

When detecting an error during the BIST, this device shifts to the Safety state at the completion of the BIST and maintains it until the interrupt factor is cleared.

Safety Mechanism

This IC can detect the following errors.

1. Abnormal Clock Frequency and Clock Stop
2. REGn PS Start Sequence Timeout
3. REGn Soft-start Time Error
4. DCDC Overcurrent Protect
5. REGn Over/Under-Voltage
6. EXDET1 Over/Under Voltage
7. REGn Slot Violation
8. Abnormal RESETO Pin Release
9. VIN Monitor

When detecting an error, this IC performs the following functions.

1. Abnormal Clock Frequency and Clock Stop

When detecting an abnormal oscillation, this IC outputs interrupt request and all REGs are turned off.

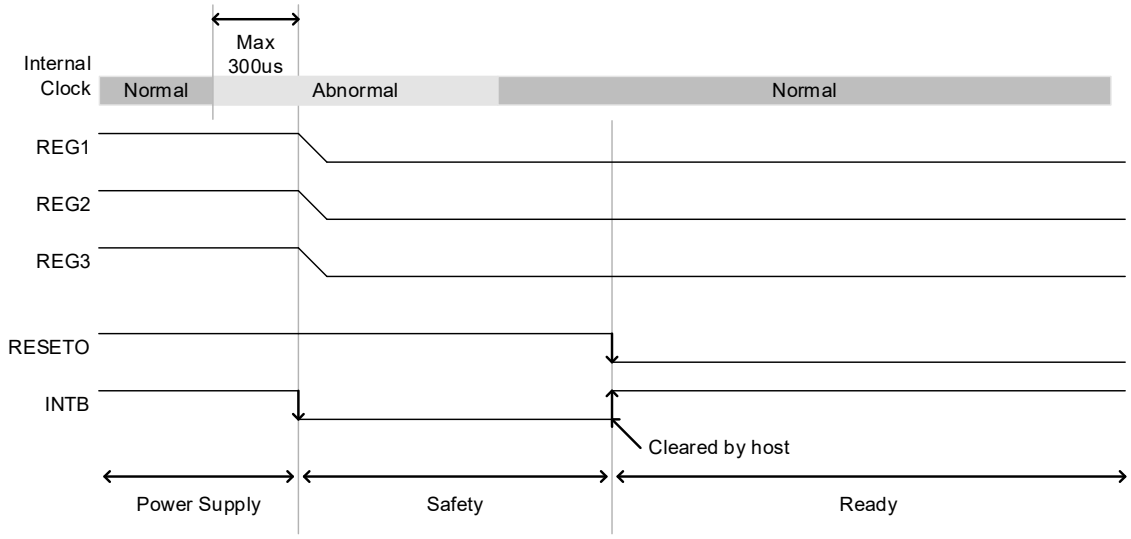


Figure 10 Example of Abnormal Clock

2. REGn PS Start Sequence Timeout

A timeout error indicates that the output of REGn has not reached the target voltage within the slot delay time.

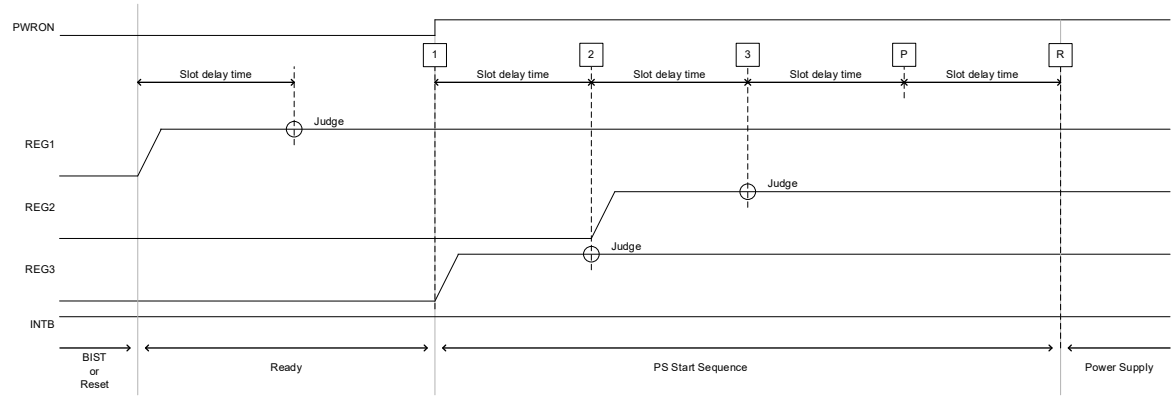


Figure 11 PS Start Timeout Judge Timing

The following conditions are provided for the examples in Figure 8, 9 and 10.

- REG1: Start Slot Number = Always-on
- REG2: Start Slot Number = 2
- REG3: Start Slot Number = 1

When detecting a PS Start timeout, this IC outputs interrupt request and all REGs are turned off.

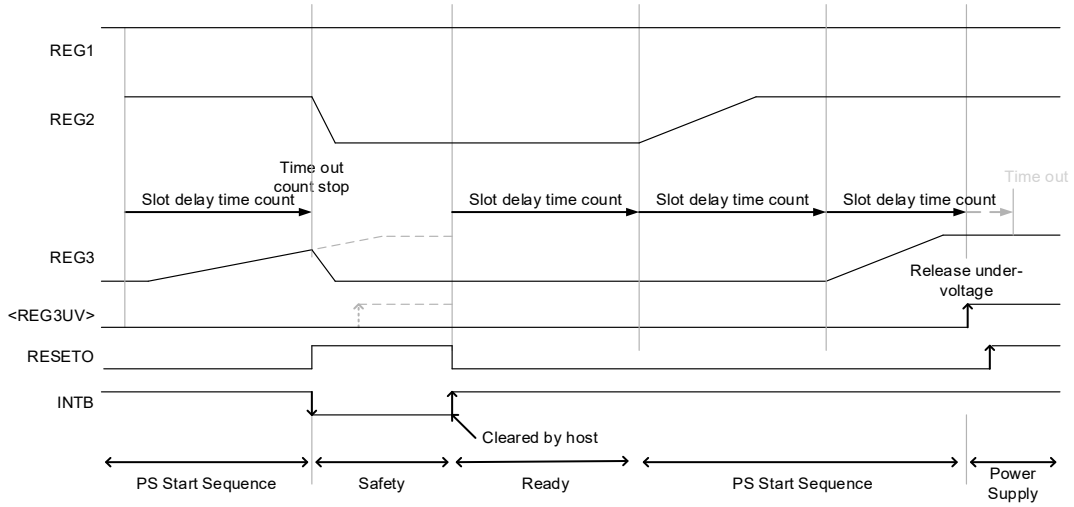


Figure 12 PS Start Timeout Error

3. REGn Soft-start Time Error

The error of soft-start time indicates a short rising time of the REGn output. The count value of soft-start for one-slot is 250 µs (Max.).

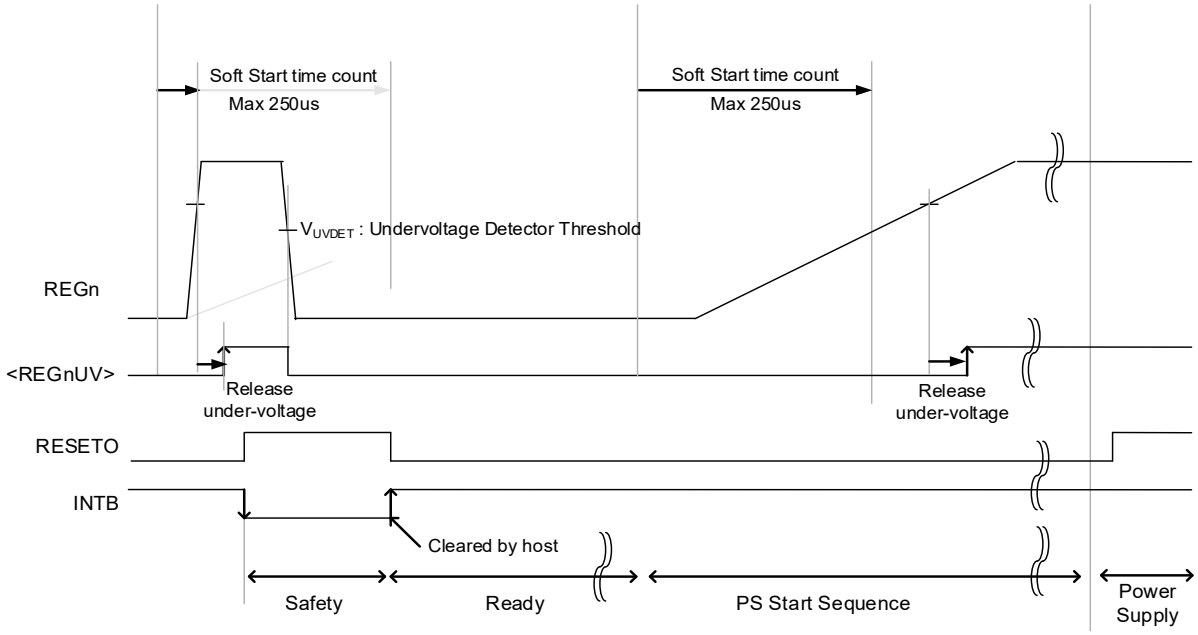


Figure 13 Soft-start Time Error

When the REGn starts within 250 µs (Max.) of the slot-start to release an under-voltage, this IC handles as the REGn soft-start error.

4. **DCDC Overcurrent Protect**

The Step-down DCDC Converter (REG1, REG2) has an overcurrent latch protection circuit to detect continuous overcurrent. When detecting an overcurrent, this IC outputs an interrupt request and all REGs except Always-on REG are turned off.

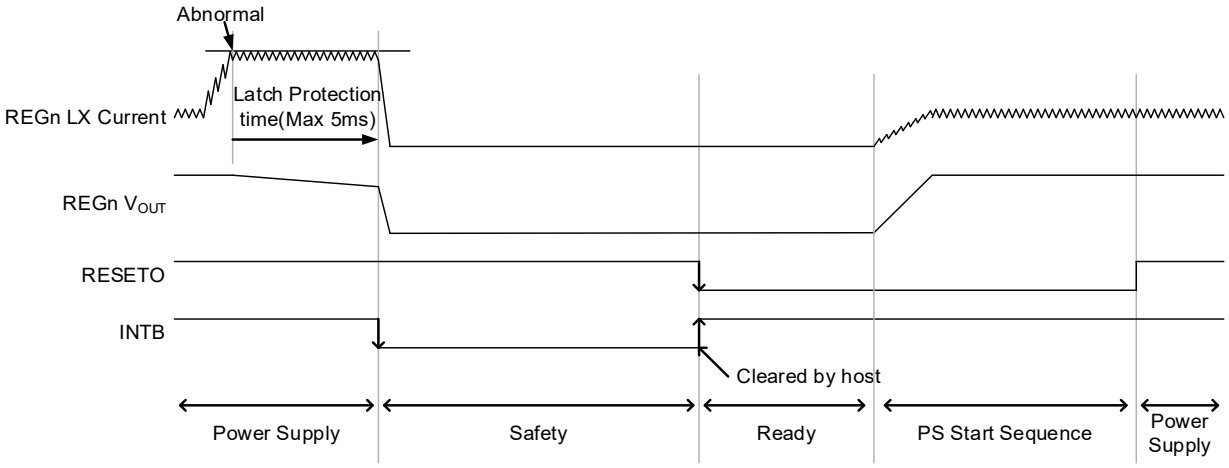


Figure 14 DCDC Overcurrent Error

5. REGn Over/Under-Voltage

The window voltage detector monitors REGn voltage. When detecting over/under-voltage, this IC outputs interrupt request and REGn is turned off.

In addition, it is over-voltage also when it is ON of REGn (except Always-on REG) in the READY State. The turn-off function can disable. In addition, this IC can turn off other REG at the same timing (Refer to “Auto-off setting Register”). If REGn remains on, the RESETO pin also remain on.

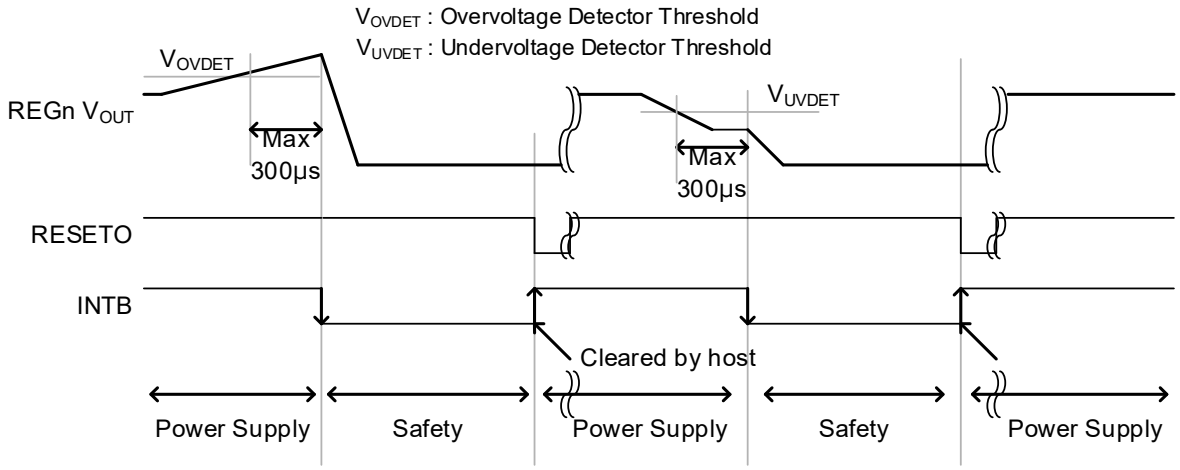


Figure 15 REGn Abnormal Voltage Detection with REG OFF

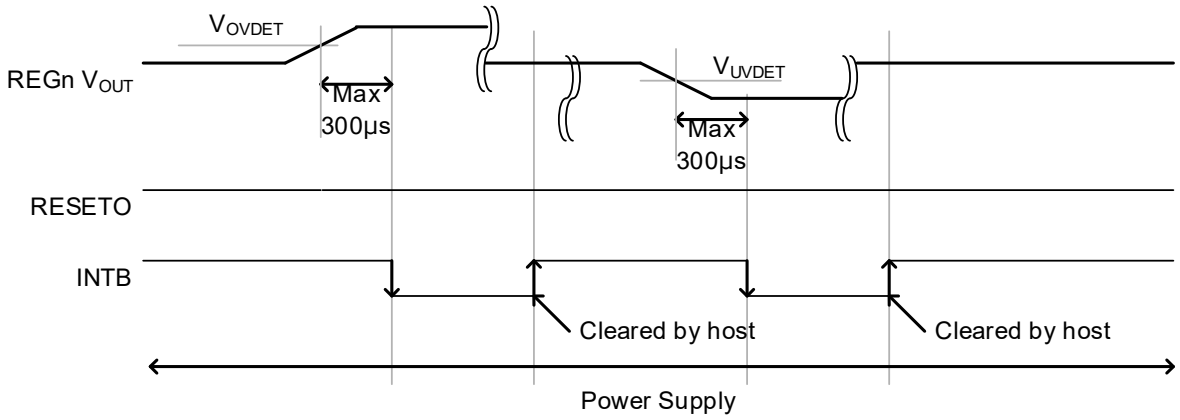


Figure 16 REGn Abnormal Voltage Detection with REG ON

6. EXDET1 Over/Under Voltage

When the window voltage detector monitoring the EXDET1 pin voltage detects an over/under-voltage, this IC outputs the interrupt request only.

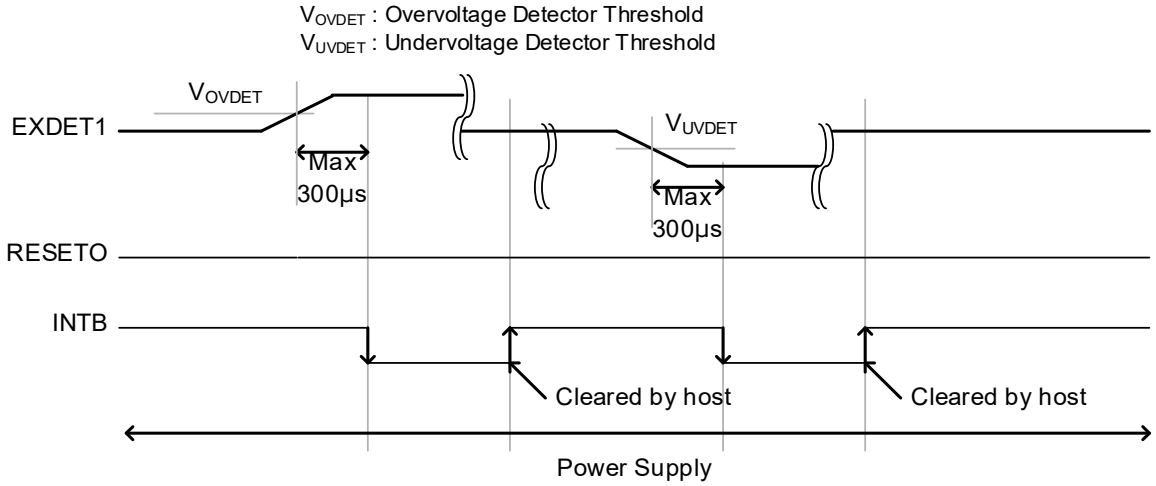


Figure 17 EXDET1 Abnormal Voltage Detection

7. REGn Slot Violation

When detecting the slot violation for the REGn start, this IC generates an interrupt to stop the REGn. The detecting conditions for the slot violation are as follows:

- Don't start REGn in the specified slot.
- Starts REGn in the another except the specified slot.

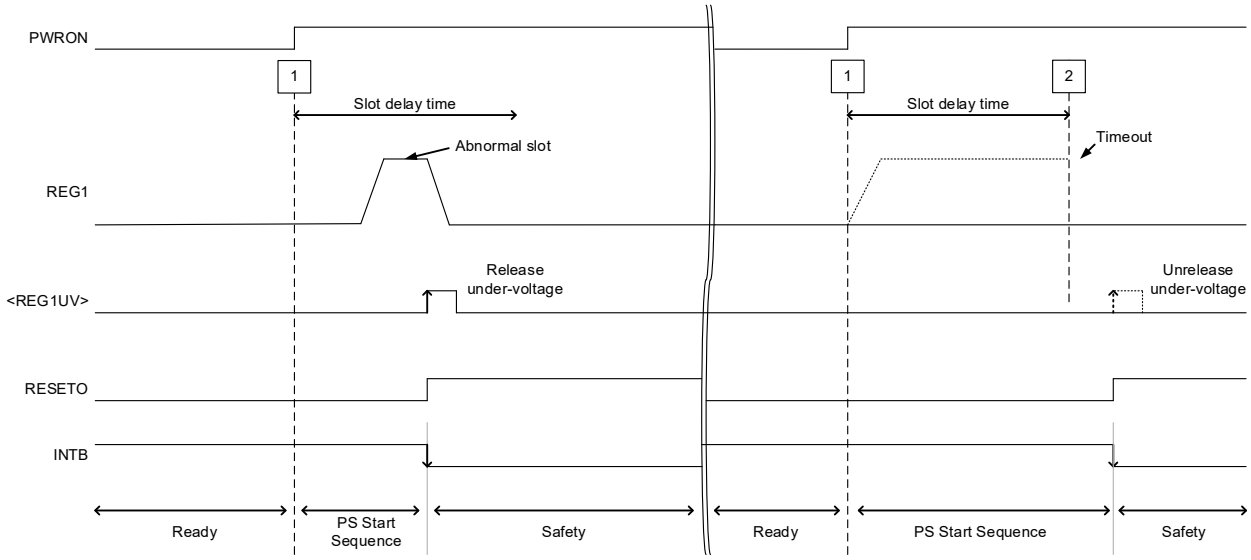


Figure 18 Example of Start Slot Violation

The following condition is provided for the example in Figure 18.

- REG1: Start Slot Number = 2

In this example, when the REG1 starts up before the specified slot (Slot2), this IC handles as an over-voltage detection for REG1. When the REG1 does not start up in the specified slot, this IC handles as timeout for REG1.

This IC works as for the above cases even if an error occurs in the slot period. For example, if the slot period becomes short, this IC handles as a timeout because the REGn does not start up.

8. Abnormal RESETO Pin Release

The IC monitors the status of the RESETO pin. When detecting an abnormal reset release, this IC outputs an interrupt request and turns all REGn off.

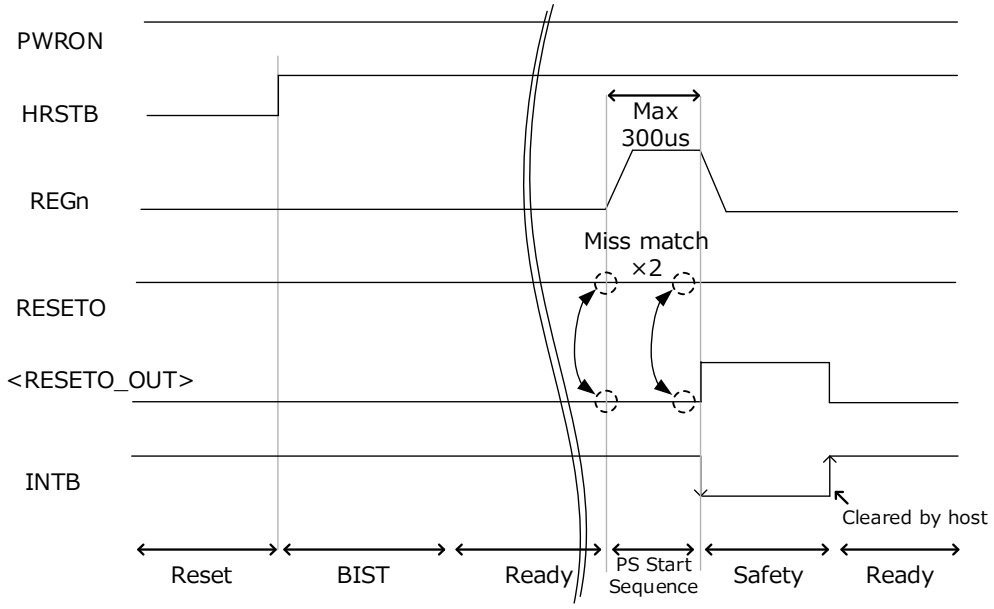


Figure 19 Abnormal RESETO Release

9. VIN Monitor

This IC monitors the voltages for VINA and VIND pins all the time. When detecting a low-voltage or an abnormal voltage-difference between the pins, this IC is shut down.

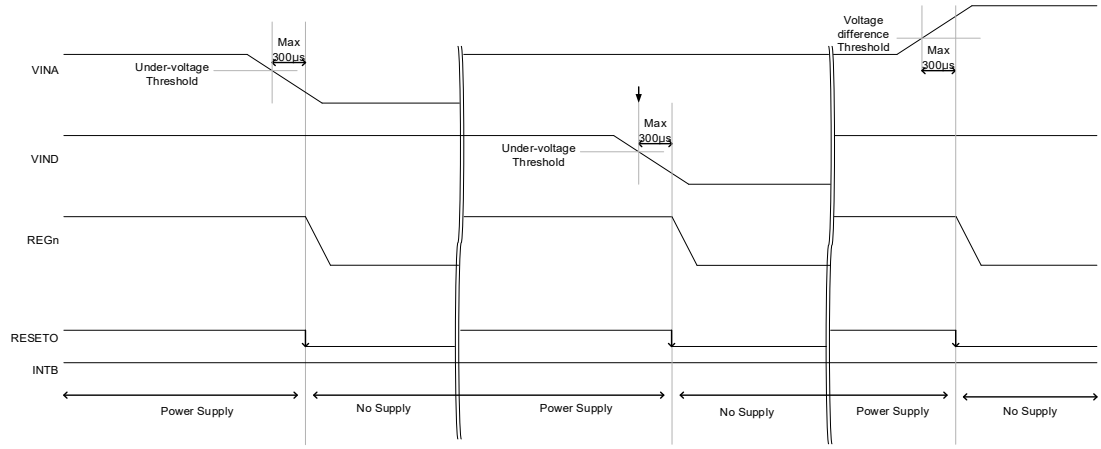


Figure 20 VIN Monitor

Auto-restoration Sequence

Auto-restoration Sequence

The auto-restoration functions at the error (1) detection. The auto-restoration time is able to select from 0 to 3 (Refer to “System Control Register”). If the error detection times is not more than it, the error flag is cleared automatically and the state transitions to the Power Supply state via the Ready and the PS Start Sequence state.

[Auto-restoration Condition]

The error detection times is not more than the auto-restoration times (ATRENUM bits).

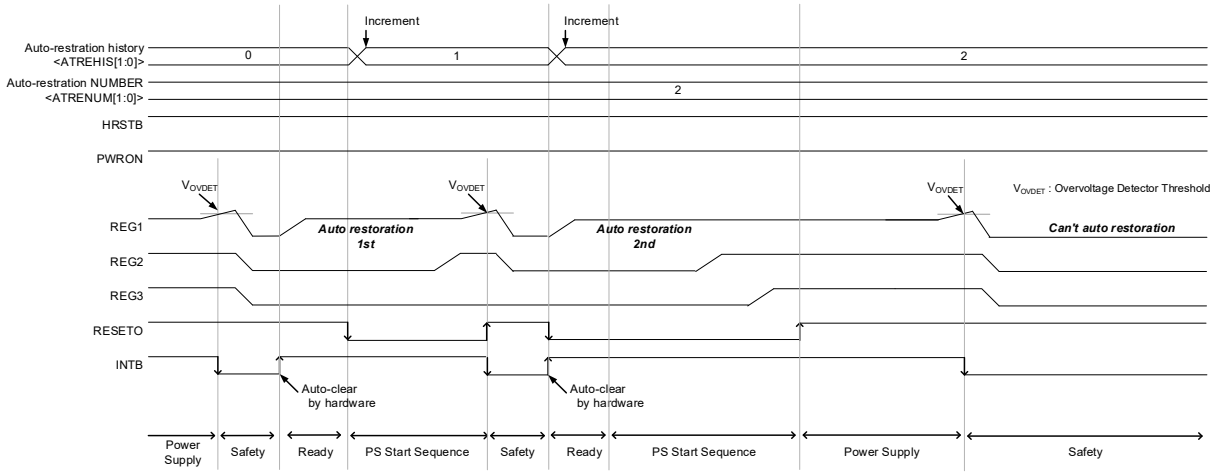


Figure 21 Auto-restoration Sequence

The following conditions are provided for the example in Figure 22.

- REG1: Always-on
- REG2: Slot On
- REG3: Slot On

(1) The errors are shown below.
- Overcurrent / Reverse current Protection of DCDCs (REG1, REG2)
- Over-voltage of window voltage detection of REGn
- Under-voltage of window voltage detection of REGn
- Timeout of power supply sequence
- Short rise time of REGn Soft-start
- Detection of abnormal temperature

Interrupt Controller (INTC)

This IC has an open-drain output INTB (Interrupt) pin. This pin is used to indicate an interrupt request state. "Hiz" is non-request. "Low" is request.

Interrupt Request factors are as follows.

- Detection and release of abnormal temperature
- Over-voltage output of REGn
- Under-voltage output of REGn
- Overcurrent and reverse current of DCDCs (REG1, REG2)
- Timeout of power supply sequence
- Short rise time of REGn soft-start.
- EXDET1 pin over-voltage detection
- EXDET1 pin under-voltage detection
- BIST error detection
- I^2C error
- BIST done

The interrupt request is set in the INTREQ register by this IC and cleared by host writing “1”. The flag can be masked with the unmask register.

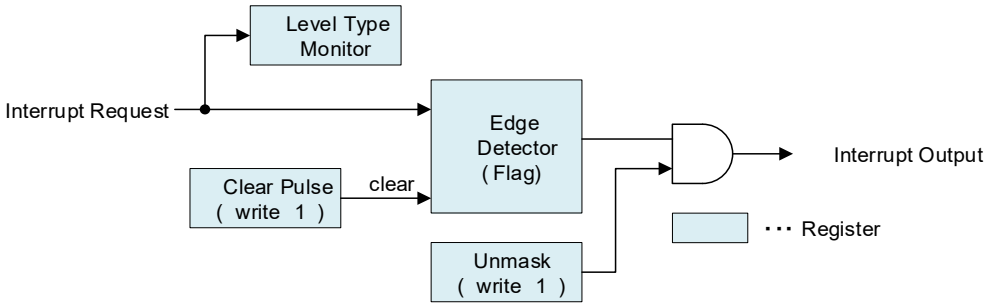


Figure 22 INTC Block Diagram

Note: When using the interrupt controller, the pull-up resistance of 10 kΩ to 100 kΩ for INTB pin is recommended. When not using it, the INTB pin must be left floating or connected to GND.

Shut-down Request (SHUTREQ)

The SHUTREQ pin is used to protect against an error that cannot turn off REG1,2,3 of this IC. It is assumed that the power supply from primary DCDC will be stopped by receiving the output of the SHUTREQ pin.

The SHUTREQ pin issues a request to shut this IC down when the following factor occurs.

- Over-voltage output of REGn
- Under-voltage output of REGn
- Overcurrent and reverse current of DCDCs (REG1, REG2)
- Short rise time of REGn soft-start
- REGn PS Start sequence timeout

These factors can be masked in the register. The occurrence of a masked factor causes a transition to the Safety state, but the SHUTREQ pin keeps Low output.

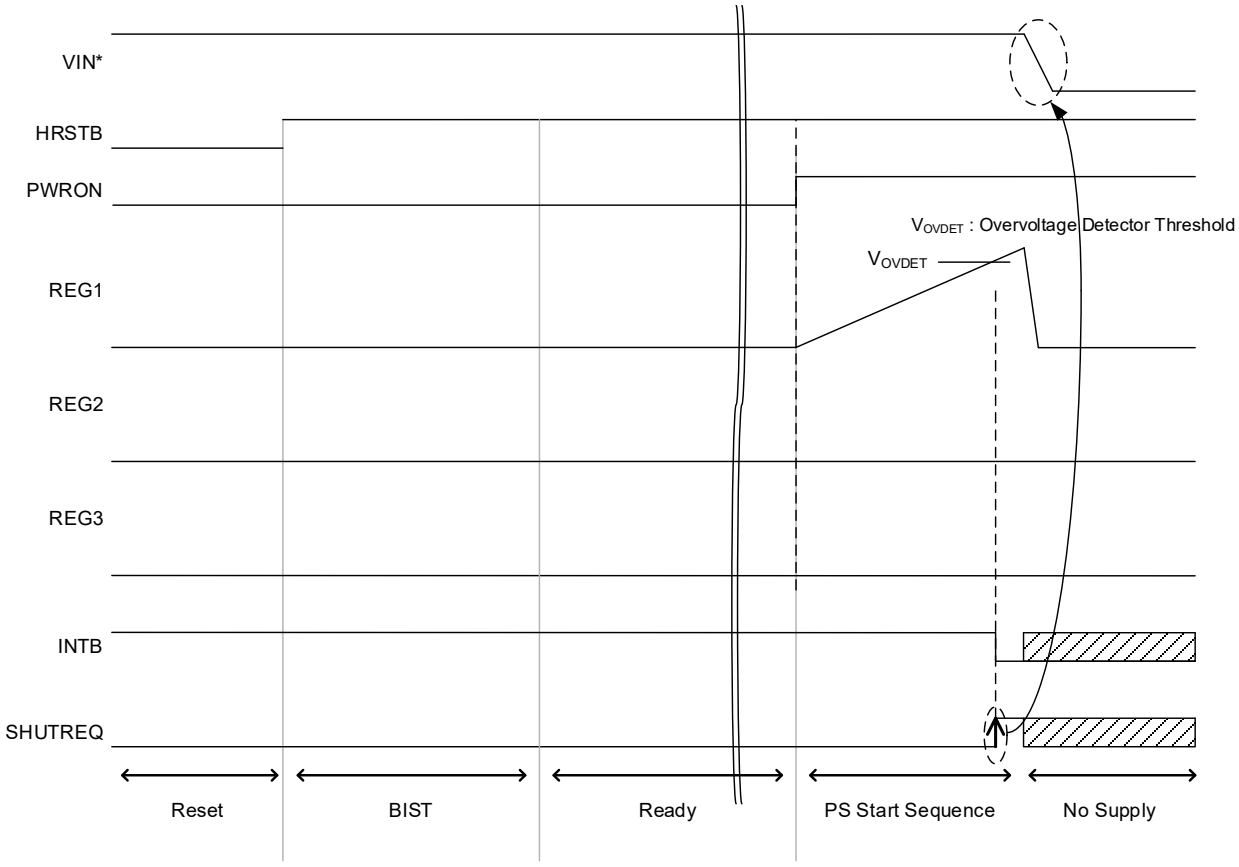


Figure 23 Shutdown Request (Ex:REG1 Over-voltage)

VOLTAGE DETECTOR

Electrical Characteristics

V_{SYS} = V_{SYS_TYP}, unless otherwise specified.

REG1DET, REG2DET Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{OVRANGE}$	Overvoltage (OV) Detector Threshold Range	-		0.6		3.7	V
$V_{UVRANGE}$	Undervoltage (UV) Detector Threshold Range			0.6		3.7	V
V_{OVDET}	Overvoltage (OV) Detector Threshold	V_{OVDET} ≥ 1.0V	Ta = 25°C	× 0.99	V_{OVDET} (1)	× 1.01	V
			–40°C ≤ Ta ≤ 125°C	× 0.985	V_{OVDET} (1)	× 1.011	V
		V_{OVDET} < 1.0V	Ta = 25°C	× 0.987	V_{OVDET} (1)	× 1.013	V
			–40°C ≤ Ta ≤ 125°C	× 0.976	V_{OVDET} (1)	× 1.016	V
V_{UVDET}	Undervoltage (UV) Detector Threshold	V_{UVDET} ≥ 1.0V	Ta = 25°C	× 0.99	V_{UVDET} (1)	× 1.01	V
			–40°C ≤ Ta ≤ 125°C	× 0.985	V_{UVDET} (1)	× 1.011	V
		V_{UVDET} < 1.0V	Ta = 25°C	× 0.987	V_{UVDET} (1)	× 1.013	V
			–40°C ≤ Ta ≤ 125°C	× 0.976	V_{UVDET} (1)	× 1.016	V
$t_{OVDELAY}$	OV Detect Delay Time					300	µs
$t_{UVDELAY}$	UV Detect Delay Time					300	µs

REG3DET Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{OVRANGE}$	Overvoltage (OV) Detector Threshold Range	-	2.0		4.0	V
$V_{UVRANGE}$	Undervoltage (UV) Detector Threshold Range		2.0		4.0	V
V_{OVDET}	Overvoltage (OV) Detector Threshold	Ta = 25°C	× 0.99	V_{OVDET} (1)	× 1.01	V
		–40°C ≤ Ta ≤ 125°C	× 0.985	V_{OVDET} (1)	× 1.011	V
V_{UVDET}	Undervoltage (UV) Detector Threshold	Ta = 25°C	× 0.99	V_{UVDET} (1)	× 1.01	V
		–40°C ≤ Ta ≤ 125°C	× 0.985	V_{UVDET} (1)	× 1.011	V
$t_{OVDELAY}$	OV Detect Delay Time				300	µs
$t_{UVDELAY}$	UV Detect Delay Time				300	µs

(1) V_{OVDET} and V_{UVDET} are selectable by trimming.

EXTDET Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{OVRANGE}$	Overvoltage (OV) Detector Threshold Range	-		0.6		3.7	V
$V_{UVRANGE}$	Undervoltage (UV) Detector Threshold Range			0.6		3.7	V
V_{OVDET}	Overvoltage (OV) Detector Threshold	V_{OVDET} ≥ 1.0V	Ta = 25°C	× 0.99	V_{OVDET} (1)	× 1.01	V
			–40°C ≤ Ta ≤ 125°C	× 0.985	V_{OVDET} (1)	× 1.011	V
		V_{OVDET} < 1.0V	Ta = 25°C	× 0.987	V_{OVDET} (1)	× 1.013	V
			–40°C ≤ Ta ≤ 125°C	× 0.976	V_{OVDET} (1)	× 1.016	V
V_{UVDET}	Undervoltage (UV) Detector Threshold	V_{UVDET} ≥ 1.0V	Ta = 25°C	× 0.99	V_{UVDET} (1)	× 1.01	V
			–40°C ≤ Ta ≤ 125°C	× 0.985	V_{UVDET} (1)	× 1.011	V
		V_{UVDET} < 1.0V	Ta = 25°C	× 0.987	V_{UVDET} (1)	× 1.013	V
			–40°C ≤ Ta ≤ 125°C	× 0.976	V_{UVDET} (1)	× 1.016	V
R_{SENSE}	SENSE Resistance	V_{OVDET} = 1.2V, V_{UVDET} = 1.0V		0.5	1.2	2.5	MΩ
$t_{OVDELAY}$	OV Detect Delay Time					300	µs
$t_{UVDELAY}$	UV Detect Delay Time					300	µs

UVLO Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DET}	Detect Voltage		2.5	2.55	2.6	V
V_{REL}	Release Voltage		2.55		2.7	V
t_{DELAY}	Detect Delay Time	C_{IN} = 1µF			300	µs

VINCMP Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DET_VIND}	VIND-VINA Detect Voltage		0.3		1.0	V
V_{DET_VINA}	VINA-VIND Detect Voltage		0.3		1.0	V
t_{DELAY}	Detect Delay Time	C_{IN} = 1µF			300	µs

IODET Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DET}	Detect Voltage		1.6	1.63	1.66	V
V_{REL}	Release Voltage		1.62		1.70	V
t_{DELAY}	Detect Delay Time				300	µs

(1) V_{OVDET} and V_{UVDET} are selectable by trimming.

REGULATOR

DCDC (REG1, REG2) Electrical Characteristics

V_{SYS} = V_{SYS_TYP}, unless otherwise specified.

REG1, REG2 Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	× 0.99	V_{SET} (1)	× 1.01	V
		−40°C ≤ Ta ≤ 125°C	× 0.97	V_{SET} (1)	× 1.03	
I_{LXLIM1}	LX Current Limit1	I_{OUTMAX} = 600 mA Ver (2)	900	1400	1900	mA
I_{LXLIM2}	LX Current Limit2	I_{OUTMAX} = 1000 mA Ver (2)	1300	1900	2600	mA
t_{PROT}	Protection Delay Time		0.5	1.5	5	ms
t_{PROT_REV}	Protection Delay Time (Reverse Current)		0.5	1.5	5	ms
I_{REVLIM}	Reverse Current Limit		–2700	–1400	–600	mA
f_{OSC}	LX Oscillator Frequency		2.0	2.3	2.5	MHz
t_{START}	Soft-start Time	Time from Enable to 90% of V_{OUT}	× 0.5	t_{SET} (3)	× 2.0	ms
R_{LOW}	On Resistance of Low Output	V_{SYS} = 3.0V, VOUT1, 2 = 0.1V		5	18	Ω

Test circuit is operated with “Open Loop Control” (GND = 0 V), unless otherwise specified.

(1) V_{SET} is selectable from 1.0 V to 3.3 V by trimming.
V_{SET} must be less than or equal to “V_{SYS} (Min.) -1.0V”.
(2) I_{OUTMAX} is selectable from 600mA / 1000mA by trimming.
(3) t_{SET} is selectable from four set times (0.5 / 1.0 / 2.0 / 4.0 ms) by trimming.

OSC Electrical Characteristics

V_{SYS} = V_{SYS_TYP}, unless otherwise specified.

OSC23M1, OSC23M2 Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency		2.0	2.3	2.5	MHz
f_{DIFF}	Frequency Difference	OSC23M1 - OSC23M2	–146		149	kHz
f_{DETL1}	OSC23M1 Low Frequency Detect Threshold	OSC23M2 = 2MHz	1.854			MHz
f_{DETH1}	OSC23M1 High Frequency Detect Threshold	OSC23M2 = 2.5MHz			2.702	MHz
f_{DETL2}	OSC23M2 Low Frequency Detect Threshold	OSC23M1 = 2MHz	1.850			MHz
f_{DETH2}	OSC23M2 High Frequency Detect Threshold	OSC23M1 = 2.5MHz			2.698	MHz
t_{DELAY}	Detect Delay Time				300	µs

LDO (REG3) Electrical Characteristics

V_{SYS} = V_{SYS_TYP}, I_{OUT} = 1 mA, unless otherwise specified.

REG3 Electrical Characteristics (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	× 0.99	V_{SET} (1)	× 1.01	V
		−40°C ≤ Ta ≤ 125°C.	× 0.985	V_{SET} (1)	× 1.015	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	1 mA ≤ I_{OUT} ≤ 200 mA	–10	5	10	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 200 mA			200	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{SET} (1) +0.5 V ≤ V_{SYS} ≤ 5.5 V,		0.02	0.10	%/V
I_{LIM1}	Limit Current1	I_{OUTMAX} = 100 mA Ver (2)	100	140	180	mA
I_{LIM2}	Limit Current2	I_{OUTMAX} = 200 mA Ver (2)	200	280	360	mA
I_{SC}	Short Current Limit	V_{OUT} = 0 V	40	75	100	mA
t_{START}	Soft-start Time	Time from Enable to 90% of V_{OUT}	× 0.5	t_{SET} (3)	× 2.0	ms
R_{LOW}	On Resistance of Low Output	V_{SYS} = 3.0V, V_{OUT3} = 0.1V		15	30	Ω

(1) V_{SET} is selectable from 2.5 V to 3.5 V by trimming.
V_{SET} must be less than or equal to "V_{SYS}(Min.) – 0.5 V".
(2) I_{OUTMAX} is selectable from 100mA / 200mA by trimming.
(3) t_{SET} is selectable from four set times (0.5 / 1.0 / 2.0 / 4.0 ms) by trimming.

I²C-BUS INTERFACE

This IC supports the I²C-bus system with two-wires for connecting the CPU. Connection and Transfer system of the I²C-bus are described in the following sections.

I²C-Bus Operation

Within the procedure of I²C-bus, unique situations arise which are defined as start and stop conditions.

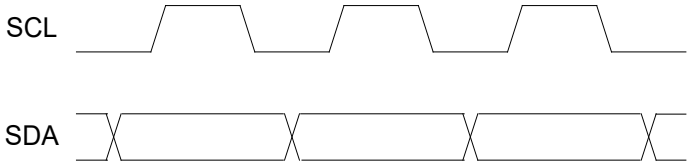


Figure 24 I²C-Bus Data Transmission

A “High” to “Low” transition on SDA line while SCL is “High” indicates a start condition. A “Low” to “High” transition on SDA line while SCL is “High” defines a stop condition. Start and stop conditions are always generated by master (Refer to the figure below). The bus is considered to be busy after start condition. The bus is considered to be free again a certain time after the stop condition.

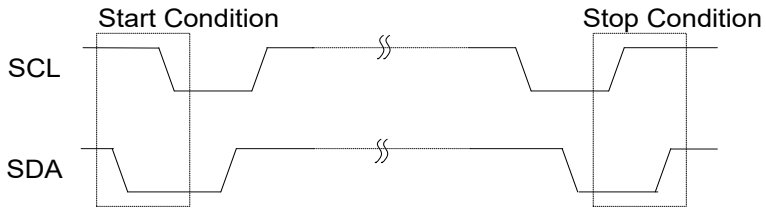


Figure 25 I²C-Bus Start / Stop Condition

AC Characteristics of I²C-Bus

V_{INIO} = 1.8 V, C_B (1) = 550 pF (Max.), unless otherwise specified.

Fast-mode Plus (Fm+) (–40°C ≤ Ta ≤ 125°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	-			1000	kHz
t_{BUF}	Bus Free Time Between a Precedent and Start	-	0.5		-	µs
t_{LOW}	SCL Clock Time, “Low”	-	0.5		-	µs
t_{HIGH}	SCL Clock Time, “High”	-	0.26		-	µs
$t_{SU;STA}$	Start Condition Setup Time	-	0.26		-	µs
$t_{HD;STA}$	Start Condition Hold Time	-	0.26		-	µs
$t_{SU;STO}$	Stop Condition Setup Time	-	0.26		-	µs
$t_{HD;DAT}$	Data Hold Time	-	0			µs
$t_{SU;DAT}$	Data Setup Time	-	50		-	ns
t_R	Rising Time of SCL and SDA (Input)	-			120	ns
t_F	Falling Time of SCL and SDA (Input)	-			120	ns
t_{SP}	Suppressing Pulse Width	-	0		50	ns

Note: All the above-mentioned values are corresponding to V_{IH} min and V_{IL} max level.

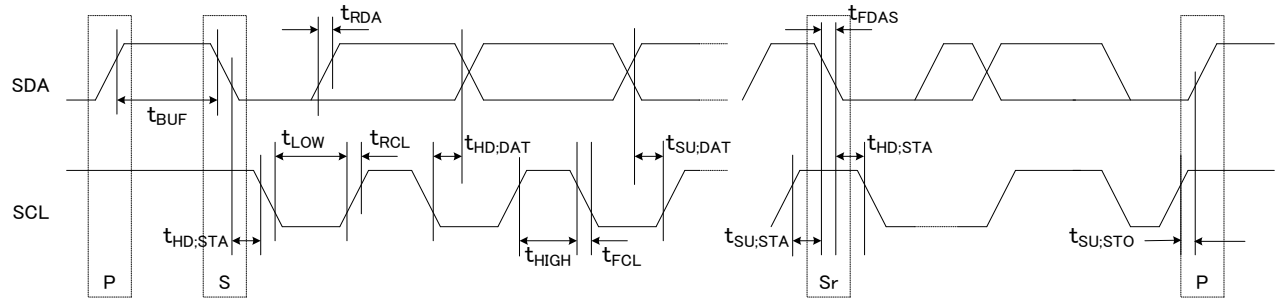


Figure 26 I²C-Bus Interface Timing Chart

I²C-Bus Internal Register Write-in Timing

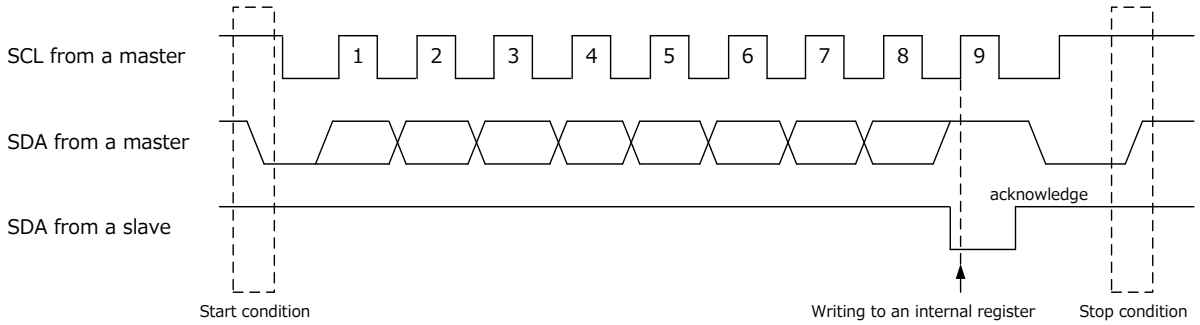


Figure 27 I²C-Bus Write timing

(1) C_B: Capacitive load for each bus line

I²C-Bus Data Transmission and Its Acknowledge

After start condition, data is transmitted by 1-byte (8-bit). The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit. Data transmission with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases SDA line during the acknowledge clock pulse. The receiver must pull down SDA line during the acknowledge clock pulse so that SDA line remains stable “Low” during the “High” period of the acknowledge clock pulse. If a master-receiver is involved in a transfer, it must signal the end of the data to the slave-transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop condition.

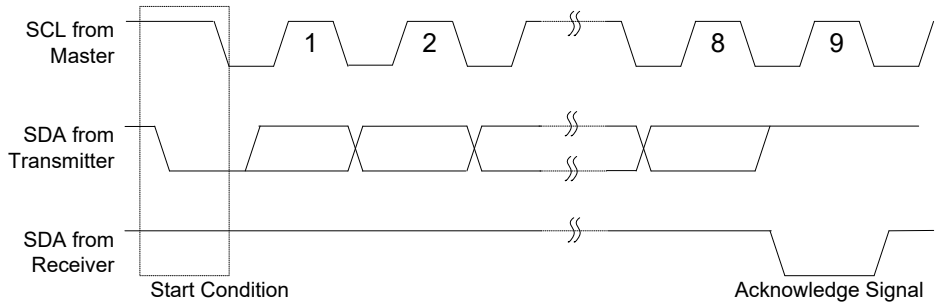


Figure 28 I²C-Bus ACK

I²C-Bus Slave Address

After start condition, a slave address is sent. The address is 7-bit long followed by an 8-bit which is data direction bit (Read/Write). The slave address of this IC is selectable by trimming and pin.

	A7	A6	A5	A4	A3 (1)	A2 (2)	A1 (3)
Slave Address	0	1	1	0	X	X	X

Figure 29 I²C-Bus Slave Address

(1) A [3] of the slave address is selectable by trimming.
(2) A [2] of the slave address are selectable by SLV2 pin. The state of SLV2 pin is stored when the reset is released.
(3) A [1] of the slave address are selectable by SLV1 pin. The state of SLV1 pin is stored when the reset is released.

I²C-Bus Data Transmission Read Format

In order to read the internal register data:

- Specify an internal address pointer (8-bit).
- Generate the repeated start condition to change the data transmission direction to read.

With a start of read mode, automatic increment in address pointers will be made. Read mode is repeated until stop condition is initiated.

The format for read processing after the start condition consists as shown in the following figure.

1st byte: Slave address + Write instruction

2nd byte: Address for the internal register from which the data is to read.

3rd byte: Slave address + Read instruction

4th byte: Data read out from the address specified in the second byte.

5th byte: CRC data

The CRC data is an 8-bit data to indicate the result of the CRC error detection. The CRC data to the 16-bit data (In continuous reading, an 8-bit data immediately before the second and subsequent byte) immediately after restarting is given by the following polynomial.

$$C(x) = X^8 + X^2 + X^1 + 1$$

After the completion of the data transfer in the 5th byte, the master issues a non-acknowledgement signal and a stop condition continuously. After reading out, no enter of the non-acknowledgement and the stop condition, it is possible to read the data continuously. Then, the target address is incremented.

An example of the continuous read format is as follows:

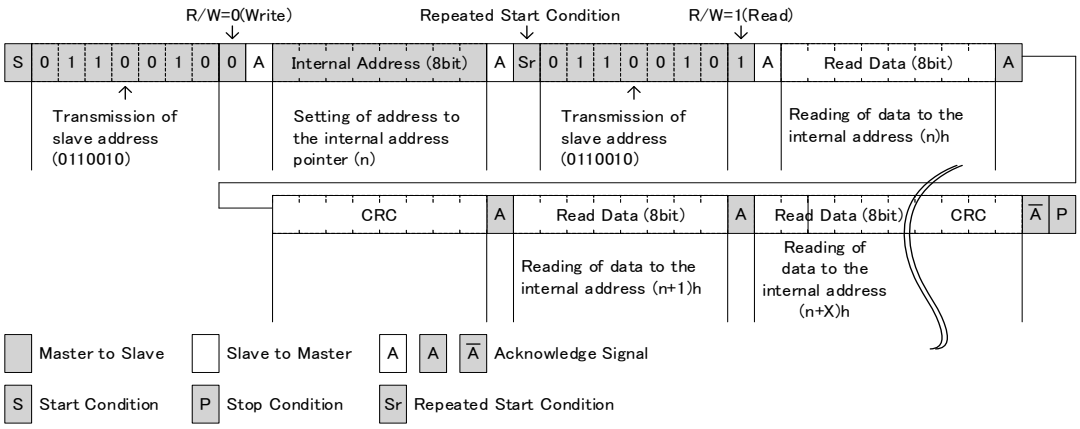


Figure 30 I²C-Bus Read Format

I²C-Bus Data Transmission Write Format

The transmission format for the slave address allocated to each IC is defined in the I²C-bus standard, but transmission method of address information of each IC is not defined. This IC transmits command data. For the data transmission, please transmit MSB first from master and following data in sequence.

The format for write processing after the start condition consists as shown in the following figure.
1st byte: Slave address + Write instruction
2nd byte: Address for internal register to which the data to write.
3rd byte: Data to write in the second byte.
4th byte: CRC data.

The CRC data is an 8-bit data to indicate the result of the CRC error detection. The CRC data to the 24-bit data (In continuous writing, an 8-bit data immediately before the second and subsequent byte) immediately after starting is given by the following polynomial.

$$C(x) = X^8 + X^2 + X^1 + 1$$

After writing the data, the stop condition is required. If transferring the data, which must be written into the register at the next address, and the CRC data by bypassing the stop condition, it is possible to write the data continuously. This IC determines whether a receive error is detected or not when the LSB of the CRC data is received. The interrupt occurs at detecting error (max. 50μs), but no transition to the Safety state occurs. Then, the target address is incremented. An example of the continuous write format is as follows:

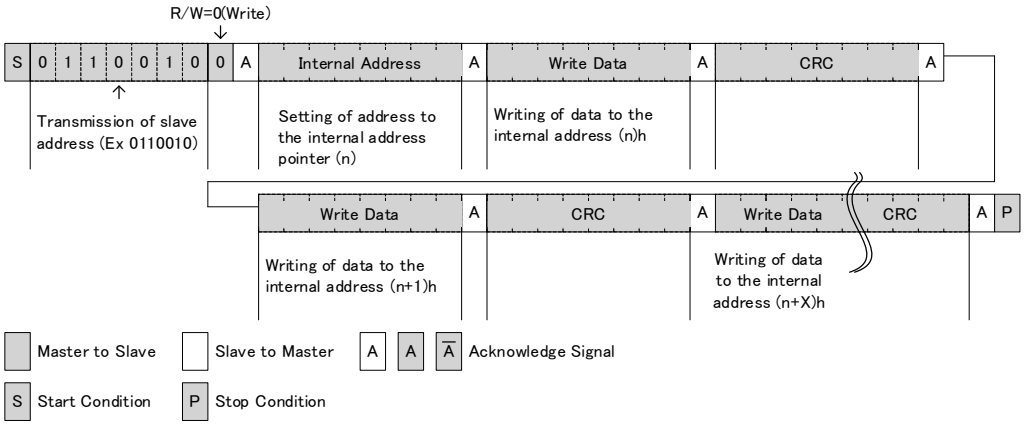


Figure 31 I²C-Bus Write Format

TRIMMING

The RN5T5611 functions and initial settings can be laser-trimmed as user required at shipping. Some functions are changeable by a programming via the I²C-bus after startup.

Item	Description		Register(1)	Set Values
System	A3 Bit in I²C Slave Address		-	0: 0, 1: 1
	Mask of BIST Completion Interrupt		26h[7]	0: Mask, 1: UnMask
	Auto-restoration times		-	0: 0, 1: 1, 2: 2, 3: 3
Sequence	Slot Width		-	0: 1.8ms, 1: 3.6ms, 2: 7.2ms, 3: 14.4ms
	Power-on Slot	REG1	-	0: Always ON, 1: Slot_1, 2: Slot_2, 3: Slot_3
		REG2	-	1: Slot_1, 2: Slot_2, 3: Slot_3
		REG3	-	1: Slot_1, 2: Slot_2, 3: Slot_3
	Power-off Slot	REG1	-	0: Slot_0, 1: Slot_1, 2: Slot_2, 3: Slot_3
		REG2	-	0: Slot_0, 1: Slot_1, 2: Slot_2, 3: Slot_3
		REG3	-	0: Slot_0, 1: Slot_1, 2: Slot_2, 3: Slot_3
	RESETO Output Slot		-	1: Slot_1, 2: Slot_2, 3: Slot_3, 4: Slot_4, 5: Slot_5
REGn	Output Voltage	REG1	-	1.00V ≤ Source ≤ 3.30V (in 50mV step)
		REG2	-	1.00V ≤ Source ≤ 3.30V (in 50mV step)
		REG3	-	2.50V ≤ Source ≤ 3.50V (in 50mV step)
	Soft-start Time	REG1	-	0: 0.5ms, 1: 1.0ms, 2: 2.0ms, 3: 4.0ms
		REG2	-	0: 0.5ms, 1: 1.0ms, 2: 2.0ms, 3: 4.0ms
		REG3	-	0: 0.5ms, 1: 1.0ms, 2: 2.0ms, 3: 4.0ms
	Current Limit	REG1	-	0: 1400mA, 1: 1900mA
		REG2	-	0: 1400mA, 1: 1900mA
		REG3	-	0: 100mA, 1:200mA
DETn	REG1DET	OV Detection	11h[7:0]	0.60V ≤ Source ≤ 3.70V (in 12.5mV step)
		UV Detection	10h[7:0]	0.60V ≤ Source ≤ 3.70V (in 12.5mV step)
	REG2DET	OV Detection	13h[7:0]	0.60V ≤ Source ≤ 3.70V (in 12.5mV step)
		UV Detection	12h[7:0]	0.60V ≤ Source ≤ 3.70V (in 12.5mV step)
	REG3DET	OV Detection	15h[7:0]	2.00V ≤ Source ≤ 4.00V (in 12.5mV step)
		UV Detection	14h[7:0]	2.00V ≤ Source ≤ 4.00V (in 12.5mV step)

Figure 32 Trimming Program

Refer to *"Code List"* for details.

(1) Program changeable register

REGISTERS

Registers Map

Address	Block	Name	Read /Write	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value
00h	System	LSIVER	R	LSIVER[7:0]								8'h02
01h		STATE_	R	-	-	-	-	-	STATE[2:0]			8'h00
02h		BISTCTRL	R/W	-	-	-	-	-	BIST_MENU[1:0]		BISTEN	8'h00
03h		BISTRESULT_L	R	BIST_RESULT[7:0]								-
04h		BISTRESULT_H	R	BIST_RESULT[15:8]								-
05h		SYSCTRL	R/W	ATREHIS[1:0]		ATRENUM[1:0]		-	-	-	SWREP	Trimming
06h		AUTOOFF	R/W	-	-	-	-	-	DISAUTOOFF[3:0]			8'h00
07h	-	-	-	-	-	-	-	-	-	-	-	-
08h	Sequence	REG1SEQ	R	-	-	REG1ONT[1:0]		-	-	REG1OFFT[1:0]		Trimming
09h		REG2SEQ	R	-	-	REG2ONT[1:0]		-	-	REG2OFFT[1:0]		Trimming
0Ah		REG3SEQ	R	-	-	REG3ONT[1:0]		-	-	REG3OFFT[1:0]		Trimming
0Bh		RESETSEQ	R	-	RESETONT[2:0]			-	-	-	-	Trimming
0Ch		SLOTDTIM	R	-	-	-	-	-	-	SLOTDLYTIM[1:0]		Trimming
0Dh	Power-Source	REGCNT	R/W	-	-	-	-	-	REGDISOFF[2:0]			8'h00
0Eh		EXDETCNT	R/W	-	-	-	-	-	-	-	EXDETEN	8'h00
0Fh	-	-	-	-	-	-	-	-	-	-	-	-
10h	DETCNT	DET1DAC_UV	R/W	DET1UVDAC[7:0]								Trimming
11h		DET1DAC_OV	R/W	DET1OVDAC[7:0]								Trimming
12h		DET2DAC_UV	R/W	DET2UVDAC[7:0]								Trimming
13h		DET2DAC_OV	R/W	DET2OVDAC[7:0]								Trimming
14h		DET3DAC_UV	R/W	DET3UVDAC[7:0]								Trimming
15h		DET3DAC_OV	R/W	DET3OVDAC[7:0]								Trimming
16h		EXDETDAC_UV	R/W	EXDETUVDAC[7:0]								8'h00
17h		EXDETDAC_OV	R/W	EXDETOVDAC[7:0]								8'h00
18h	-	-	-	-	-	-	-	-	-	-	-	-
19h	-	-	-	-	-	-	-	-	-	-	-	-
1Ah	-	-	-	-	-	-	-	-	-	-	-	-
1Bh	-	-	-	-	-	-	-	-	-	-	-	-
1Ch	-	-	-	-	-	-	-	-	-	-	-	-
1Dh	-	-	-	-	-	-	-	-	-	-	-	-
1Eh	-	-	-	-	-	-	-	-	-	-	-	-
1Fh	-	-	-	-	-	-	-	-	-	-	-	-
20h	Interrupt	INTREQ_L	R/W	INTREQ[7:0]								Undef
21h		INTREQ_M	R/W	INTREQ[15:8]								Undef
22h		INTREQ_H	R/W	INTREQ[16:24]								Undef
23h		VOLMON	R	VOLMON[7:0]								Undef
24h		SYSMON	R	-	-	-	-	-	-	CLKFREQ	TEMPERATURE	Undef
25h		INTMSK_L	R/W	INTREQ[7:0]								8'h00
26h		INTMSK_M	R/W	INTREQ[15:8]								Trimming
27h		INTMSK_H	R/W	INTREQ[16:24]								8'h80
28h		SHREQMSK_L	R/W	SHREQMSK[7:0]								8'h00
29h		SHREQMSK_H	R/W	SHREQMSK[15:8]								8'h07
2Ah	-	-	-	-	-	-	-	-	-	-	-	-
2Bh	-	-	-	-	-	-	-	-	-	-	-	-
2Ch	-	-	-	-	-	-	-	-	-	-	-	-
2Dh	-	-	-	-	-	-	-	-	-	-	-	-
2Eh	-	-	-	-	-	-	-	-	-	-	-	-
2Fh	-	-	-	-	-	-	-	-	-	-	-	-
30-FFh	-	-	-	-	-	-	-	-	-	-	-	-

Registers Map (1)(2)

(1) The bit of "-" returns "0" when read, but it cannot be set even if "1" is written.
(2) The default value of bits with green hatch are set by trimming.

System

STATE: Current State Monitor Register **[Address 01h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	STATE[2:0]		
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bits [2:0]: STATE

These bits indicate the current state.

STATE	Current State
000	Reset / Ready
001	PS Start Sequence
010	Power Supply
011	PS Stop Sequence
100	Safety
Others	Reserved

BISTCTRL: BIST Control Register **[Address 02h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	BIST_MENU		BISTEN
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits [2:1]: BIST MENU

BIST_MENU	Test Menu
00	Logic & Analog BIST
01	Analog BIST only
10	Logic BIST only
11	prohibit

Bit 0: BISTEN

Enable/Disable the BIST check function.

0: Disable

1: Enable (In the READY state, start BIST).

This bit is automatically cleared when BIST is completed.

BISTRESULT_L/H: BIST Result Register **[Address 03h – 04h]**

Address 04h								
Bit	7	6	5	4	3	2	1	0
Symbol	BIST_RESULT[15:8]							
R/W	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-
Address 03h								
Bit	7	6	5	4	3	2	1	0
Symbol	BIST_RESULT[7:0]							
R/W	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-

This register indicates result of BIST.

0: Normal done

1: An error was detected

BIST_RESULT[15:0]	Test Block
Bit 15	Reserved
Bit 14	Reserved
Bit 13	Abnormal RESETO Pin Release
Bit 12	Trimming Cell Fault
Bit 11	LOGIC BIST
Bit 10	EXTDET
Bit 9	REG3DET
Bit 8	REG2DET
Bit 7	REG1DET
Bit 6	REG3(LDO)
Bit 5	REG2(DCDC)
Bit 4	REG1(DCDC)
Bit 3	IODET
Bit 2	VINCMP
Bit 1	UVLO_D
Bit 0	UVLO_A

SYSCTRL: System Control Register **[Address 05h]**

Bit	7	6	5	4	3	2	1	0
Symbol	ATREHIS[1:0]		ATRENUM[1:0]		-	-	-	SWREP
R/W	R	R	R	R	R	R	R	W
Default	0	0	By trim	By trim	0	0	0	-

Bits [7:6]: ATREHIS

Indicates the history number of times auto restoration execution.

The history number of times is clear by normal power-off (by the PWRON pin) or reading this register.

Bits [5:4]: ATRENUM

Sets the maximum number of times auto restoration. The number of times is set by trimming. Every time an error is detected, it will automatically restoration to the maximum number of times.

ARNUM[1:0]	Auto-restoration Times
00	0
01	1
10	2
11	3

Bit 0: SWREP

Starts Repower-on Sequence. If “1” is written into this bit in Power Supply state, the state transitions to PS Stop Sequence state and returns to the Power Supply state via the PS Start Sequence state. Refer to the chapter of “Repower-on Sequence”.

AUTOOFF: REGn Auto Off Setting Register **[Address 06h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	DISAUTOOFF[2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register is set to auto power-supply-off even at under/over-voltage detection.

Setting REGn behavior when REGDETn detects REGn's under/over-voltage (n:1 to 3).

0: Enable: REG forced off.

1: Disable: REG keeps power supply.

DISAUTOOFF [2:0]	behavior
Bit 2	Setting REG3 behavior
Bit 1	Setting REG2 behavior
Bit 0	Setting REG1 behavior

Sequence

REG1SEQ: PS Start / Stop Sequence Timing Setting Register **[Address 08h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	REG1ONT		-	-	REG1OFFT	
R/W	R	R	R	R	R	R	R	R
Default	0	0	By Trim	By Trim	0	0	By Trim	By Trim

Bits [5:4]: REG1ONT, Bits [1:0]: REG1OFFT

These bits indicate On/Off timing of REG1 set by trimming.

REG1ONT	On Timing
00	Always-on
01	Slot 1
10	Slot 2
11	Slot 3

REG1OFFT	Off Timing
00	Slot 0
01	Slot 1
10	Slot 2
11	Slot 3

REG2SEQ: PS Start / Stop sequence Timing Setting Register **[Address 09h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	REG2ONT		-	-	REG2OFFT	
R/W	R	R	R	R	R	R	R	R
Default	0	0	By Trim	By Trim	0	0	By Trim	By Trim

Bits [5:4]: REG2ONT, Bits [1:0]: REG2OFFT

These bits indicate On/Off timing of REG2 set by trimming.

REG2ONT	On Timing
00	Reserved
01	Slot 1
10	Slot 2
11	Slot 3

REG2OFFT	Off Timing
00	Slot 0
01	Slot 1
10	Slot 2
11	Slot 3

REG3SEQ: PS Start / Stop sequence Timing Setting Register *[Address 0Ah]*

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	REG3ONT		-	-	REG3OFFT	
R/W	R	R	R	R	R	R	R	R
Default	0	0	By Trim	By Trim	0	0	By Trim	By Trim

Bits [5:4]: REG3ONT, Bits [1:0]: REG3OFFT

These bits indicate On/Off timing of REG3 set by trimming.

REG3ONT	On Timing
00	Reserved
01	Slot 1
10	Slot 2
11	Slot 3

REG3OFFT	Off Timing
00	Slot 0
01	Slot 1
10	Slot 2
11	Slot 3

RESETSEQ: Reset Start Sequence Timing Setting Register **[Address 0Bh]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	RESETONT			-	-	-	-
R/W	R	R	R	R	R	R	R	R
Default	0	By Trim	By Trim	By Trim	0	0	0	0

For further details, refer to the chapter of *"PS Start Sequence"* and *"PS Stop Sequence"*.

Bits [6:4]: RESETONT

These bits indicate On-timing of RESETONT set by trimming.

RESETONT	On Timing
000	Reserved
001	Slot 1
010	Slot 2
011	Slot 3
100	Slot 4
101	Slot 5

SLOTDTIM: Power Supply Start/Stop Slot Delay Time Setting Register **[Address 0Ch]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-				SLOTDLYTIM [1:0]	
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	By Trim	By Trim

Bits [1:0]: SLOTDLYTIM

Power-supply stop sequence slot delay value.

SLOTDLYTIM	Slot Delay Time [ms]
00	1.8
01	3.6
10	7.2
11	14.4

Power Source

REGCNT: REG Control Register **[Address 0Dh]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	DISAUTOOFF[2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register set discharge function. Discharge function is valid when this bit is enabled and REGn is turned off.

0: Discharge function valid

1: Discharge function invalid

DISAUTOOFF [2:0]	Discharge function
Bit 2	REG3 discharge off bit.
Bit 1	REG2 discharge off bit.
Bit 0	REG1 discharge off bit.

Note: When discharge is invalid, overvoltage may be detected after off-sequence.

EXDETCNT: External DET Control Register **[Address 0Eh]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	EXDET EN
R/W	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	0

This register set external DET function.

Bit 0: EXDETEN

0: Disable

1: Enable

DETCNT

DET1DAC_UV/OV: REG1DET Under/Over-Voltage Detection Setting Register **[Address 10h-11h]**

Address 10h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET1UVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim
Address 11h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET1OVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim

This register is used to set the threshold voltage of the under-voltage detector for REG1. Initial value is set by trimming. The LSB is 12.5 mV.

The valid threshold voltage range.

DET1UV(OV) DAC	V_{UVDET}, V_{OVDET} [V]
00h	0.6
01h	0.6125
⋮	⋮
F7h	3.6875
F8h	3.7
F9h	Prohibit (3.7 V)
⋮	⋮
FFh	Prohibit (3.7 V)

DET2DAC_UV/OV: REG2DET Under/Over-Voltage Detection Setting Register **[Address 12h-13h]**

Address 12h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET2UVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim
Address 13h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET2OVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim

This register is used to set the threshold voltage of the under-voltage detector for REG2.
Initial value is set by trimming. The LSB is 12.5 mV.

The valid threshold voltage range.

DET2UV(OV)DAC	V_{UVDET}, V_{OVDET} [V]
00h	0.6
01h	0.6125
⋮	⋮
F7h	3.6875
F8h	3.7
F9h	Prohibit (3.7 V)
⋮	⋮
FFh	Prohibit (3.7 V)

DET3DAC_UV/OV: REG3DET Under/Over-Voltage Detection Setting Register **[Address 14h-15h]**

Address 14h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET3UVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim
Address 15h								
Bit	7	6	5	4	3	2	1	0
Symbol	DET3OVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	By trim	By trim	By trim	By trim	By trim	By trim	By trim	By trim

This register is used to set the threshold voltage of the under-voltage detector for REG3. Initial value is set by trimming. The LSB is 12.5 mV.

The valid threshold voltage range.

DET3UV (OV) DAC	V_{UVDET}, V_{OVDET} [V]
00h	2.0
01h	2.0125
⋮	⋮
FDh	3.9875
A0h	4.00
A1h	Prohibit (4.0 V)
⋮	⋮
FFh	Prohibit (4.0 V)

EXDETDAC_UV/OV: EXTDET Under/Over-Voltage Detection Setting Register **[Address 16h-17h]**

Address 16h								
Bit	7	6	5	4	3	2	1	0
Symbol	EXDETUVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Address 17h								
Bit	7	6	5	4	3	2	1	0
Symbol	EXDETOVDAC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register is used to set the threshold voltage of the under-voltage detector for EXDET1 pin. Initial value is set by trimming. The LSB is 12.5 mV.

The valid threshold voltage range.

EXDETUV (OV) DAC	V_{UVDET}, V_{OVDET} [V]
00h	0.6
01h	0.6125
⋮	⋮
F7h	3.6875
F8h	3.7
F9h	Prohibit (3.7 V)
⋮	⋮
FFh	Prohibit (3.7 V)

Interrupt Control

INTREQ_H/M/L: Interrupt Request Register **[Address 22-20h]**

Address 22h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTREQ[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-
Address 21h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTREQ[15:8]							
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Default	-	-	0	-	-	-	-	-
Address 20h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTREQ[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	-	-	-	-

These registers indicate the interrupt request.

0: Not detected (Cleared)

1: A request was detected

These registers are set by this device and cleared by host.
Each bit is cleared by writing "1" and is disregarded by writing “0”.

INTREQ[23:0]	IRQ Name	Interrupt Request Factor
Bit 23	BISTERR	BIST Error detected Read the BISTRESULT_L/H register.
Bit 22	CLKERR	Clock Gen has error occurred. Read the CLKFREQ bit of SYSMON register.
Bit 21	REG3STIM	REG3 soft-start has a short rise time.
Bit 20	REG2STIM	REG2 soft-start has a short rise time.
Bit 19	REG1STIM	REG1 soft-start has a short rise time.
Bit 18	REG3TIMO	REG3 voltage didn't reach the target voltage within slot delay time.
Bit 17	REG2TIMO	REG2 voltage didn't reach the target voltage within slot delay time.
Bit 16	REG1TIMO	REG1 voltage didn't reach the target voltage within slot delay time.
Bit 15	BISTDONE	BIST is done.
Bit 14	I2CERR	I2C detected CRC-error.
Bit 13	-	-
Bit 12	REG2ROC	REG2 detected reverse current.
Bit 11	REG1ROC	REG1 detected reverse current.
Bit 10	REG2OC	REG2 detected overcurrent.
Bit 9	REG1OC	REG1 detected overcurrent.
Bit 8	EXUV	EXDET1 input is under-voltage.
Bit 7	EXOV	EXDET1 input is over-voltage.
Bit 6	REG3UV	REG3 output is under-voltage.
Bit 5	REG3OV	REG3 output is over-voltage.
Bit 4	REG2UV	REG2 output is under-voltage.
Bit 3	REG2OV	REG2 output is over-voltage.
Bit 2	REG1UV	REG1 output is under-voltage.
Bit 1	REG1OV	REG1 output is over-voltage.
Bit 0	OVTEMP	Die is over-temperature or recovered normal temperature. Read the TEMPERATURE bit of SYSMON register.

VOLMON: Voltage Status Monitor Register **[Address 23h]**

Bit	7	6	5	4	3	2	1	0
Symbol	VOLMON[7:0]							
R/W	R	R	R	R	R	R	R	R
Default	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

This register indicates the state of the voltage.
0: Normal voltage
1: Detect the over or under voltage

VOLMON[7:0]	Mon Name	Voltage State
Bit 7	EXOVM	Detect the over-voltage at external pin.
Bit 6	EXUVM	Detect the under-voltage at external pin.
Bit 5	REG3OVM	Detect the over-voltage of REG3
Bit 4	REG3UVM	Detect the under-voltage of REG3
Bit 3	REG2OVM	Detect the over-voltage of REG2
Bit 2	REG2UVM	Detect the under-voltage of REG2
Bit 1	REG1OVM	Detect the over-voltage of REG1
Bit 0	REG1UVM	Detect the under-voltage of REG1

SYSMON: System Status Monitor Register **[Address 24h]**

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	CLKFREQ	TEMPERATURE
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	Undefined	Undefined

Bit 1: CLKFREQ

This bit indicates the state of the Oscillator Frequency.

0: Normal

1: Abnormal frequency

Bit 0: TEMPERATURE

This bit indicates the state of the temperature.

0: Normal temperature

1: Over temperature

INTMSK_H/M/L: Interrupt Request Mask Register **[Address 27h-25h]**

Address 27h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTMSK[24:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	0	0	0	0
Address 26h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTMSK[15:8]							
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Default	By Trim	0	0	0	0	0	0	0
Address 25h								
Bit	7	6	5	4	3	2	1	0
Symbol	INTMSK[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register masks low-drive of INTB pin by interrupt request when the corresponding bit is set to zero.
0: Interrupt masked
1: Interrupt unmasked

INTMSK[23:0]	IRQ Mask Name	Mask Interrupt Request
Bit 23	BISTERR UMSK	BIST Error detected
Bit 22	CLKERR UMSK	Clock Gen has error occurred.
Bit 21	REG3STIM UMSK	REG3 soft-start has a short rise time.
Bit 20	REG2STIM UMSK	REG2 soft-start has a short rise time.
Bit 19	REG1STIM UMSK	REG1 soft-start has a short rise time.
Bit 18	REG3TIMO UMSK	REG3 voltage didn't reach the target voltage within slot delay time.
Bit 17	REG2TIMO UMSK	REG2 voltage didn't reach the target voltage within slot delay time.
Bit 16	REG1TIMO UMSK	REG1 voltage didn't reach the target voltage within slot delay time.
Bit 15	BISTDONE UMSK	BIST is done.
Bit 14	I2CERR UMSK	I2C detected CRC-error.
Bit 13	-	-
Bit 12	REG2ROC UMSK	REG2 detected reverse current.
Bit 11	REG1ROC UMSK	REG1 detected reverse current.
Bit 10	REG2OC UMSK	REG2 detected overcurrent.
Bit 9	REG1OC UMSK	REG1 detected overcurrent.
Bit 8	EXUV UMSK	EXDET1 input is under-voltage.
Bit 7	EXOV UMSK	EXDET1 input is over-voltage.
Bit 6	REG3UV UMSK	REG3 output is under-voltage.
Bit 5	REG3OV UMSK	REG3 output is over-voltage.
Bit 4	REG2UV UMSK	REG2 output is under-voltage.
Bit 3	REG2OV UMSK	REG2 output is over-voltage.
Bit 2	REG1UV UMSK	REG1 output is under-voltage.
Bit 1	REG1OV UMSK	REG1 output is over-voltage.
Bit 0	OVTEMP UMSK	Die is over-temperature or recovered normal temperature.

SHREQMSK_H/L: Shut down request Mask Register **[Address 29-28h]**

Address 29h								
Bit	7	6	5	4	3	2	1	0
Symbol	SHREQMSK[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	1
Address 28h								
Bit	7	6	5	4	3	2	1	0
Symbol	SHREQMSK[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This register is valid when the SHUTREQ pin is set to shutdown request function. This register sets mask of SHUTREQ pin assert in Safety State.

1: Unmasked

0: Masked

SHREQMSK [15:0]	Shut down Mask Name	Mask Shutdown Request
Bit 15	ROVC2SR UMSK	REG2 detected reverse current.
Bit 14	ROVC1SR UMSK	REG1 detected reverse current.
Bit 13	STIM3SR UMSK	REG3 soft-start has a short rise time.
Bit 12	STIM2SR UMSK	REG2 soft-start has a short rise time.
Bit 11	STIM1SR UMSK	REG1 soft-start has a short rise time.
Bit 10	OV3SR UMSK	REG3 output is over-voltage.
Bit 9	OV2SR UMSK	REG2 output is over-voltage.
Bit 8	OV1SR UMSK	REG1 output is over-voltage.
Bit 7	OVC2SR UMSK	REG2 detected overcurrent.
Bit 6	OVC1SR UMSK	REG1 detected overcurrent.
Bit 5	TIMOUT3SR UMSK	REG3 voltage didn’t reach the target voltage within slot delay time.
Bit 4	TIMOUT2SR UMSK	REG2 voltage didn’t reach the target voltage within slot delay time.
Bit 3	TIMOUT1SR UMSK	REG1 voltage didn’t reach the target voltage within slot delay time.
Bit 2	UV3SR UMSK	REG3 output is under-voltage.
Bit 1	UV2SR UMSK	REG2 output is under-voltage.
Bit 0	UV1SR UMSK	REG1 output is under-voltage.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit.
A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- REG1,2 Phase Compensation

Choose a low ESR ceramic capacitor. The input capacitor (CIN) between VINP and GNDP should be more than 10 µF, and the output capacitor (COUT) should be used by two or more parallel connection with ceramic capacitor of 22 µF. The phase compensation of this device is designed according to the COUT and L values. The inductance value of an inductor should be 2.2 μH to gain stability. Choose an inductor that has small DC resistance, has enough permissible current and is hard to cause magnetic saturation.

- REG1,2 PCB Layout

External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VINP pin and GNDP pin must be wiring the shortest. If the impedance of power supply lines and GND lines is high, the internal voltage of the IC may shift by the switching current, and the operating may be unstable. A sufficient consideration is required due to a large switching current flows through power supply lines, GND lines, an inductor, LX and VOUT lines. The wiring between VOUT pin and inductor should be separated from the wiring connected to the load.

- REG3 Phase Compensation

Phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, use a ceramic capacitor of 4.7 µF or more with ESR (Equivalent Series Resistance) of up to 300 mΩ to connect an output capacitor (C_{OUT}) between the VOUT3 and GNDL pins with shortest-distance wiring.

- Thermal Shutdown Function

The thermal shutdown function prevents the IC from fuming and ignition but does not ensure the IC's reliability or keep the IC below the absolute maximum ratings. The thermal shutdown function does not operate on the heat generated by other than the normal IC operation such as latch-up and overvoltage application. The thermal shutdown function operates in a state over the absolute maximum ratings, therefore, the thermal shutdown function should not be used for a system design.

- Nch Open Drain Pin Connection

When using the interrupt controller, the pull-up resistance of 10 kΩ to 100 kΩ for INTB pin is recommended. When not using it, the INTB pin must be left floating or connected to GND. When using the reset output function, the pull-up resistance of 10 kΩ to 100 kΩ for RESETO pin is recommended. The RESETO pin must be pulled up even when not in use.

TYPICAL CHARACTERISTICS

Typical characteristics are intended to be used as reference data, they are not guaranteed.

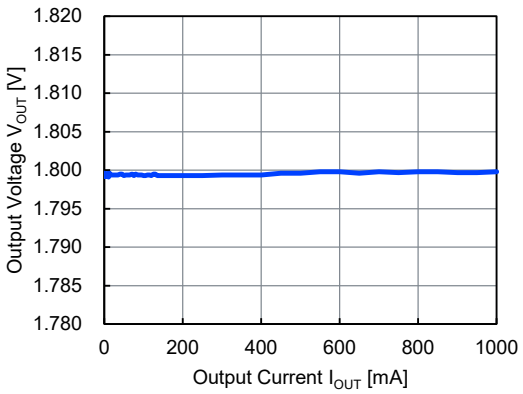
■DCDC Converters Typical Characteristics

1) Output Voltage vs Output Current

V_{IN} = 5.0 V, Ta = 25 °C

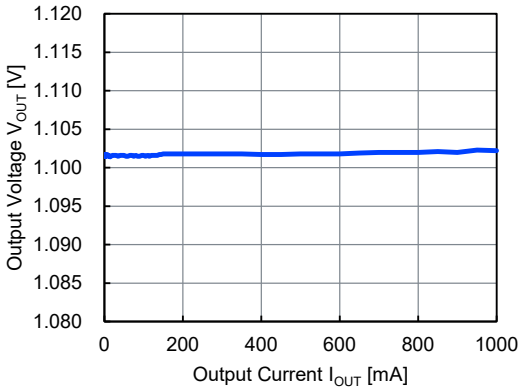
REG1

V_{SET} = 1.8 V

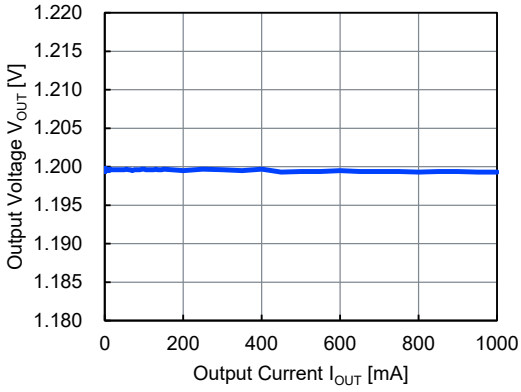


REG2

V_{SET} = 1.1 V



V_{SET} = 1.2 V

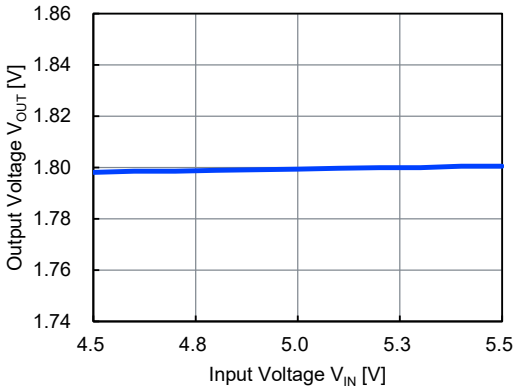


2) Output Voltage vs Input Voltage

Ta = 25 °C

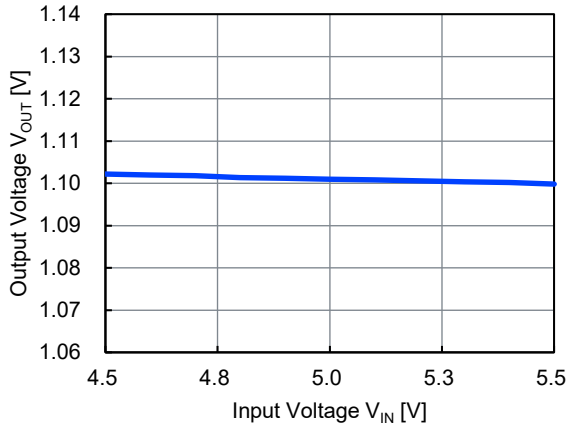
REG1

V_{SET} = 1.8 V

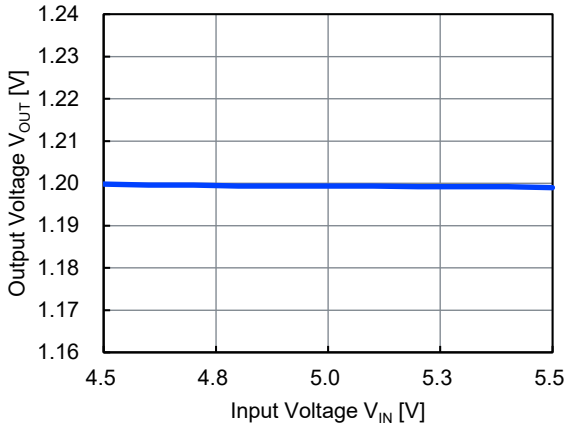


REG2

V_{SET} = 1.1 V



V_{SET} = 1.2 V

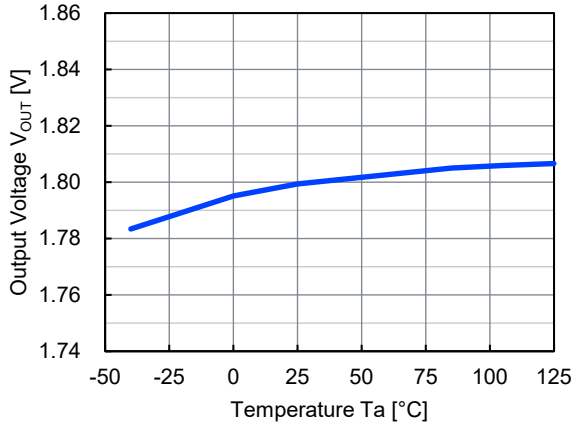


3) Output Voltage vs Temperature

V_{IN} = 5.0 V

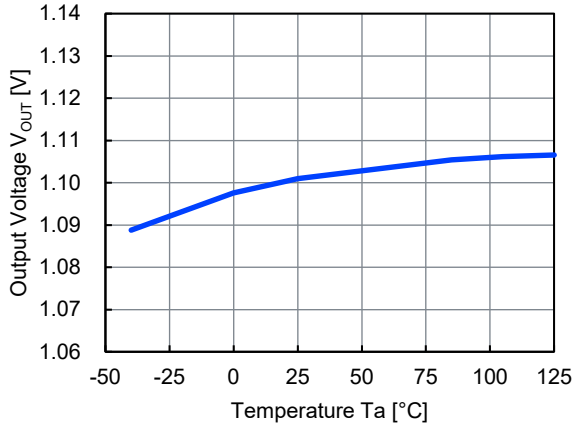
REG1

V_{SET} = 1.8 V

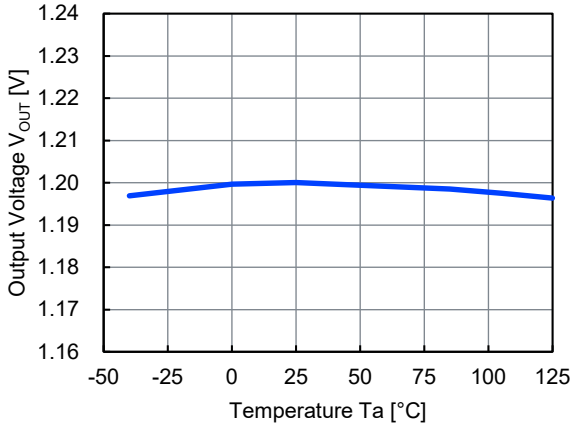


REG2

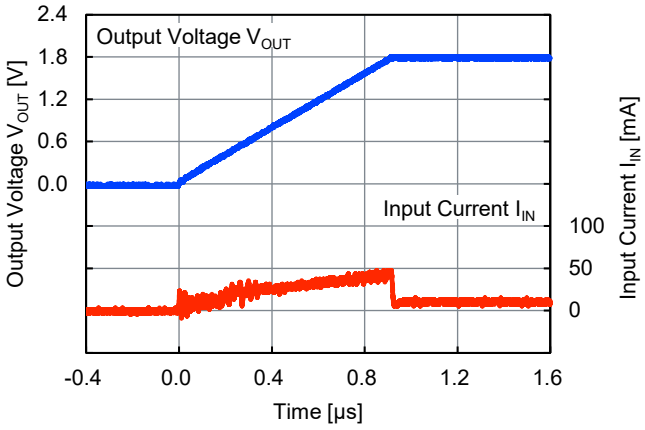
V_{SET} = 1.1 V



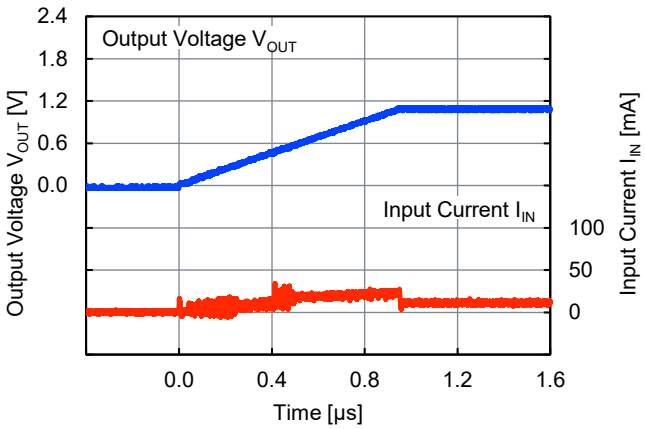
V_{SET} = 1.2 V



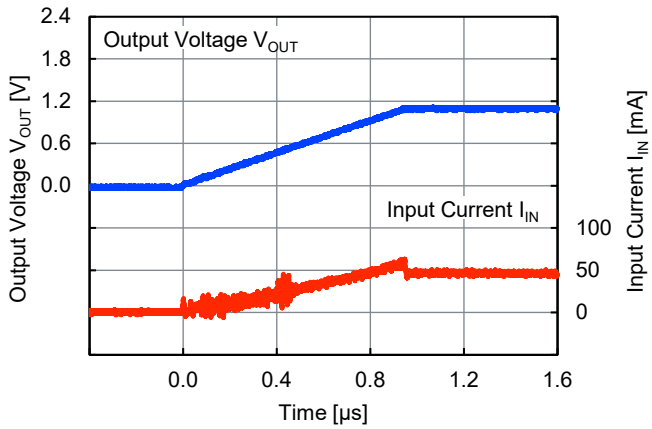
4) Soft Start Waveform
V_{IN} = 5.0 V, Ta = 25 °C
REG1
V_{SET} = 1.8 V, I_{OUT} = 0 mA



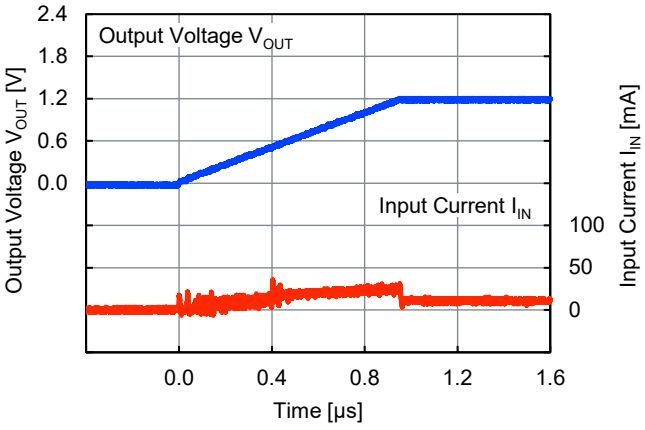
REG2
V_{SET} = 1.1 V, I_{OUT} = 0 mA



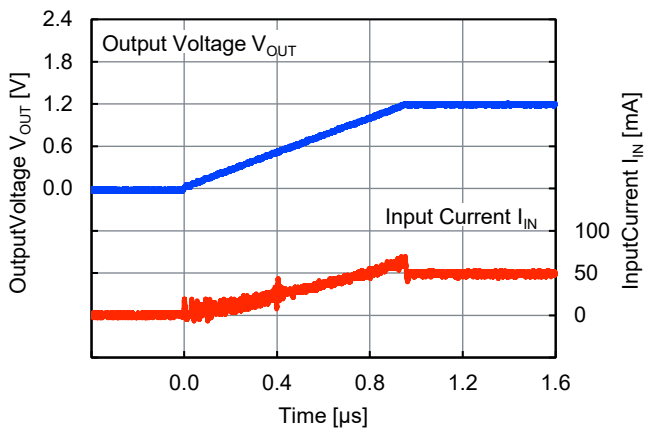
V_{SET} = 1.1 V, I_{OUT} = 150 mA



V_{SET} = 1.2 V, I_{OUT} = 0 mA



V_{SET} = 1.2 V, I_{OUT} = 150 mA

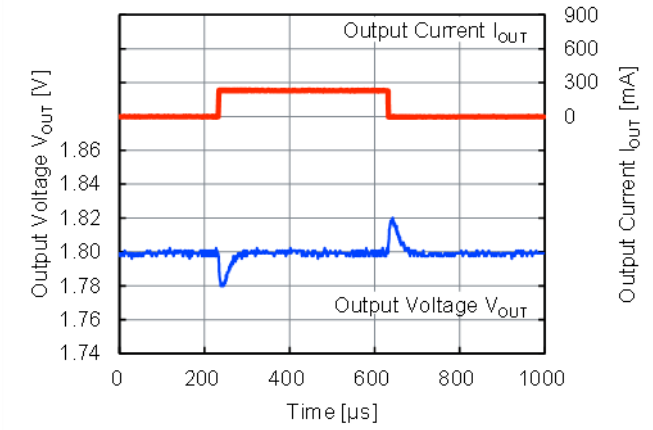


5) Load Transient Response

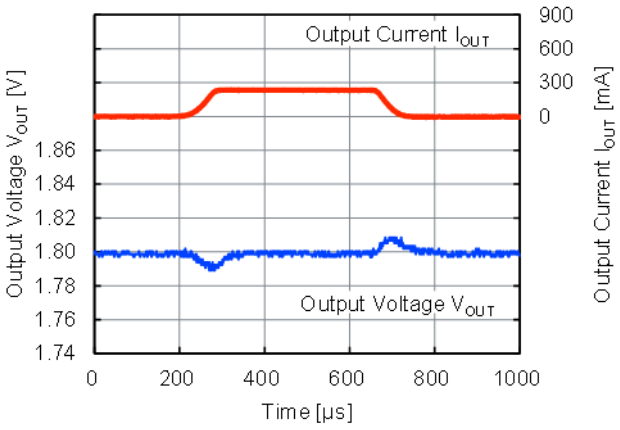
V_{IN} = 5.0 V, Ta = 25 °C

REG1, V_{SET} = 1.8 V, I_{OUT} = 1 mA ⇔ 230 mA

tr = tf = 1 µs

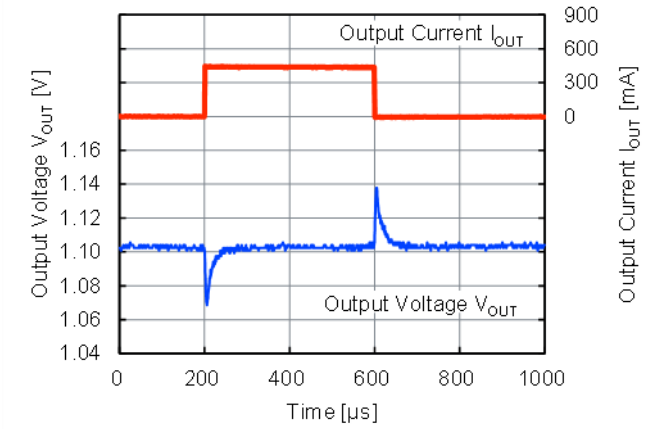


tr = tf = 50 µs

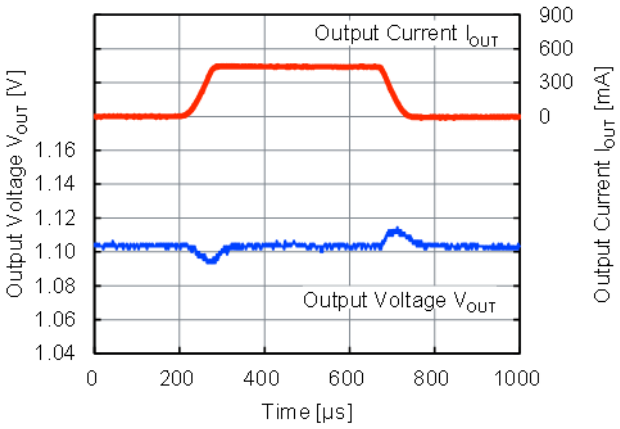


REG2, V_{SET} = 1.1 V, I_{OUT} = 1 mA ⇔ 440 mA

tr = tf = 1 µs

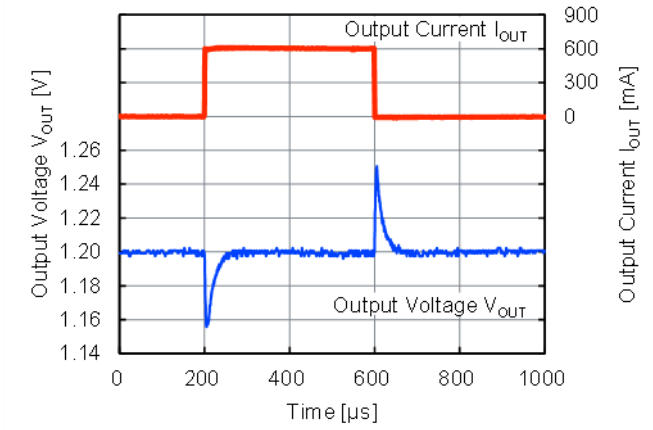


tr = tf = 50 µs

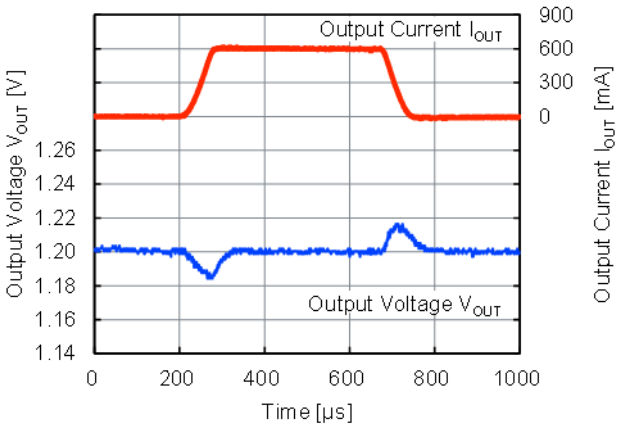


REG2, V_{SET} = 1.2 V, I_{OUT} = 1 mA ⇔ 600 mA

tr = tf = 1 µs

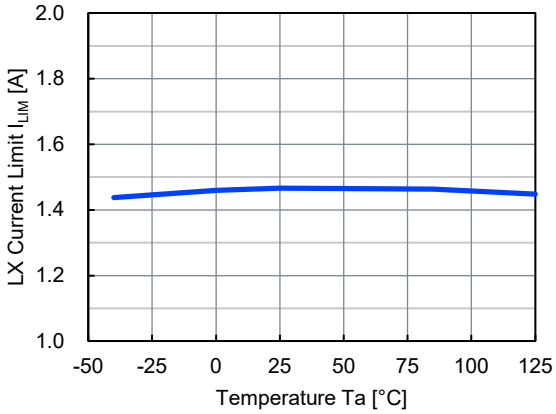


tr = tf = 50 µs

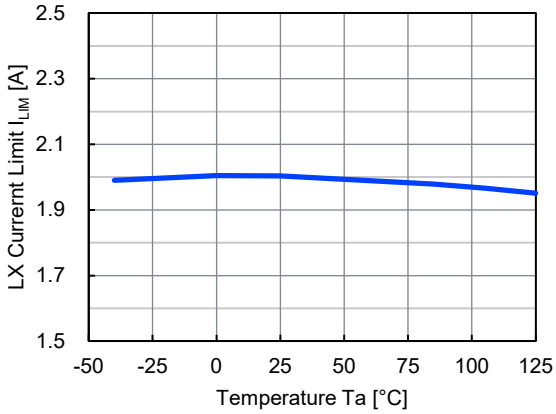


6) LX Limit Current vs Temperature
V_{IN} = 5.0 V

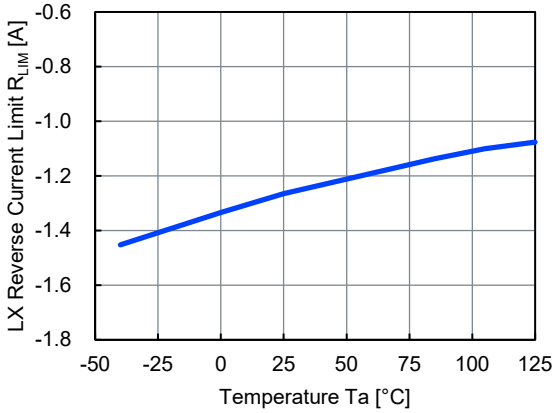
I_{OUT}MAX = 600 mA Ver



I_{OUT}MAX = 1000 mA Ver

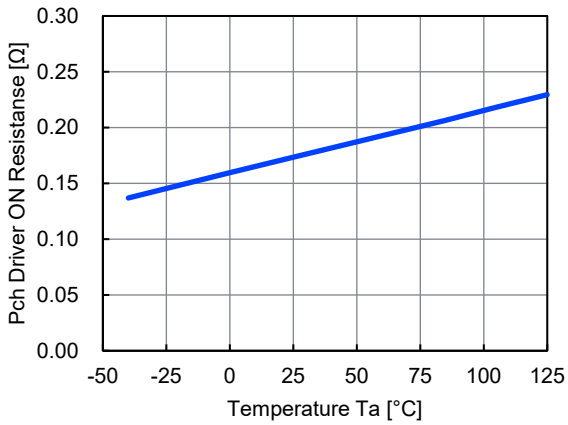


7) LX Reverse Limit Current vs Temperature
V_{IN} = 5.0 V

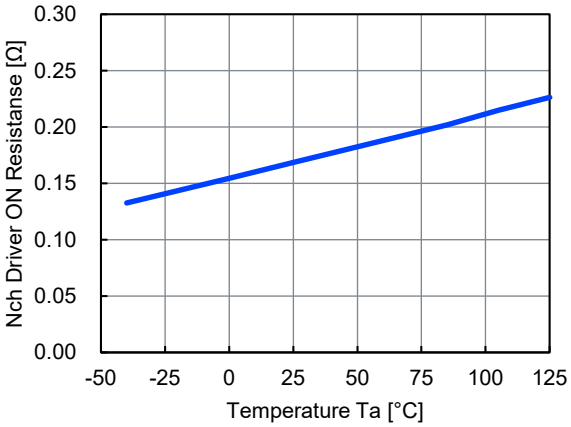


8) Driver On Resistance vs Temperature
V_{IN} = 5.0 V

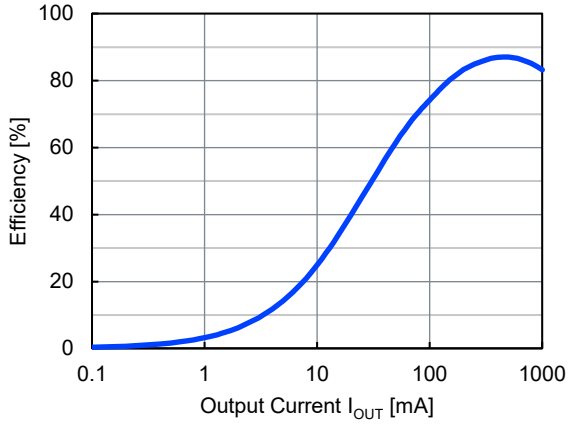
Pch Driver



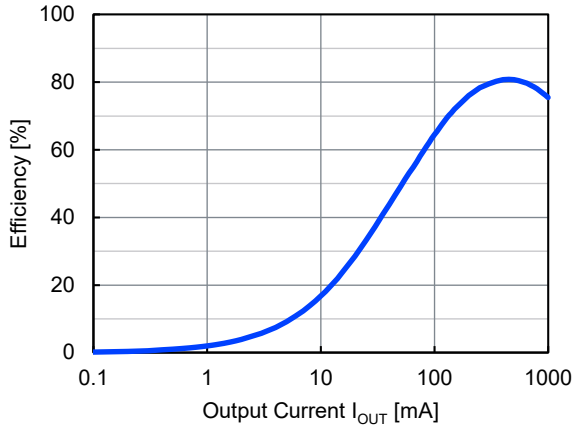
Nch Driver



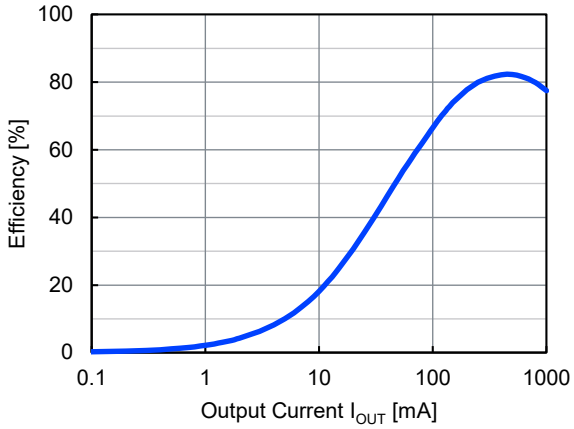
9) Efficiency
V_{IN} = 5.0 V, Ta = 25 °C
REG1
V_{SET} = 1.8 V



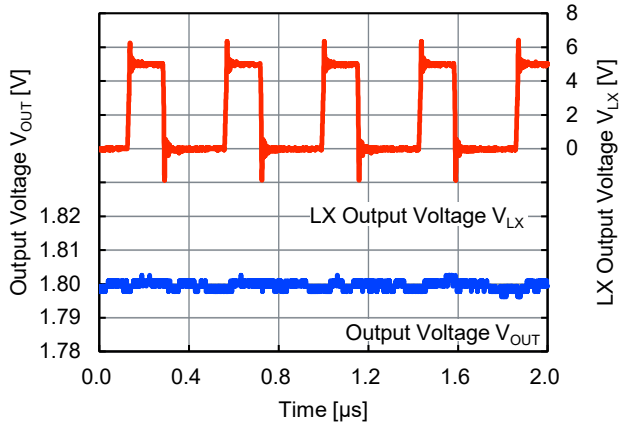
REG2
V_{SET} = 1.1 V



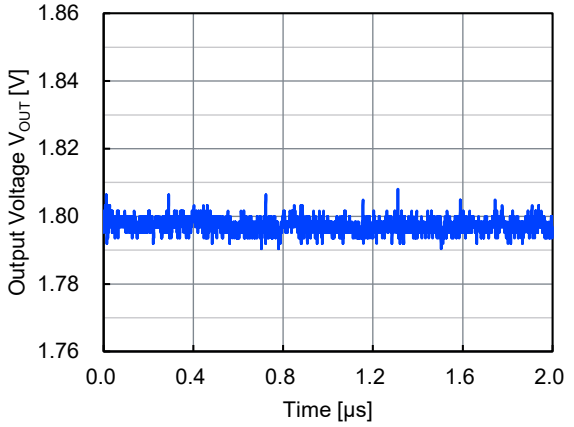
V_{SET} = 1.2 V



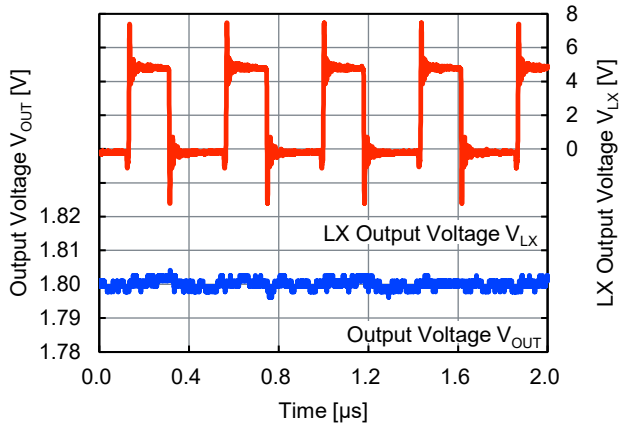
10) Output Voltage Waveform
REG1
V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.8 V, I_{OUT} = 0mA



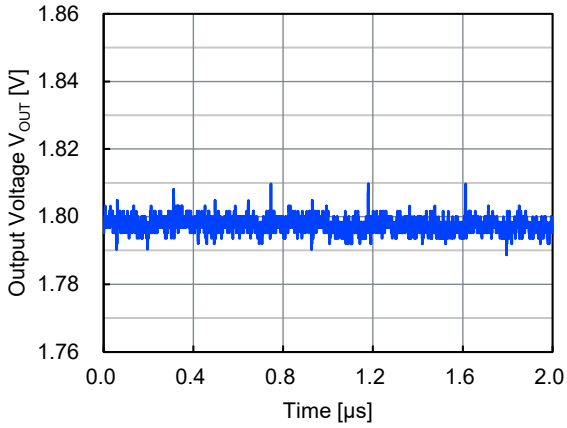
Without probe Filter



V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.8 V, I_{OUT} = 1000mA



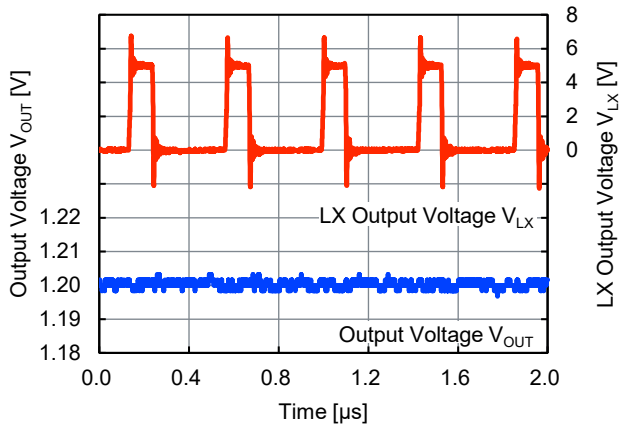
Without probe Filter

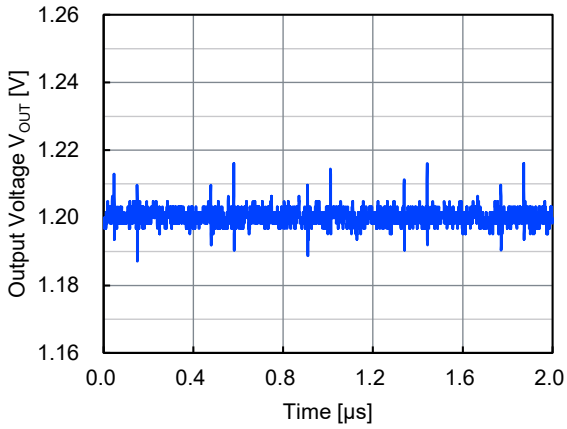


REG2

V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.2 V, I_{OUT} = 0mA

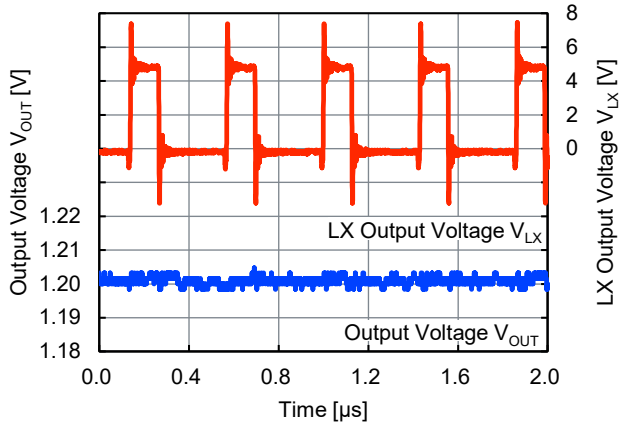
Without probe Filter

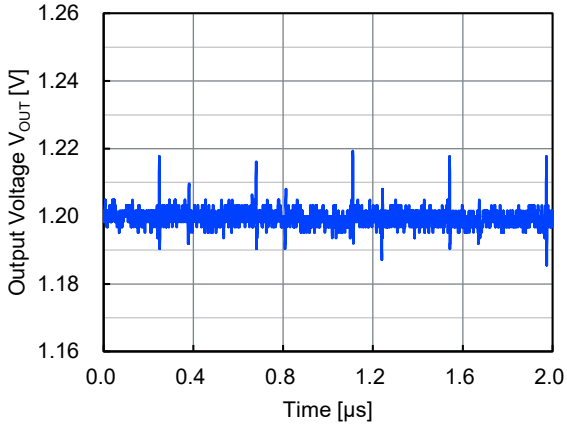




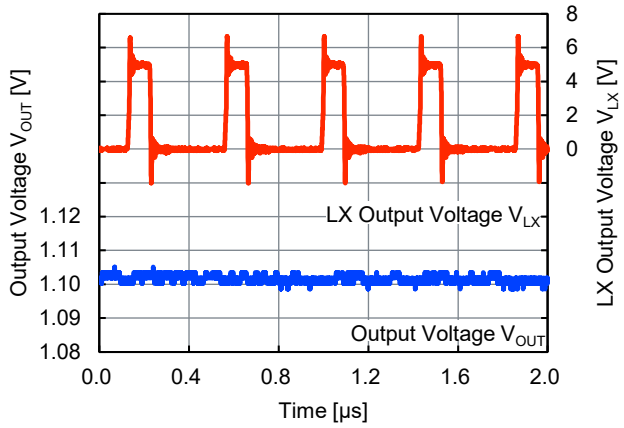
V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.2 V, I_{OUT} = 1000mA

Without probe Filter

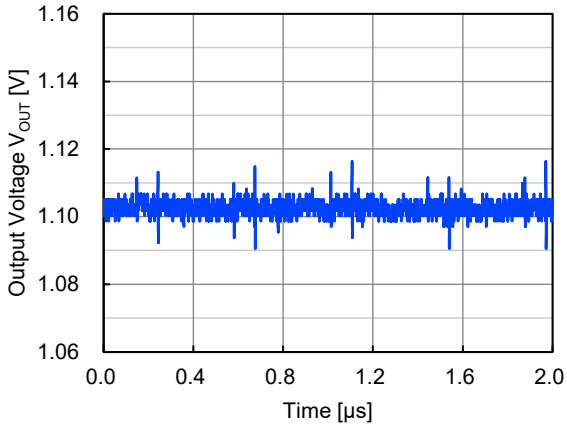




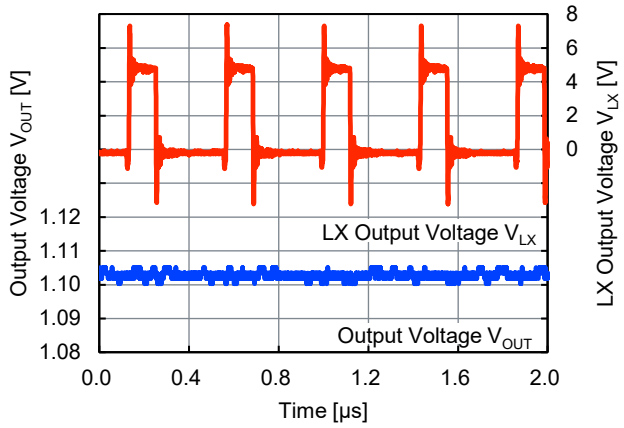
V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.1 V, I_{OUT} = 0mA



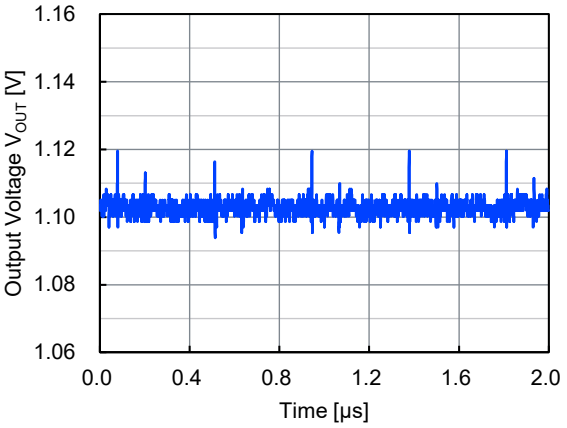
Without probe Filter



V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 1.1 V, I_{OUT} = 1000mA



Without probe Filter

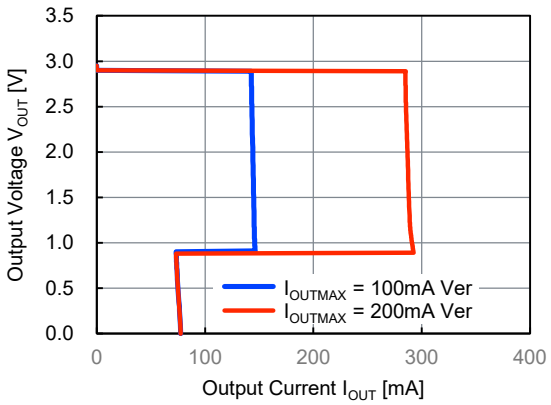


■LDO Typical Characteristics

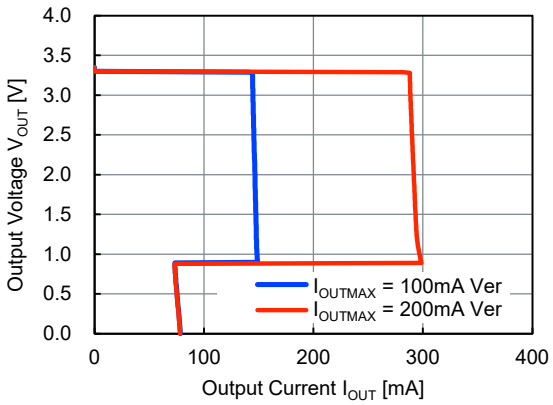
1) Output Voltage vs Output Current

V_{IN} = 5.0 V, Ta = 25 °C

V_{SET} = 2.9 V



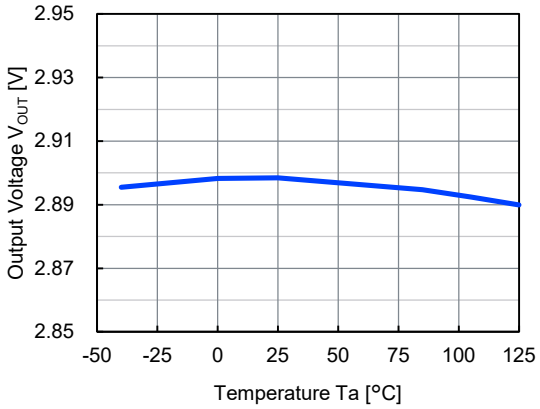
V_{SET} = 3.3 V



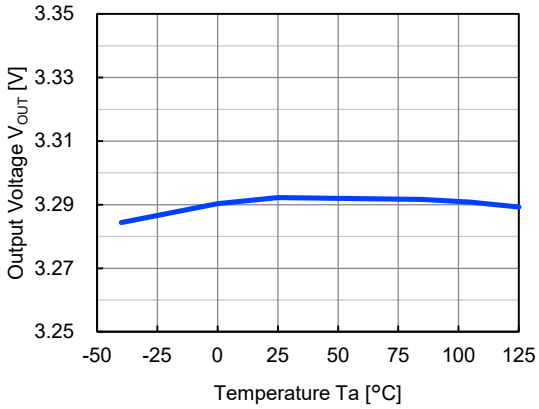
2) Output Voltage vs Temperature

V_{IN} = 5.0 V

V_{SET} = 2.9 V



V_{SET} = 3.3 V

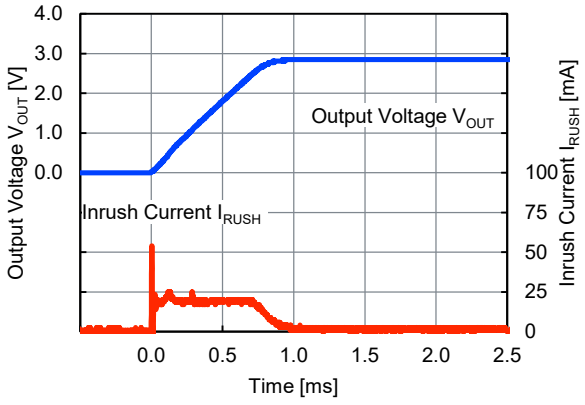


3) Soft Start Waveform

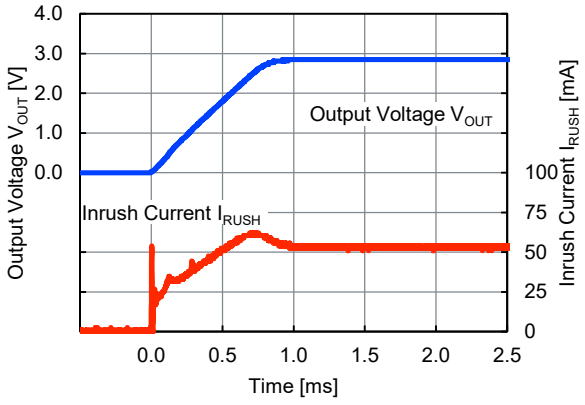
V_{IN} = 5.0 V, Ta = 25 °C

V_{SET} = 2.9 V

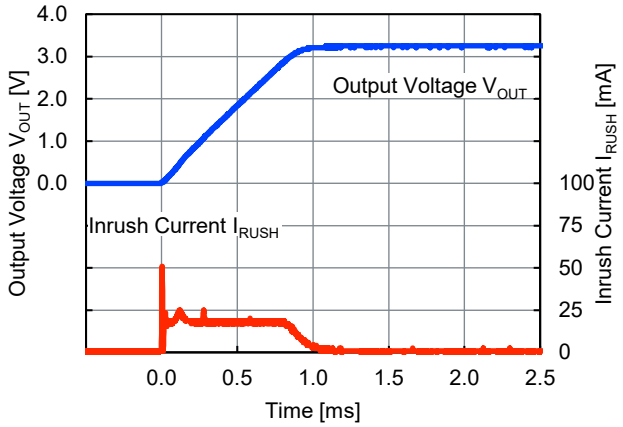
I_{OUT} = 0 mA



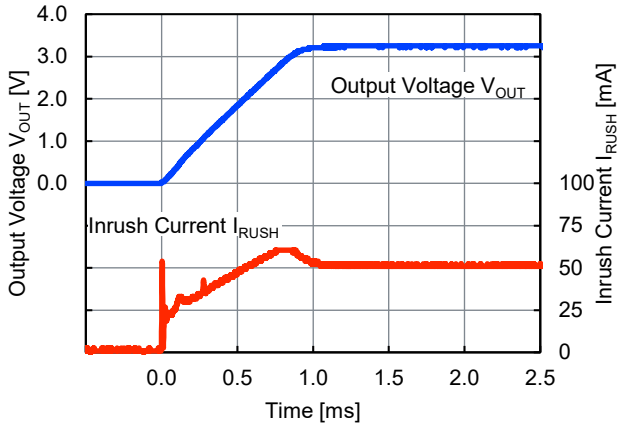
I_{OUT} = 50 mA



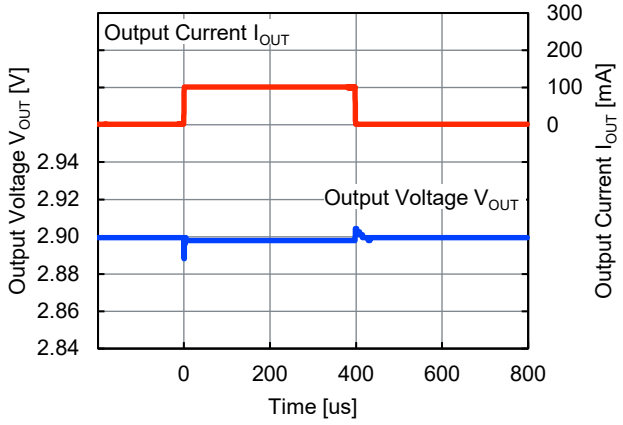
V_{SET} = 3.3 V
I_{OUT} = 0 mA



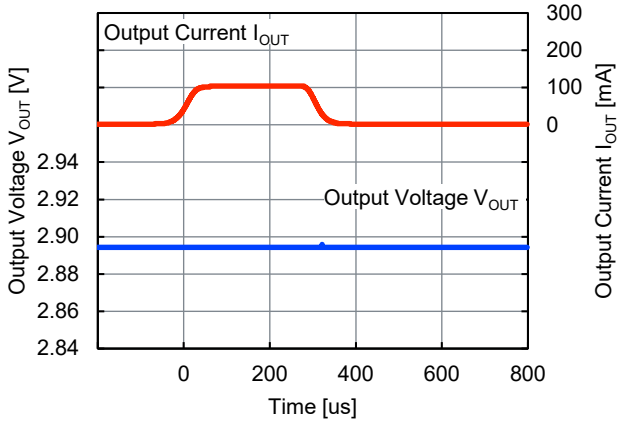
I_{OUT} = 50 mA



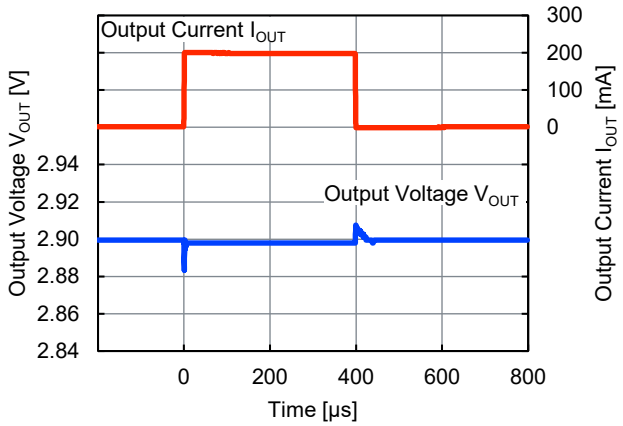
4) Load Transient Response
V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 2.9 V
I_{OUT} = 1 mA ⇔ 100 mA
tr = tf = 1 µs



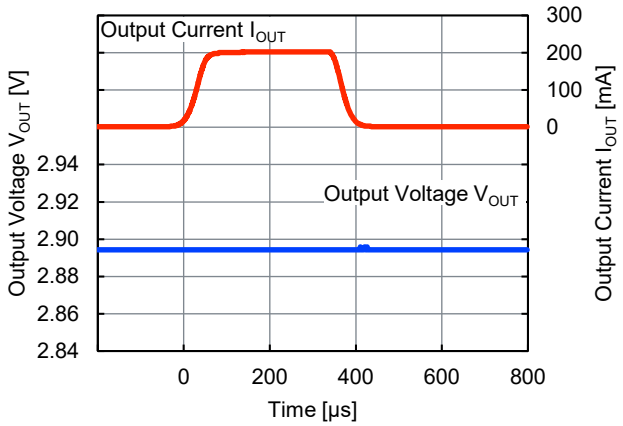
tr = tf = 50 µs



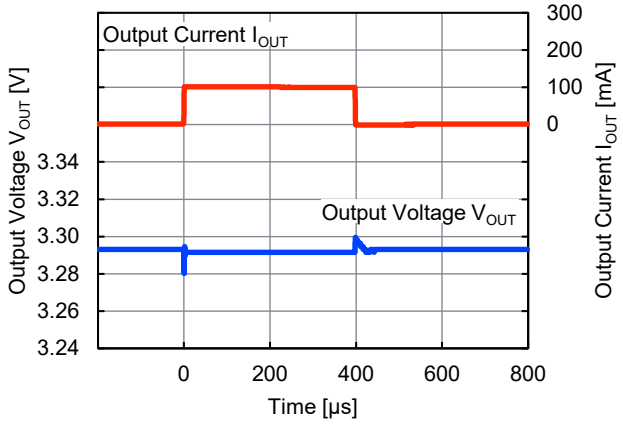
I_{OUT} = 1 mA ⇔ 200 mA
tr = tf = 1 µs



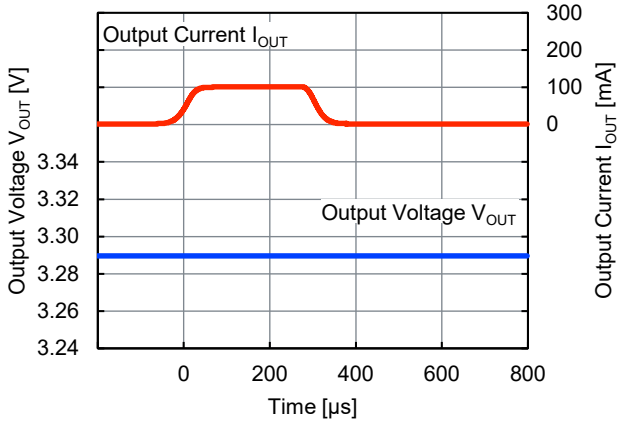
tr = tf = 50 µs



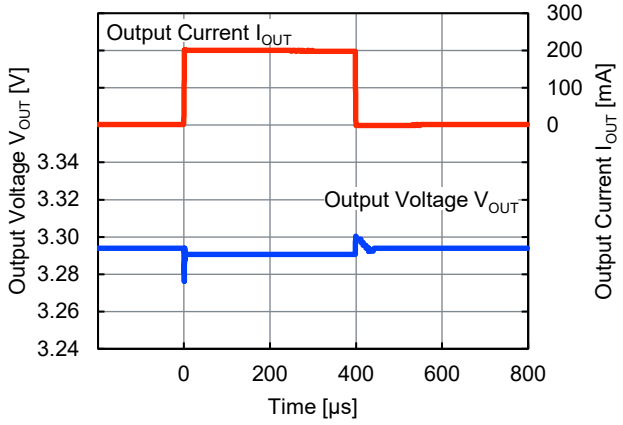
V_{IN} = 5.0 V, Ta = 25 °C, V_{SET} = 3.3 V
I_{OUT} = 1 mA ⇔ 100 mA
tr = tf = 1 µs



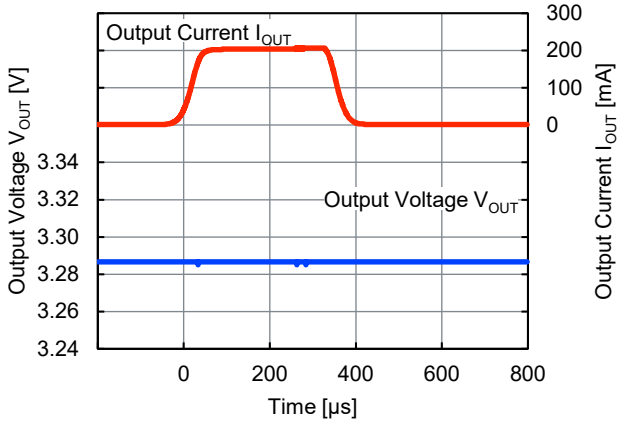
tr = tf = 50 µs



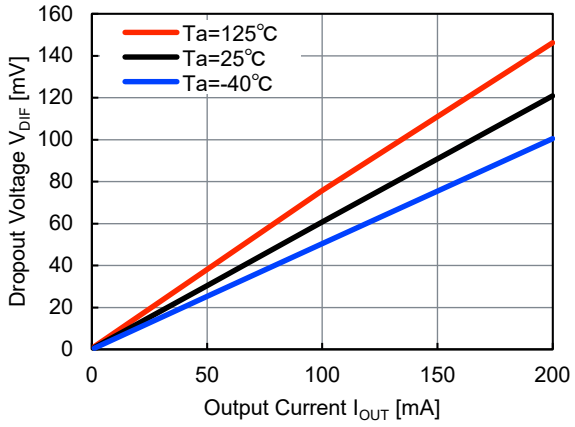
I_{OUT} = 1 mA ⇔ 200 mA
tr = tf = 1 µs



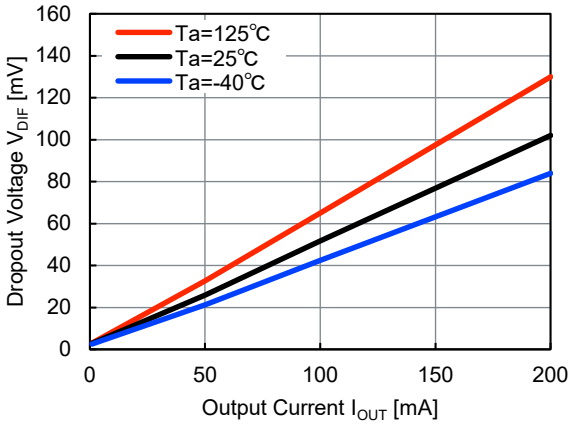
tr = tf = 50 µs



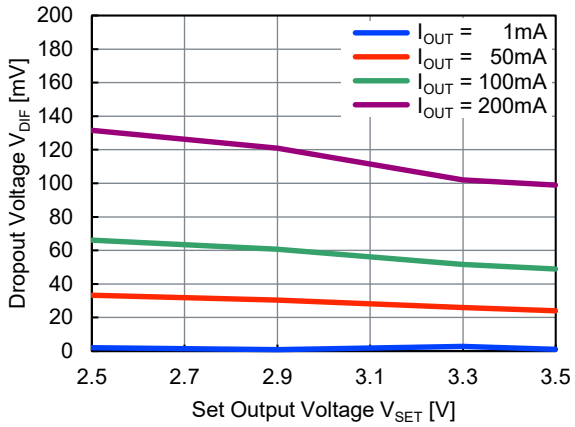
5) Dropout Voltage vs Output Current
V_{SET} = 2.9 V



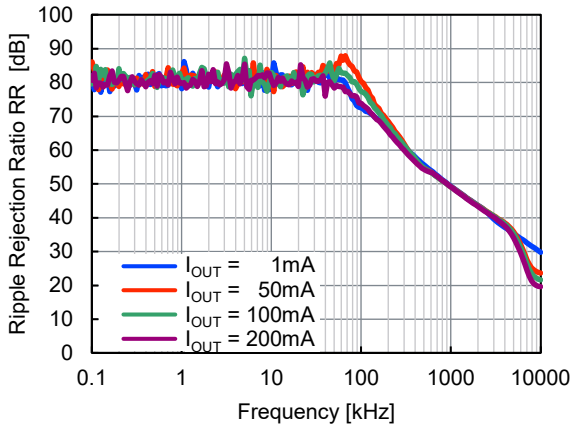
V_{SET} = 3.3 V



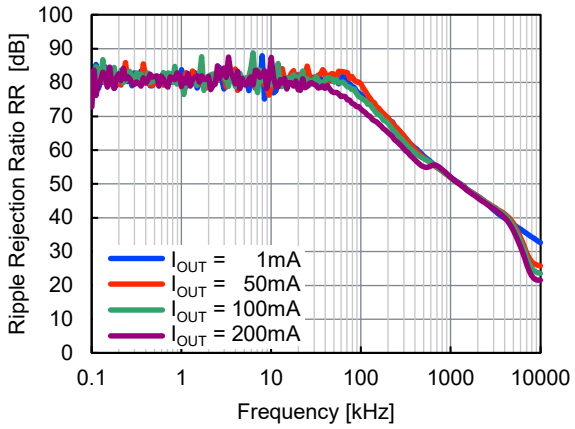
6) Dropout Voltage vs Set Output Voltage
Ta = 25 °C



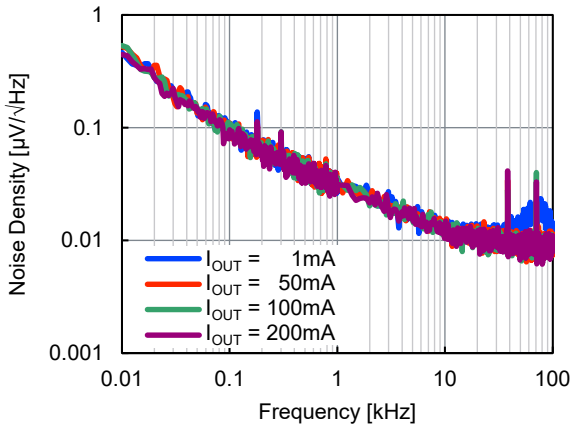
7) Ripple Rejection vs Frequency
V_{IN} = 5.0 V, Ta = 25 °C, VRIPPLE = 0.2 Vp-p
V_{SET} = 2.9 V



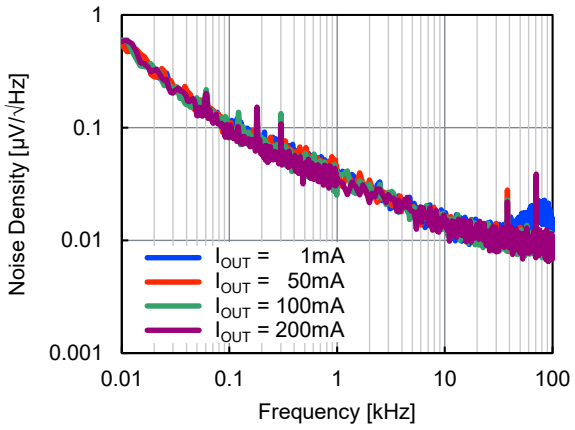
V_{SET} = 3.3 V



8) Output Noise Spectral Density vs Frequency
V_{IN} = 5.0 V, Ta = 25 °C
V_{SET} = 2.9 V



V_{SET} = 3.3 V



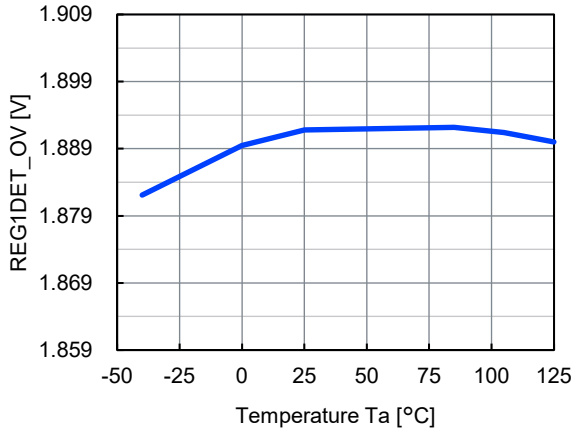
■Voltage Detector Typical Characteristics

1) Detect / Release Voltage vs Temperature

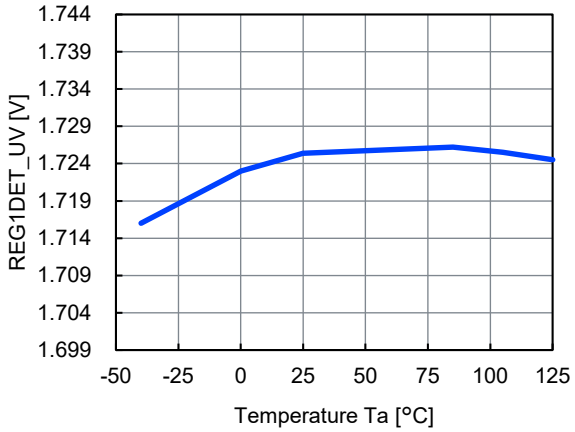
V_{IN} = 5.0 V

REG1DET

OV = 1.8875 V

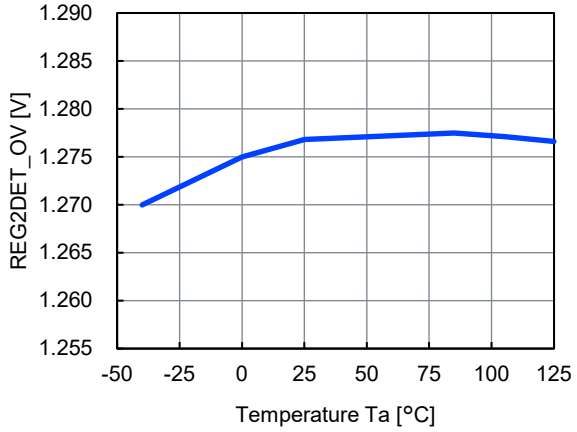


UV = 1.7250 V

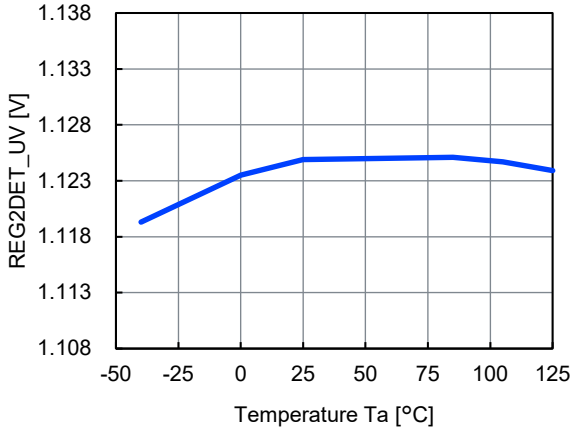


REG2DET

OV = 1.2750 V

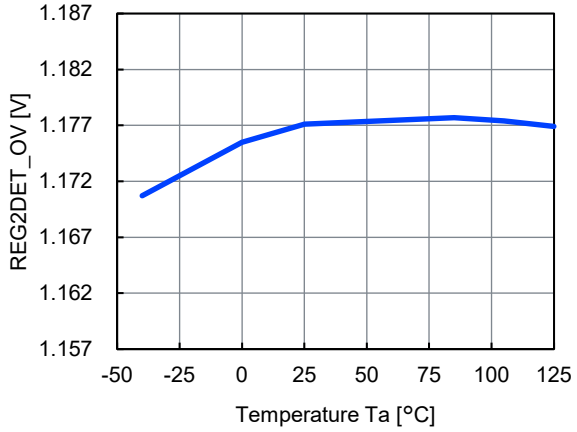


UV = 1.1250 V

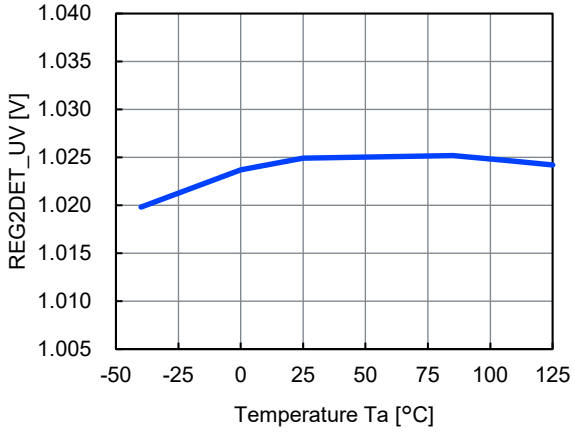


REG2DET

OV = 1.1750 V

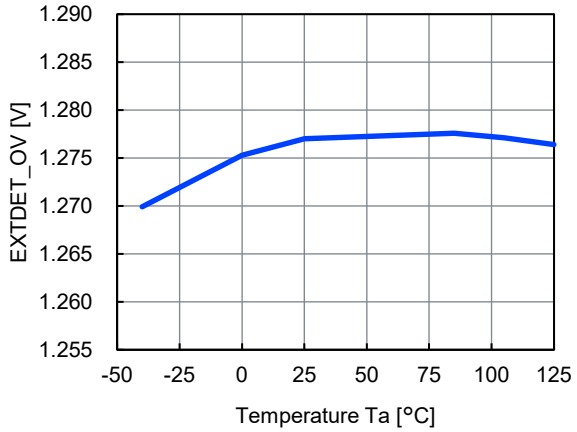


UV = 1.0250 V

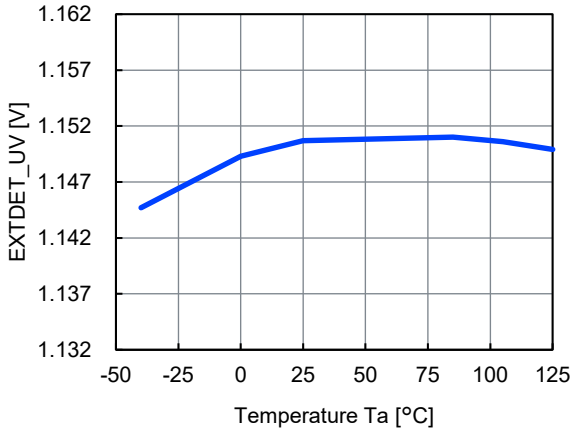


EXTDET

OV = 1.2750 V

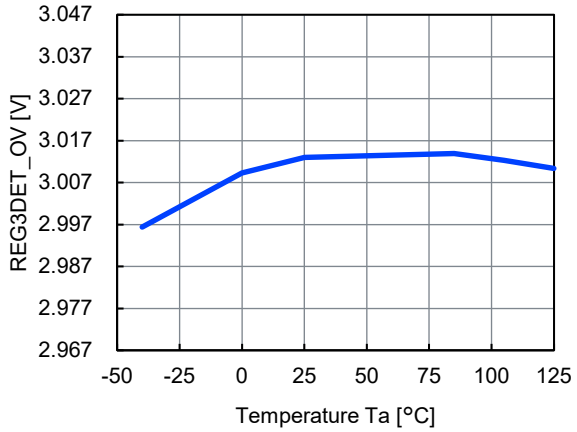


UV = 1.1500 V

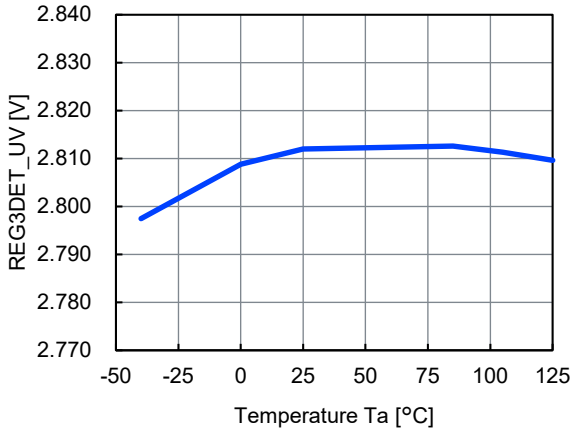


REG3DET

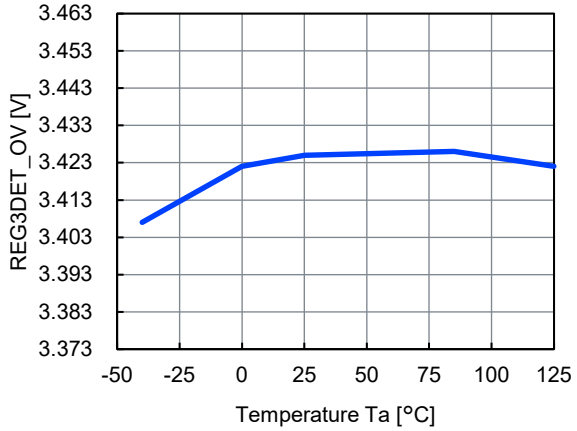
OV = 3.0125 V



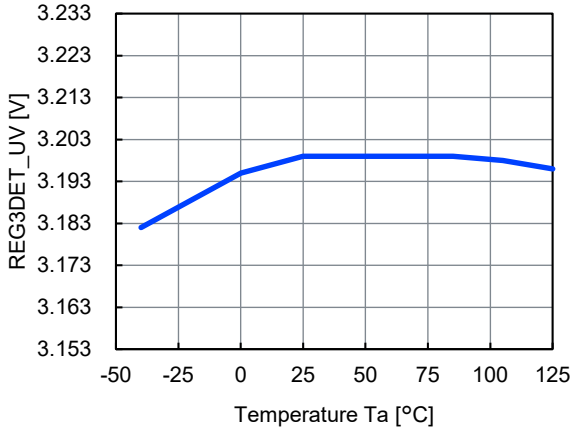
UV = 2.8125 V



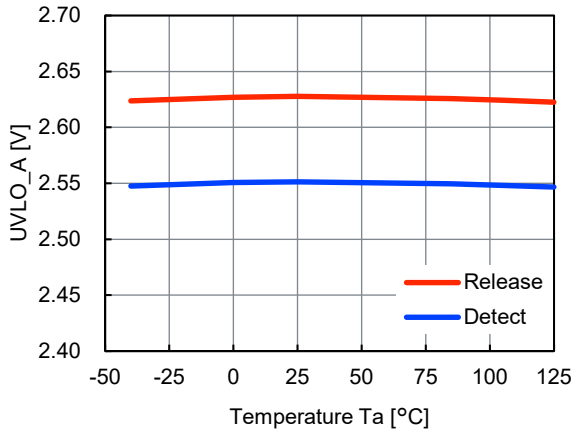
OV = 3.4250 V



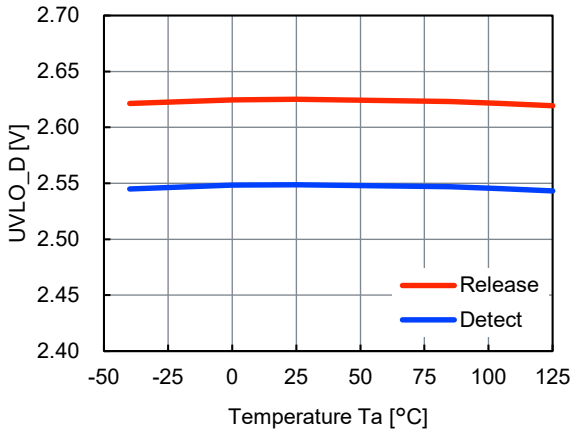
UV = 3.2000 V



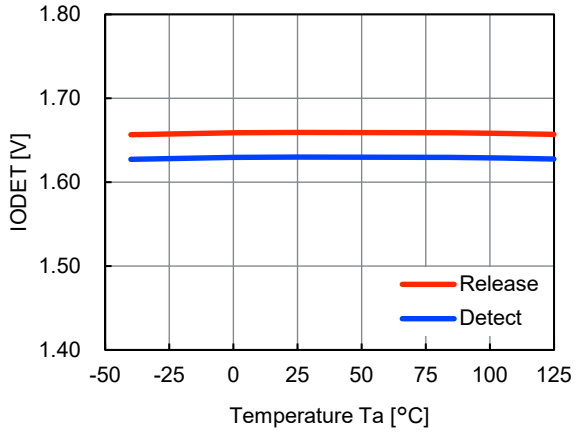
UVLO_A



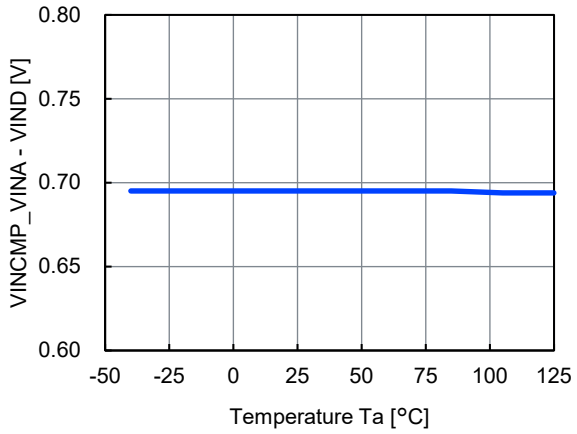
UVLO_D



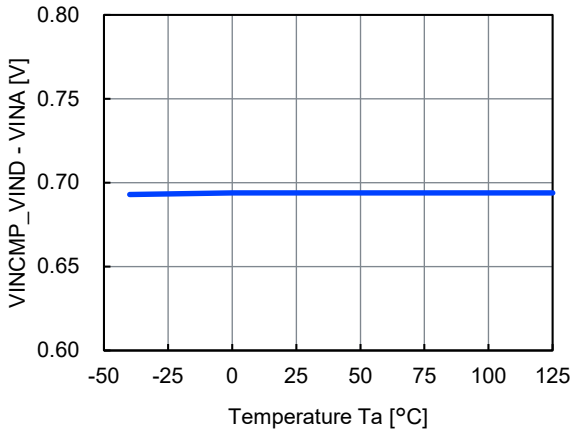
IODET



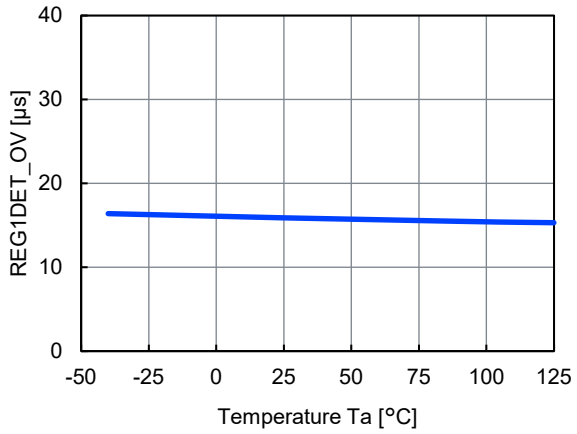
VINCMP
(VINA - VIND)



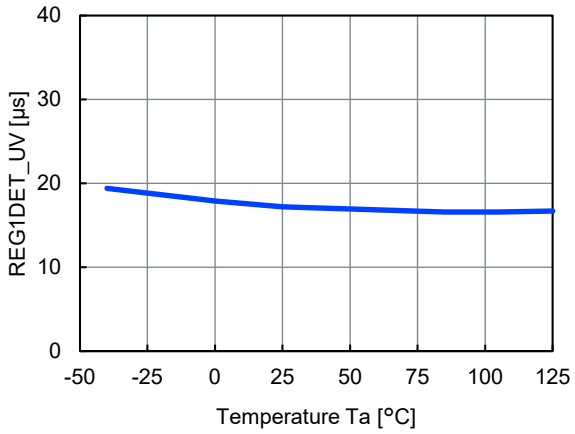
(VIND - VINA)



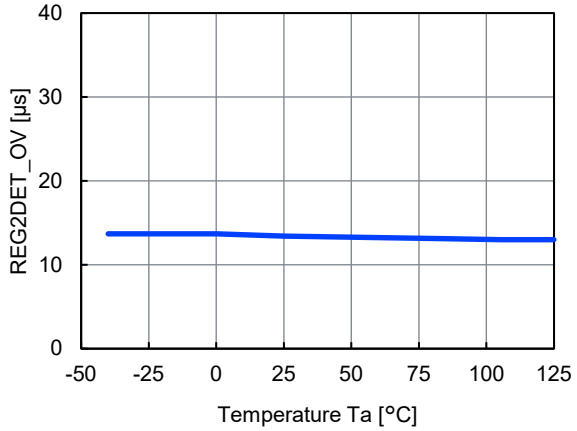
2) Detect Delay Time vs Temperature
V_{IN} = 5.0 V
REG1DET
OV = 1.8875 V



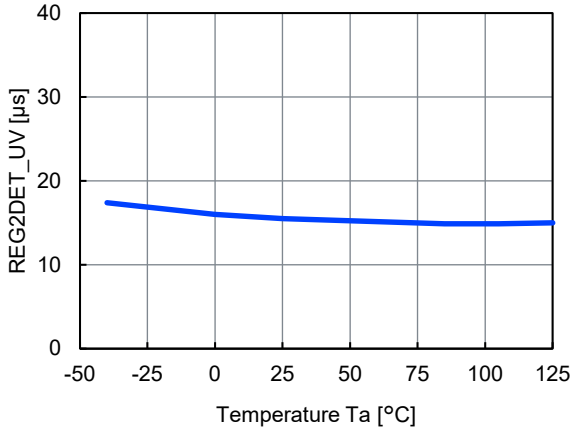
UV = 1.7250 V



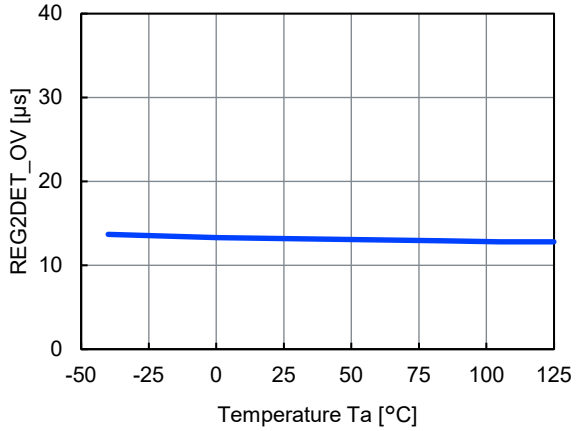
REG2DET
OV = 1.2750 V



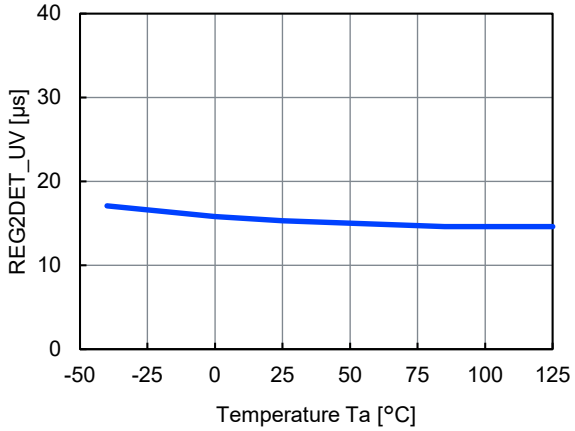
UV = 1.1250 V



REG2DET
OV = 1.1750 V

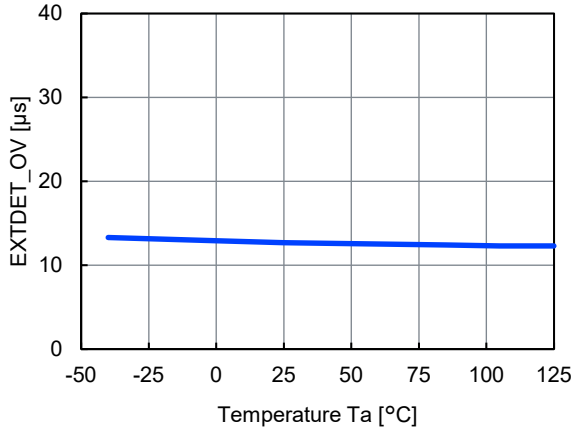


UV = 1.0250 V

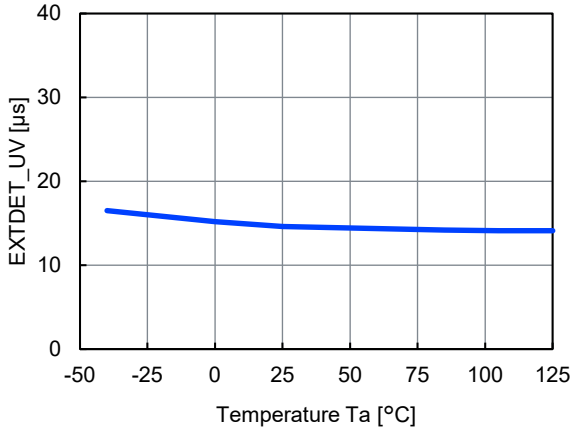


EXTDET

OV = 1.2750 V

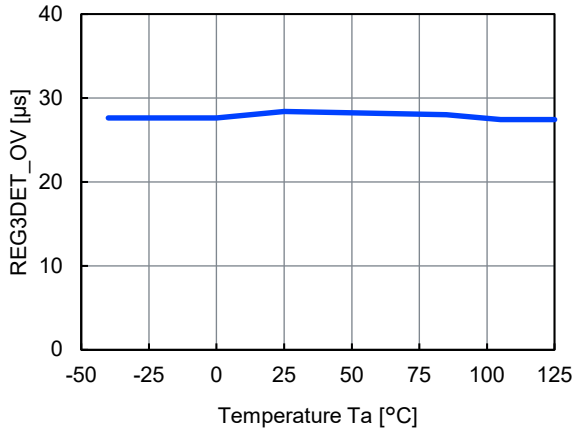


UV = 1.1500 V

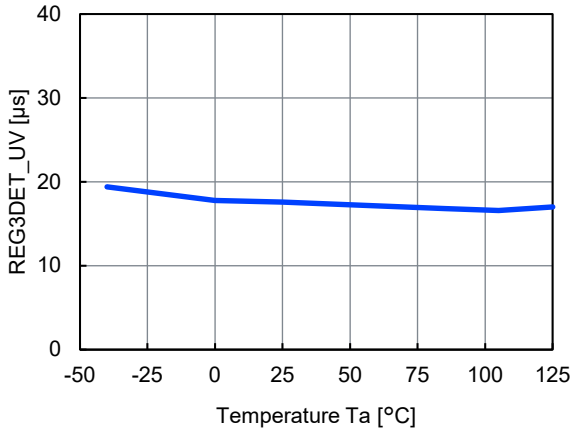


REG3DET

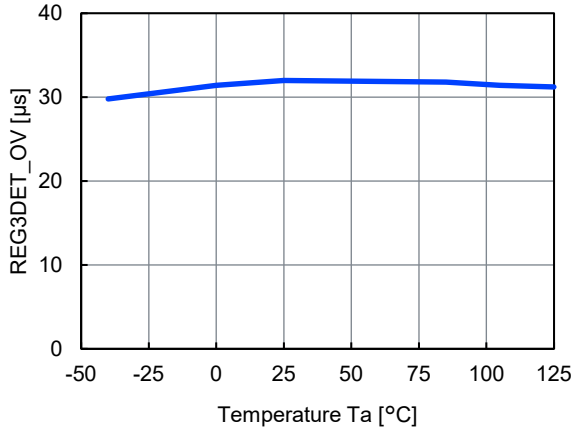
OV = 3.0125 V



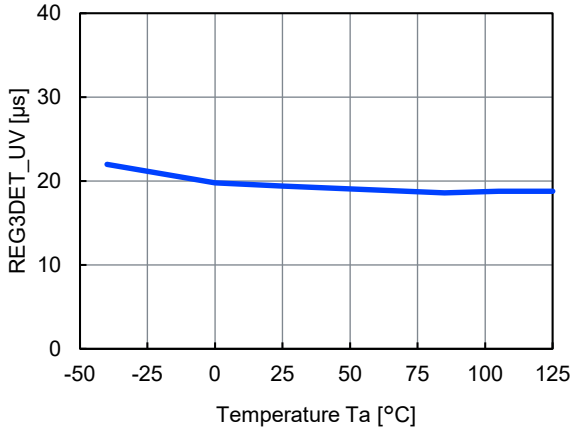
UV = 2.8125 V



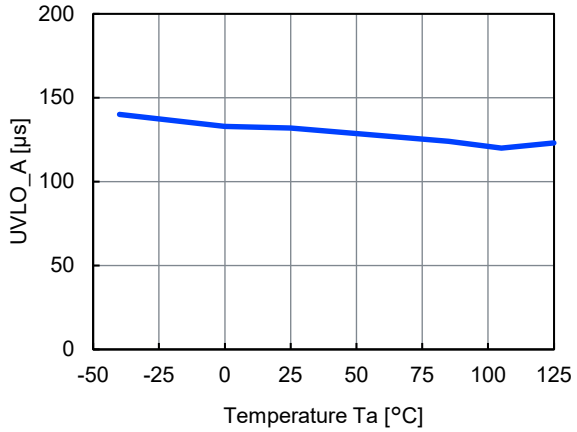
OV = 3.4250 V



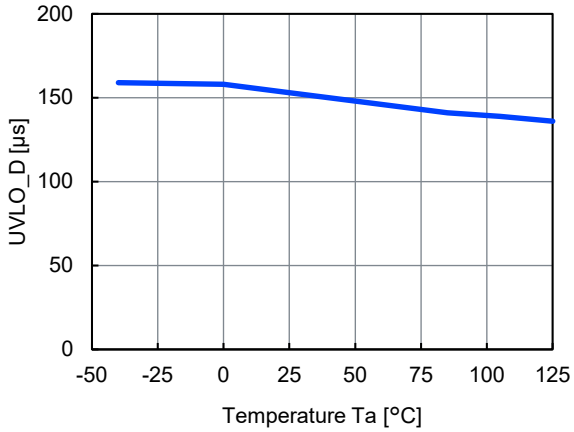
UV = 3.2000 V



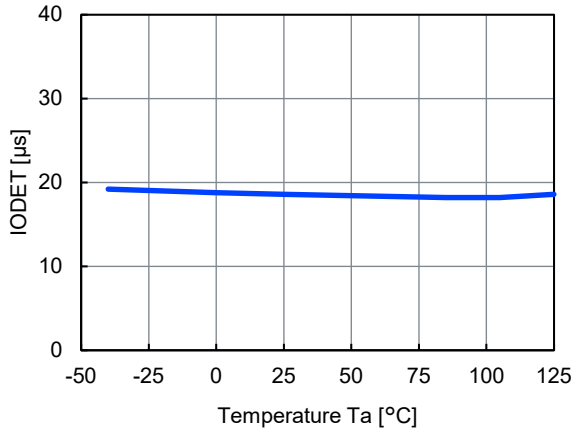
UVLO_A



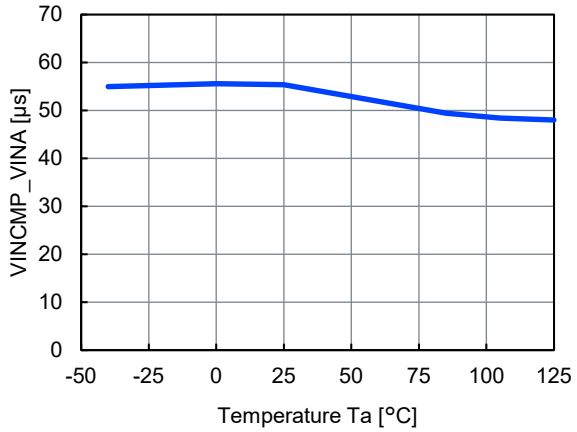
UVLO_D



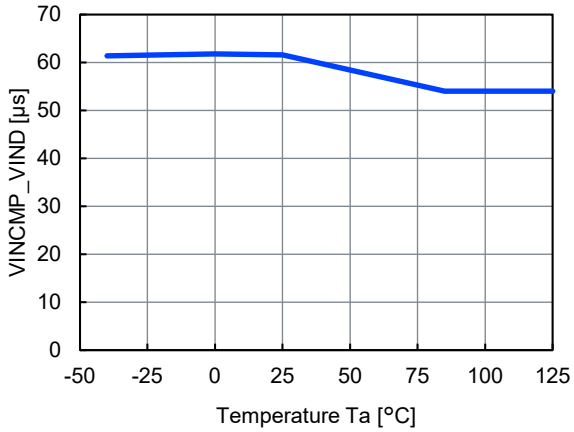
IODET



VINCMP(VINA)



VINCMP(VIND)

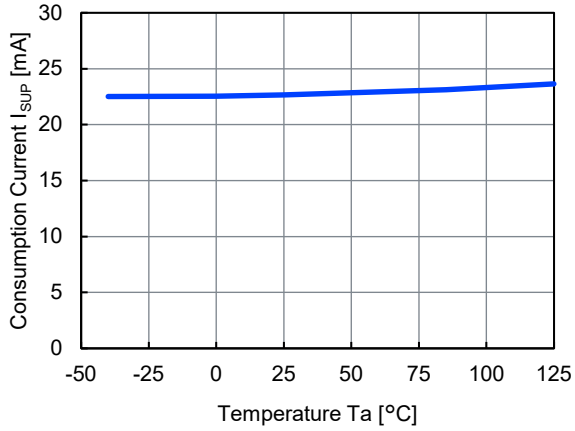


■ALL Typical Characteristics

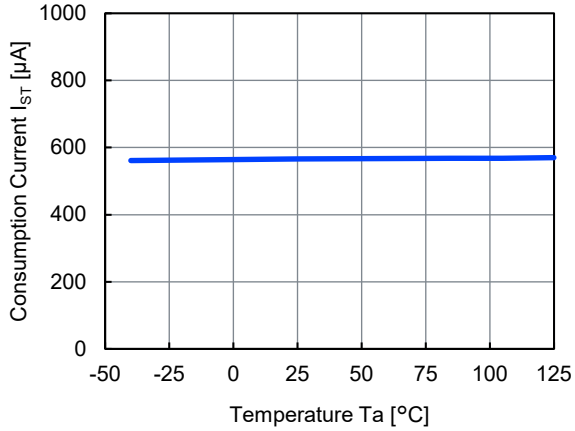
1) Consumption Current vs Temperature

V_{IN} = 5.0 V

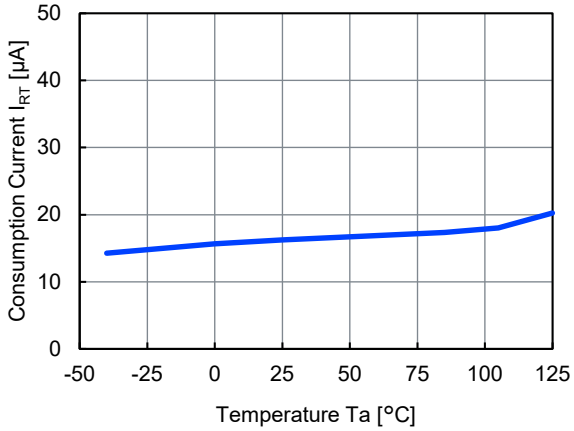
Power Supply State



Reset State



Ready State



PD-QFN0505-32-P7(125150)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51.

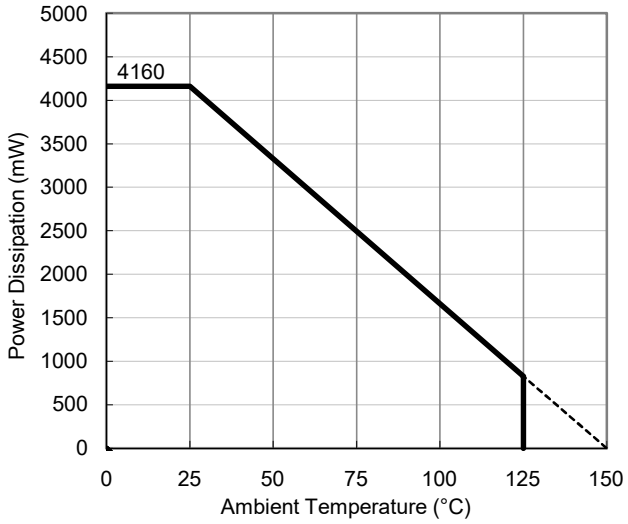
Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% Inner Layers (Second and Third Layers): Approx. 100% of 74.2 mm Square Outer Layer (Fourth Layer): Less than 10%
Through-holes	ϕ 0.3 mm × 9pcs

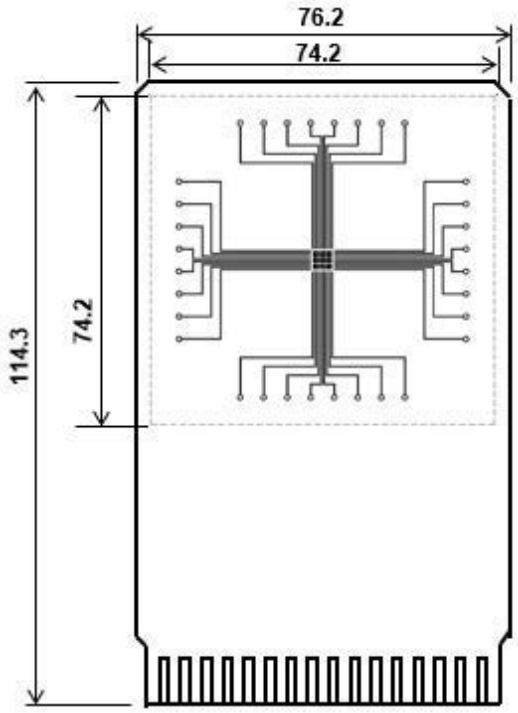
Measurement Result (Ta = 25°C, Tjmax = 150°C)

Item	Measurement Result
Power Dissipation	4160mW
Thermal Resistance (θja)	θja = 30°C/W

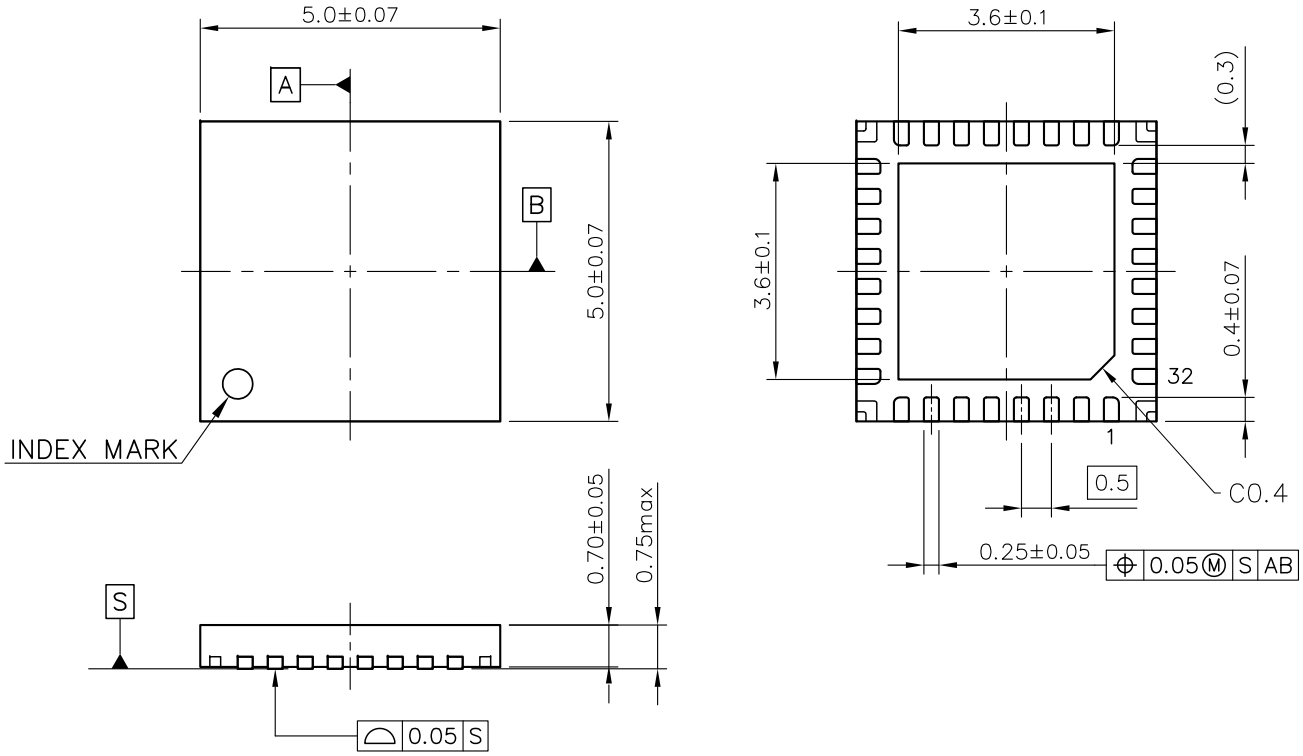
θja: Junction-to-Ambient Thermal Resistance



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



QFN0505-32-P7 Package Dimensions (Unit:mm)

Code List

In the RN5T5611 series, user can select a product code (-xx) depending on a target device's power supply, but the others except the "-02" code are under development, as of January in 2022.

Item	Description		Product Code（RN5T5611-xx）			
			-01	-02	-03	-04
System	Power Supply Voltage (V_{SYS_TYP})		5.0V	5.0V	5.0V	5.0V
	A3 Bit in I^2C Slave Address		0	0	0	0
	Mask of BIST Completion Interrupt		Mask	Mask	Mask	Mask
	Auto-restoration times		0	0	0	0
Sequence	Slot Width		1.8ms	1.8ms	1.8ms	1.8ms
	Power-on Slot	REG1	Slot_2	Slot_2	Slot_2	Slot_2
		REG2	Slot_3	Slot_3	Slot_3	Slot_3
		REG3	Slot_1	Slot_1	Slot_1	Slot_1
	Power-off Slot	REG1	Slot_2	Slot_2	Slot_2	Slot_2
		REG2	Slot_1	Slot_1	Slot_1	Slot_1
		REG3	Slot_3	Slot_3	Slot_3	Slot_3
	RESETO Output Slot		Slot_5	Slot_5	Slot_5	Slot_5
REGn	Output Voltage	REG1	1.8V	1.8V	1.8V	1.8V
		REG2	1.2V	1.1V	1.1V	1.2V
		REG3	2.9V	2.9V	3.3V	2.8V
	Soft-start Time	REG1	1.0ms	1.0ms	1.0ms	1.0ms
		REG2	1.0ms	1.0ms	1.0ms	1.0ms
		REG3	1.0ms	1.0ms	1.0ms	1.0ms
	Current Limit	REG1	1400mA	1400mA	1400mA	1400mA
		REG2	1400mA	1400mA	1400mA	1400mA
		REG3	100mA	100mA	100mA	100mA
DETn	REG1DET	OV Detection	1.8875V	1.8875V	1.8875V	1.8875V
		UV Detection	1.7250V	1.7250V	1.7250V	1.7250V
	REG2DET	OV Detection	1.2750V	1.1750V	1.1750V	1.2750V
		UV Detection	1.1250V	1.0250V	1.0250V	1.1250V
	REG3DET	OV Detection	3.0125V	3.0125V	3.4250V	2.9125V
		UV Detection	2.8125V	2.8125V	3.2000V	2.7125V

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    - Combustion equipment

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    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
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    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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