4.5V TO 40V INPUT, 600mA SYNCHRONOUS BUCK WITH ENHANCED EMI REDUCTION

Description

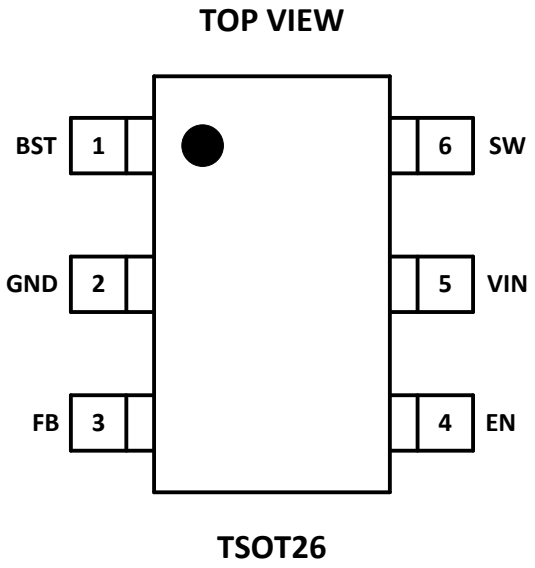
The DIODES™ AP64060Q is a 600mA, synchronous buck converter with a wide input voltage range of 4.5V to 40V. The device fully integrates a 600mΩ high-side power MOSFET and a 300mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP64060Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated loop compensation network.

The AP64060Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. The AP64060Q also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in the TSOT26 package.

Pin Assignments



Features

- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- VIN 4.5V to 40V
- 600mA Continuous Output Current
- Less than 0.1% Output Ripple at 12V
- 90μA Low Quiescent Current (Pulse Frequency Modulation)
- 2.2MHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM)
- Proprietary Gate Driver Design for Best EMI Reduction
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP64060Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- 5V, 12V, and 24V distributed power bus supplies
- eMeters
- Automotive devices
- White goods and small home appliances
- FPGA, DSP, and ASIC supplies
- General-purpose point-of-load (POL) devices

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

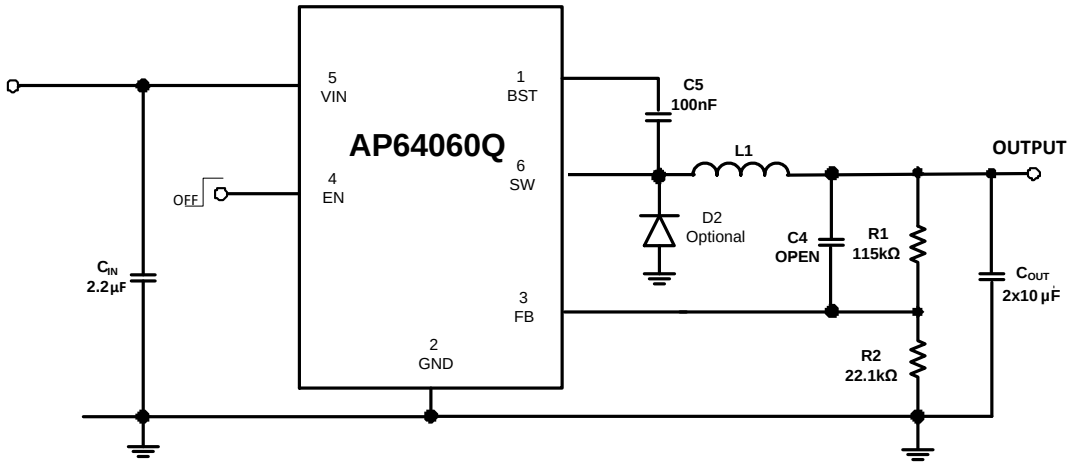


Figure 1. Typical Application Circuit

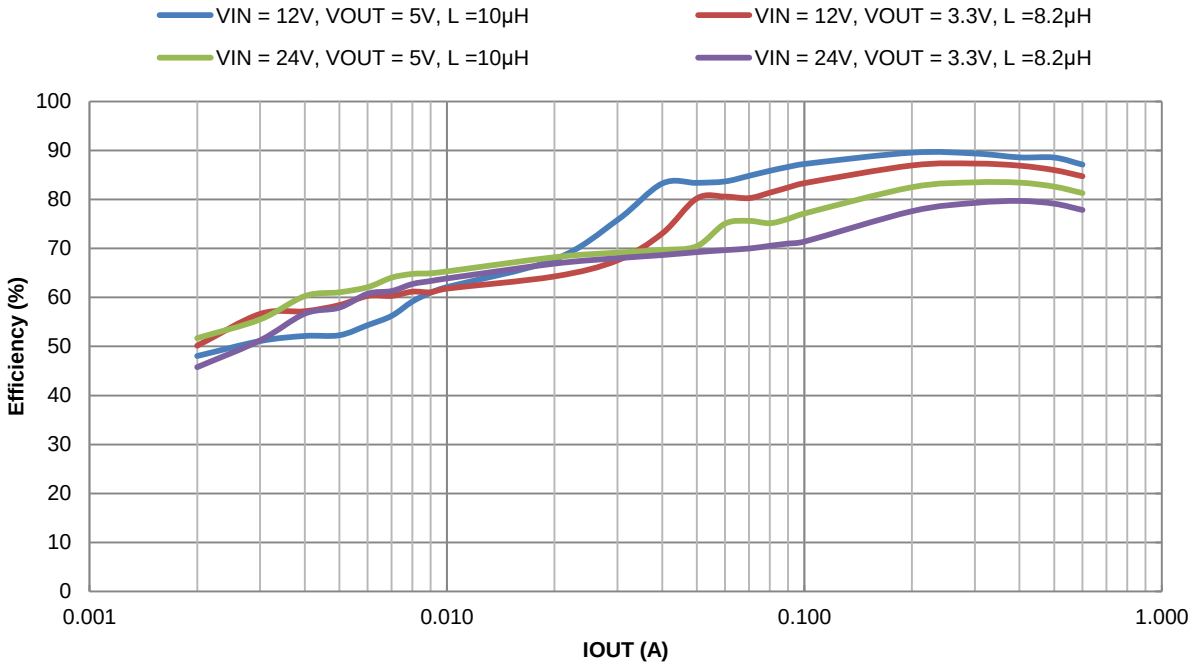


Figure 2. AP64060Q Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
BST	1	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
GND	2	Power Ground.
FB	3	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
EN	4	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN for automatic startup. The EN has a precision threshold of 1.21V for programing the UVLO. See **Enable** section for more details.
VIN	5	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 4.5V to 40V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
SW	6	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

Functional Block Diagram

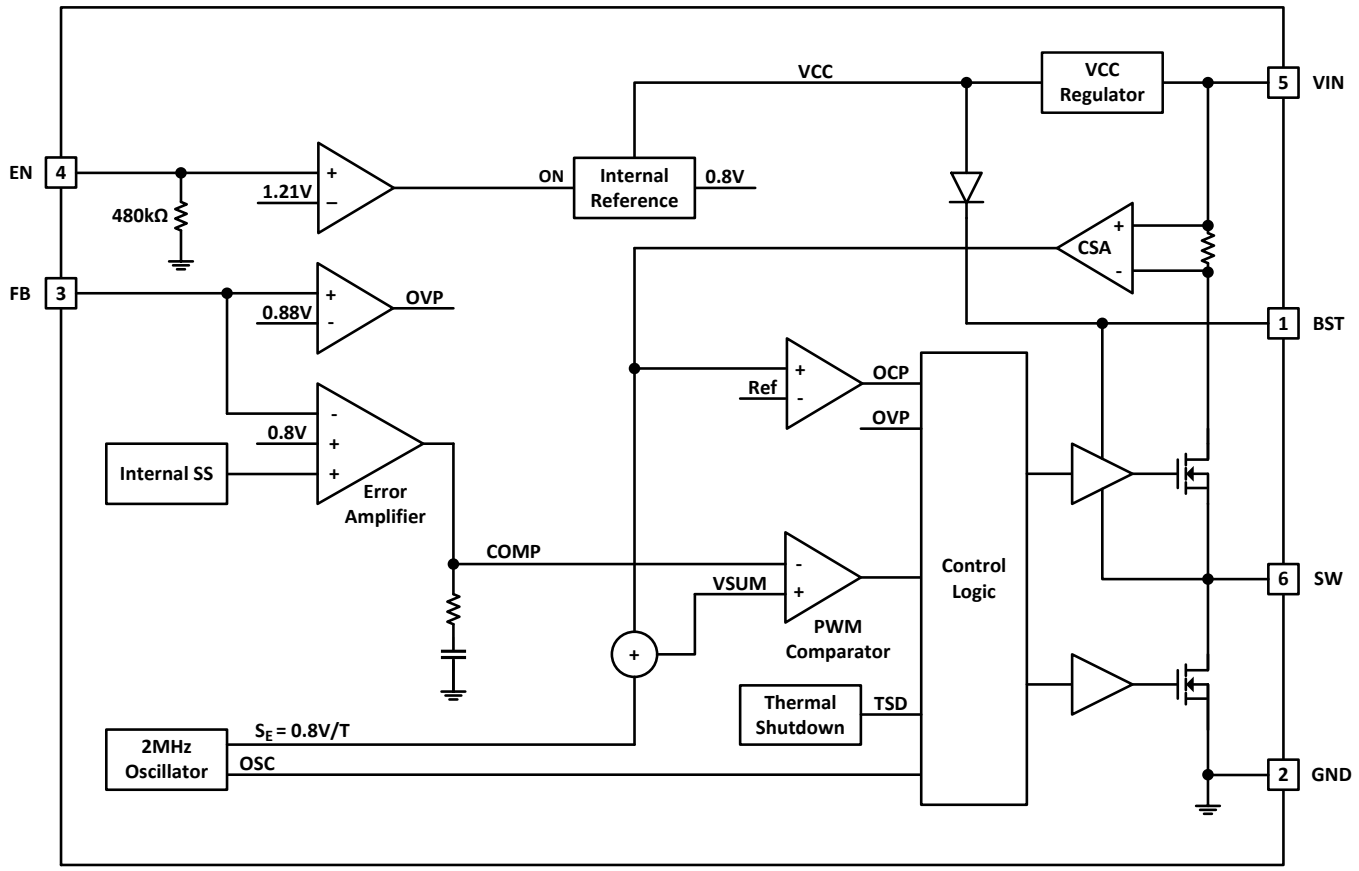


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +42.0 (DC)	V
		-0.3 to +46.0 (400ms)	
V_{FB}	Feedback Pin Voltage	-0.3V to +6.0	V
V_{EN}	Enable Pin Voltage	-0.3 to +42.0	V
V_{SW}	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+170	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±1000	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	TSOT26	80	°C/W
θ_{JC}	Junction to Case	TSOT26	39	°C/W

Note: 6. Test condition for TSOT26: Device mounted on FR-4 substrate, single-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	4.5	40	V
VOUT	Output Voltage	0.8	26	V
T_A	Operating Ambient Temperature Range	-40	+125	°C
T_J	Operating Junction Temperature Range	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input voltage range, 3.8V to 40V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	10	μA
I_Q	Supply Current (Quiescent)	V_{EN} = Floating, R2 = OPEN, No Load, V_{BST} - V_{SW} = 5V	—	90	—	μA
UVLO	VIN Undervoltage Rising Threshold	—	—	4.2	4.4	V
	VIN Undervoltage Hysteresis	—	—	440	—	mV
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	600	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	300	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	—	0.80	0.90	1.30	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	—	—	0.7	—	A
I_{PFMPK}	PFM Peak Current Limit	VOUT = 5V, L = 10μH	—	40	—	mA
I_{ZC}	Zero Cross Current Threshold	—	—	10	—	mA
f_{SW}	Oscillator Frequency	—	—	2	—	MHz
t_{ON_MIN}	Minimum On-Time	—	—	60	—	ns
V_{FB}	Feedback Voltage	CCM, T_J = -40ºC to +150 ºC	784	800	816	mV
V_{EN_H}	EN Logic High	—	—	1.21	1.25	V
V_{EN_L}	EN Logic Low	—	1.03	1.10	—	V
t_{SS}	Soft-Start Time	—	—	1	—	ms
T_{SD}	Thermal Shutdown Threshold (Note 8)	—	—	170	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	35	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (@ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

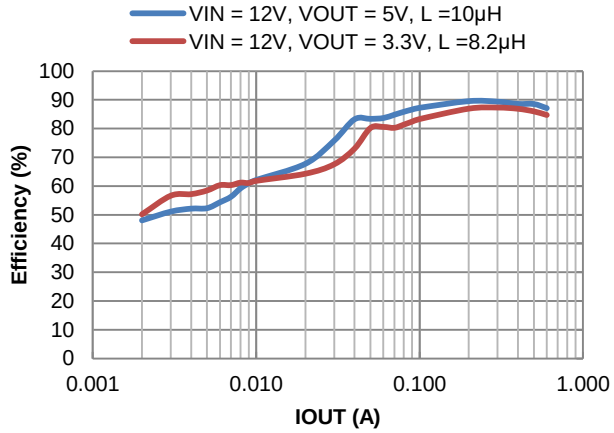


Figure 4. Efficiency vs. Output Current, VIN = 12V

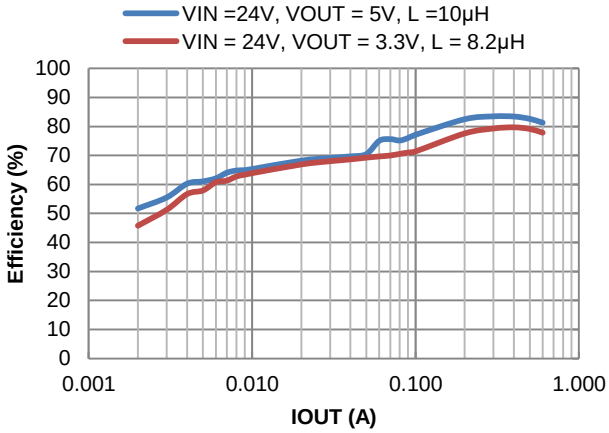


Figure 5. Efficiency vs. Output Current, VIN = 24V

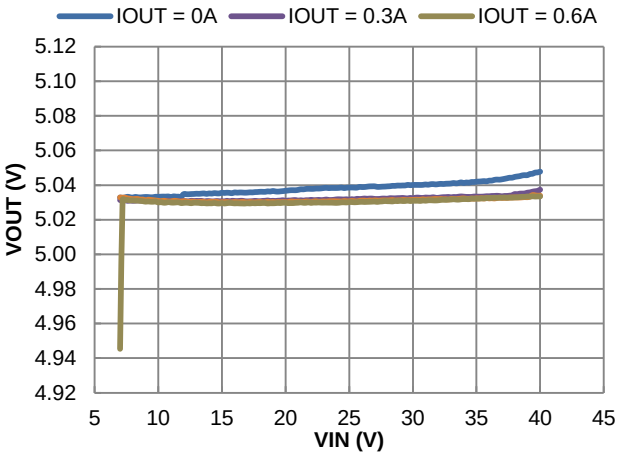


Figure 6. Line Regulation

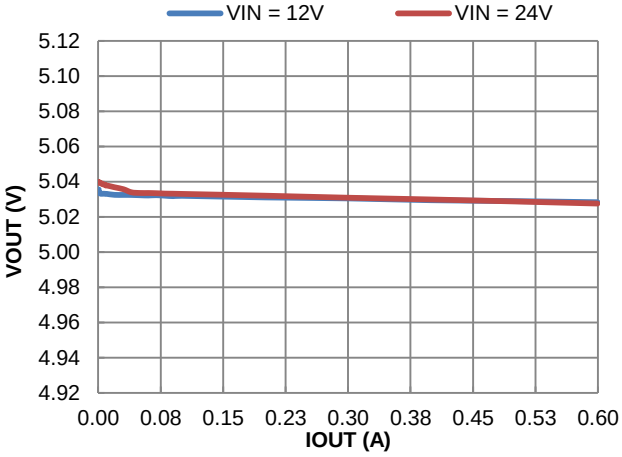


Figure 7. Load Regulation

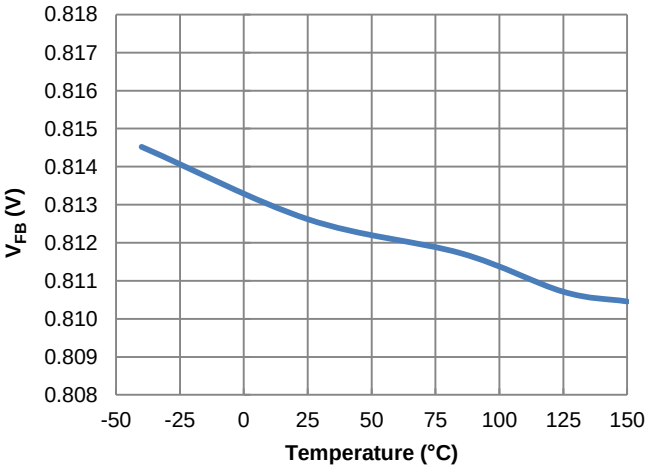


Figure 8. Feedback Voltage vs. Temperature

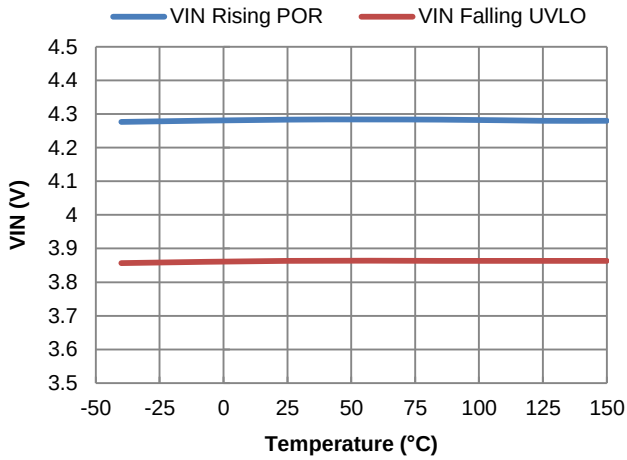


Figure 9. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (@ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

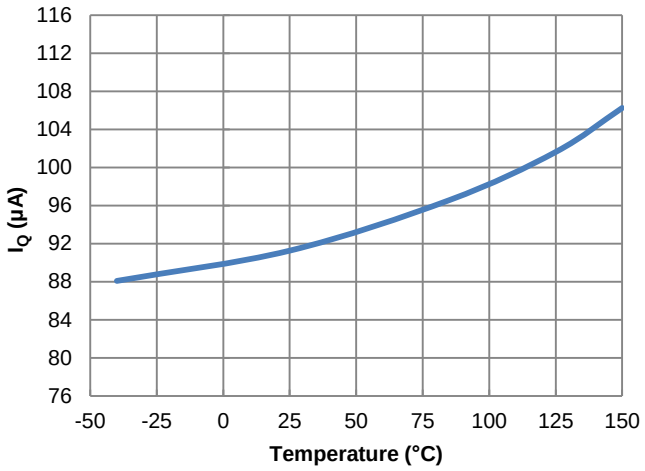


Figure 10. I_Q vs. Temperature

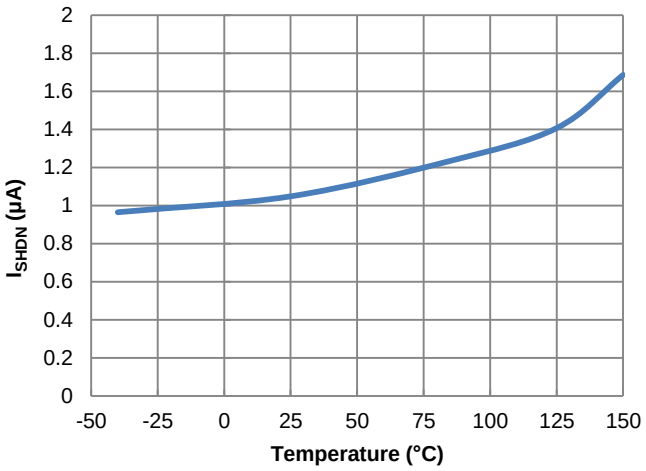


Figure 11. I_{SHDN} vs. Temperature

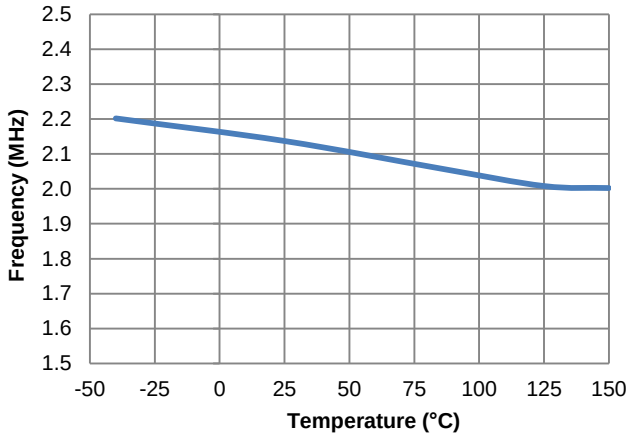


Figure 12. f_{SW} vs. Temperature

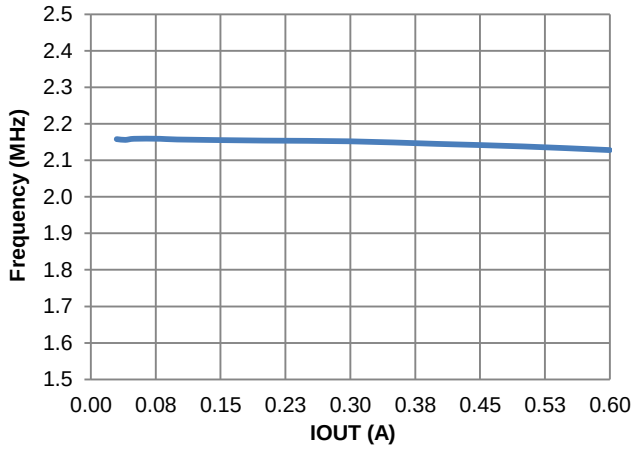


Figure 13. f_{SW} vs. IOUT (A)

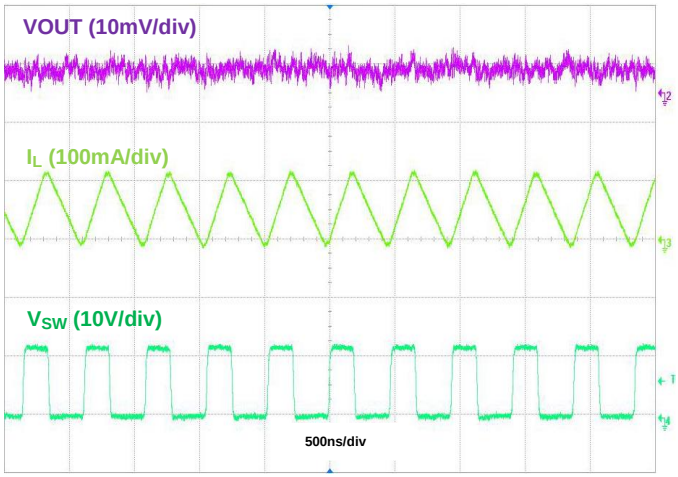


Figure 14. Output Voltage Ripple, VOUT = 5V; IOUT = 50mA

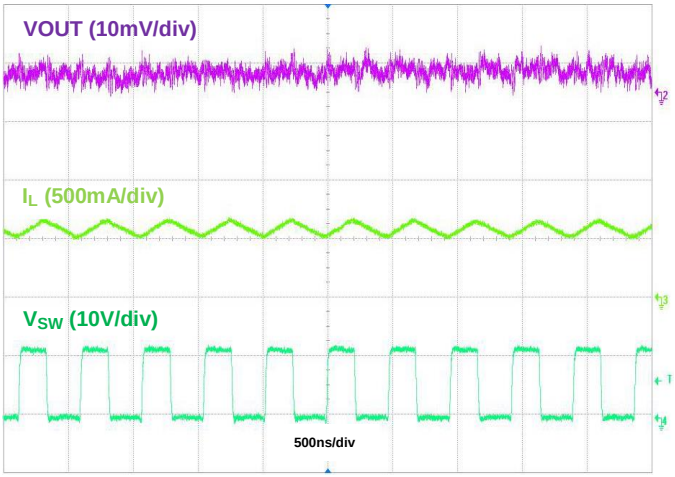


Figure 15. Output Voltage Ripple, VOUT = 5V; IOUT = 600mA

Typical Performance Characteristics (@ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

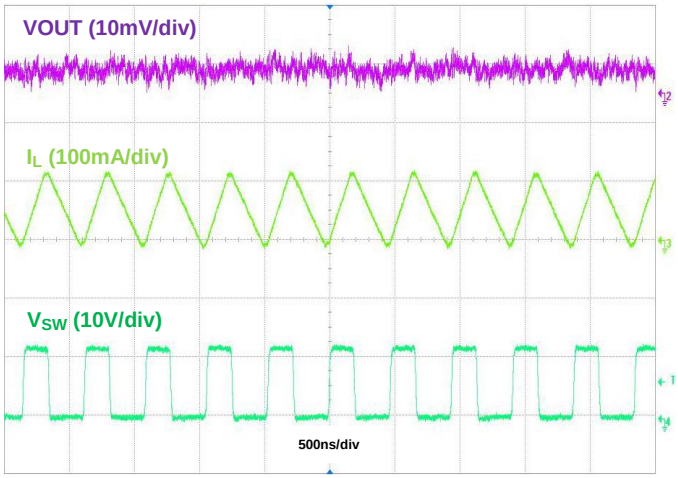


Figure 16. Output Voltage Ripple, VOUT = 3.3V; IOUT = 50mA

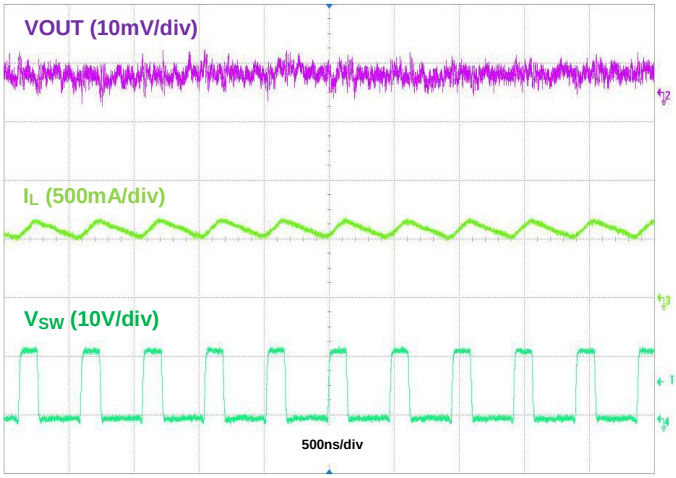


Figure 17. Output Voltage Ripple, VOUT = 3.3V; IOUT = 600mA

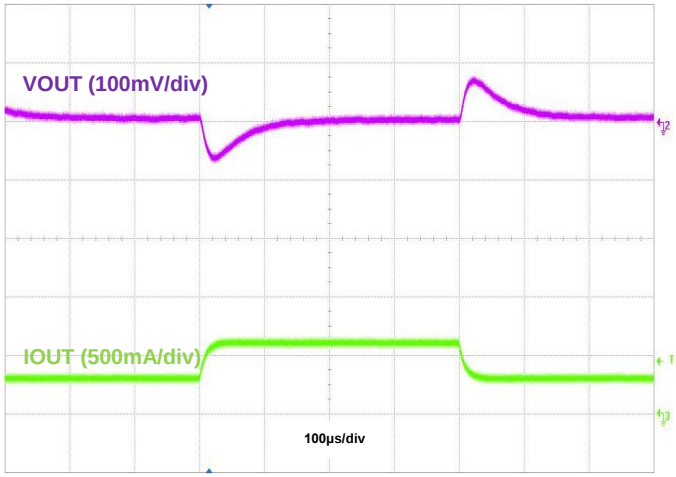


Figure 18. Load Transient, VIN = 12V, IOUT = 300mA to 600mA

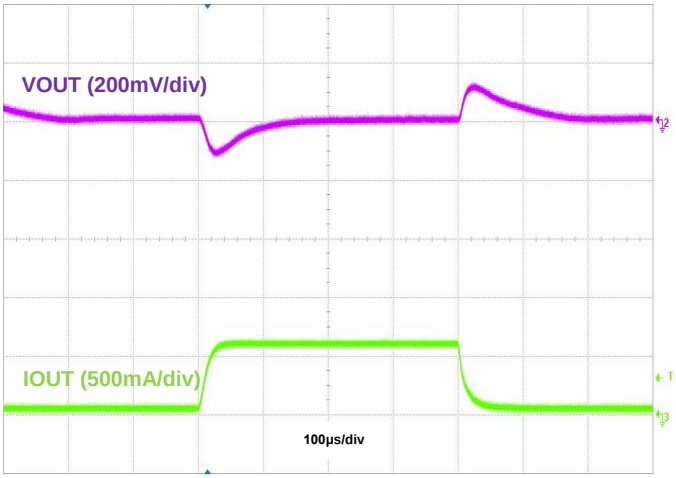


Figure 19. Load Transient, VIN = 12V, IOUT = 50mA to 600mA

Typical Performance Characteristics (@T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

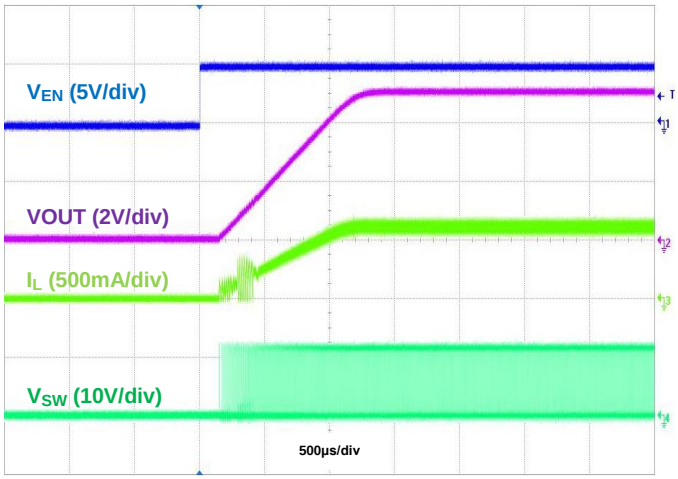


Figure 20. Startup Using EN, IOUT = 600mA

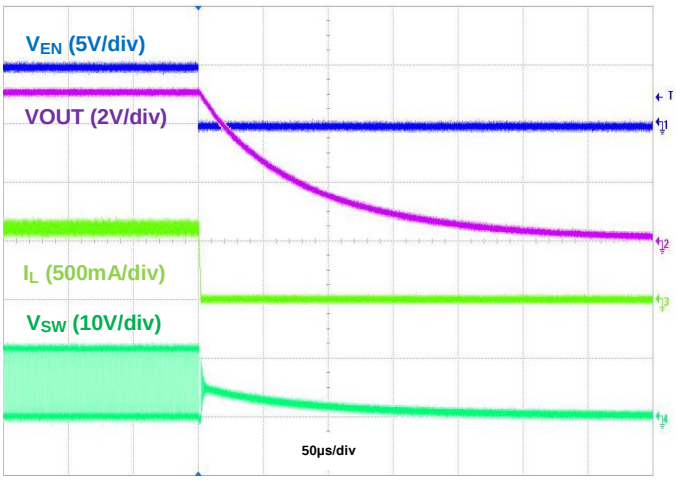


Figure 21. Shutdown Using EN, IOUT = 600mA

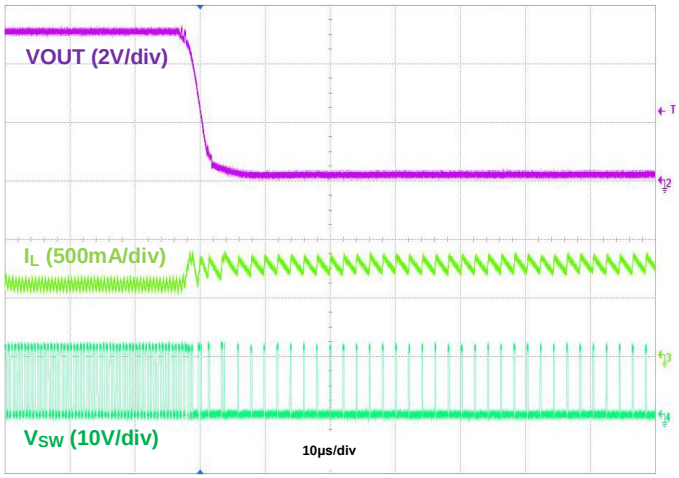


Figure 22. Output Short Protection, IOUT = 600mA

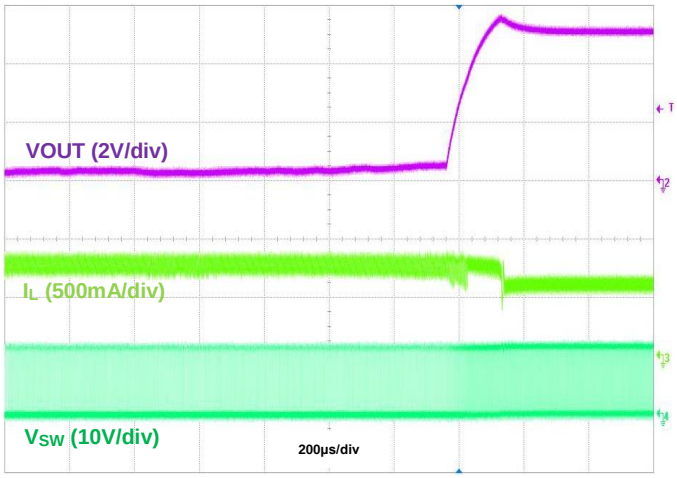


Figure 23. Output Short Recovery, IOUT = 600mA

Application Information

Pulse Width Modulation (PWM) Operation

The AP64060Q device is a 4.5V-to-40V input, 600mA output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 4. The device employs fixed-frequency peak current mode control. The internal 2MHz clock's rising edge initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The peak current mode control, integrated loop compensation network, and built-in 4ms soft-start time simplifies the AP63108Q/AP63109Q footprint as well as minimizes the external component count.

Pulse Frequency Modulation (PFM) Operation

In heavy load conditions, the AP64060Q operates in forced PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 200mA PFM peak inductor current limit. As the load current approaches zero, the AP64060Q enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 50mA, zero cross detection circuitry on the low-side power MOSFET, Q2, forces it off. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP64060Q works in PFM during light load conditions, it can achieve power efficiency of up to 82% at a 5mA load condition.

The quiescent current of the AP64060Q is 90μA typical under a no-load, non-switching condition.

Enable

When disabled, the device shutdown supply current is only 1μA. When applying a voltage greater than the EN logic high threshold (typical 1.21V, rising), the AP64060Q enables all functions and the device initiates the soft-start phase. The EN pin is a high-voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases. The AP64060Q has a built-in 1ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.10V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP64060Q device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP64060Q disables if the input voltage falls below 3.8V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

For applications requiring higher VIN UVLO threshold voltages than is provided by the default setup, an external resistor R3 added in series to the EN pin along with an internal 480kΩ configures the VIN UVLO threshold voltages as shown in Figure 24.

Application Information (continued)

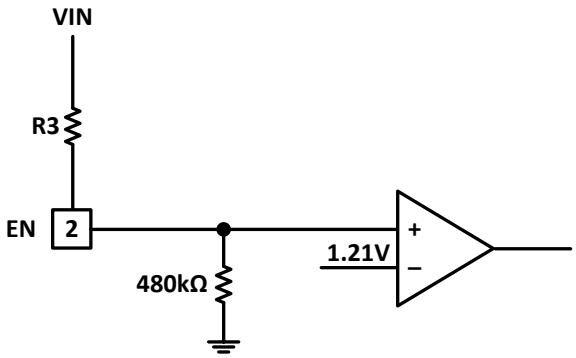


Figure 24. Programming UVLO

The resistive divider resistor values are calculated by:

$$\mathbf{R3 = 480k\Omega \frac{(V_{ON} - 1.21V)}{1.21V}} \quad \textbf{Eq. 1}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 4.2V

Output Overvoltage Protection (OVP)

The AP64060Q implements output OVP circuitry to minimize output voltage overshoots during decreasing load transients. The high-side power MOSFET turns off and the low-side power MOSFET turns on when the output voltage exceeds its target value by 10% in order to prevent the output voltage from continuing to increase.

Overcurrent Protection (OCP)

The AP64060Q has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. Once the current through Q1 exceeds the peak current limit, Q1 immediately turns off.

Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of 170°C, the AP64060Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (135°C typical), the device initiates a normal power-up cycle with soft-start.

Application Information (continued)

Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA}) \quad \text{Eq. 2}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 3}$$

Where:

- T_A is the ambient temperature of the environment

For the TSOT26 package, the θ_{JA} is 80°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of 150°C when considering the thermal design. Figure 25 shows a typical derating curve versus ambient temperature.

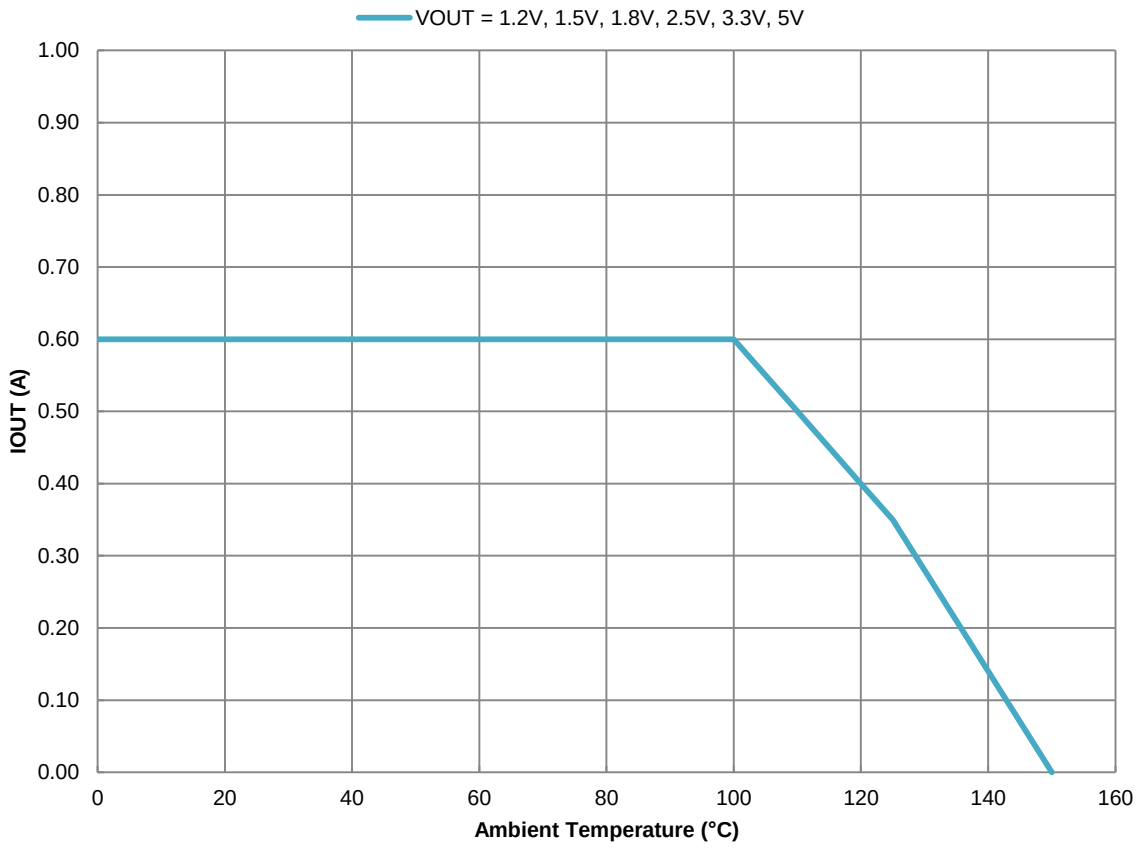


Figure 25. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

Application Information (continued)

Setting the Output Voltage

The AP64060Q has adjustable output voltages starting from 0.8V using an external resistive divider. An optional external capacitor, C4 in Figure 1, of 10pF to 220pF improves the transient response. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.8V} - 1\right)} \qquad \textbf{Eq. 4}$$

Table 1 shows a list of recommended component selections for common AP64060Q output voltages referencing Figure 1.

Table 1. Recommended Component Selections

AP64060Q							
Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)	C3 (nF)	C4 (pF)
1.8	27.4	22.1	4.7	2.2	10x2	100	OPEN
2.5	47.5	22.1	6.8	2.2	10x2	100	OPEN
3.3	69.8	22.1	8.2	2.2	10x2	100	OPEN
5.0	115	22.1	10	2.2	10x2	100	OPEN
12.0	309	22.1	22	2.2	10x3	100	OPEN

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{sw}}} \qquad \textbf{Eq. 5}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For the AP64060, choose ΔI_L to be 20% to 30% of the maximum load current of 1A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \qquad \textbf{Eq. 6}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 4.7µH to 22µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 70mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (continued)

Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor greater than 10µF is sufficient for most applications.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8 \cdot f_{sw} \cdot COUT}} \right) \quad \textbf{Eq. 7}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L \cdot I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L \cdot I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 8}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

Bootstrap Capacitor and Low-Dropout (LDO) Operation

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins. A 100nF ceramic capacitor is sufficient. If the bootstrap capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 220ns to refresh the bootstrap capacitor and raise its voltage back above 2.85V. The bootstrap capacitor voltage threshold is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event that requires the refreshing of the bootstrap capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low-dropout mode by holding Q1 on for multiple clock cycles. To prevent the bootstrap capacitor from discharging, Q2 is forced to refresh.

Layout

PCB Layout

1. The AP64060Q works at 600mA load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 26 for more details.

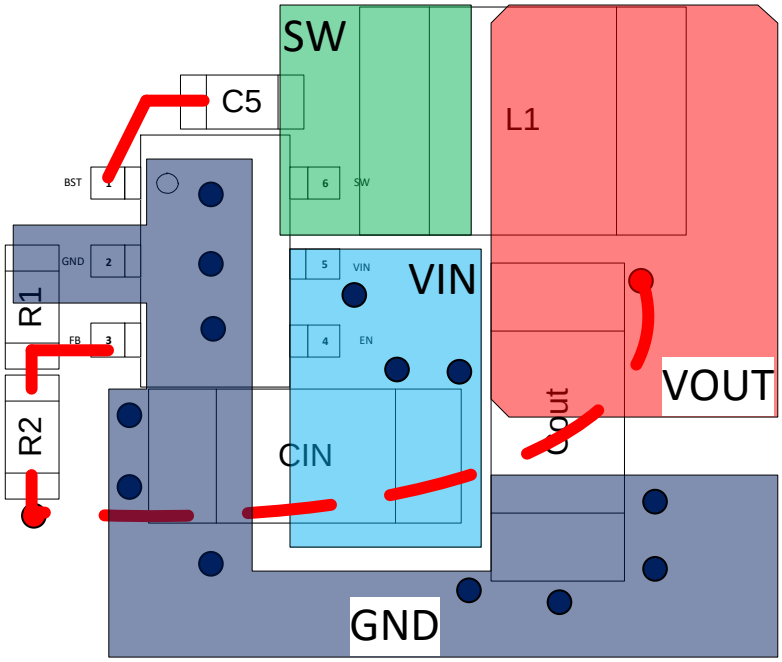
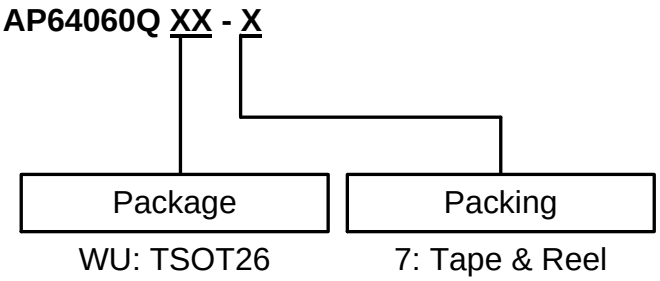


Figure 26. Recommended PCB Layout

Ordering Information

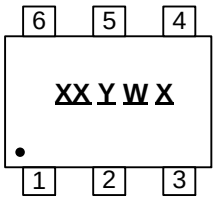


Part Number	Operation Mode	Package	Package Code	Packing	
				Qty.	Carrier
AP64060QWU-7	PFM/PWM	TSOT26	WU	3000	7" Tape & Reel

Marking Information

TSOT26

(Top View)



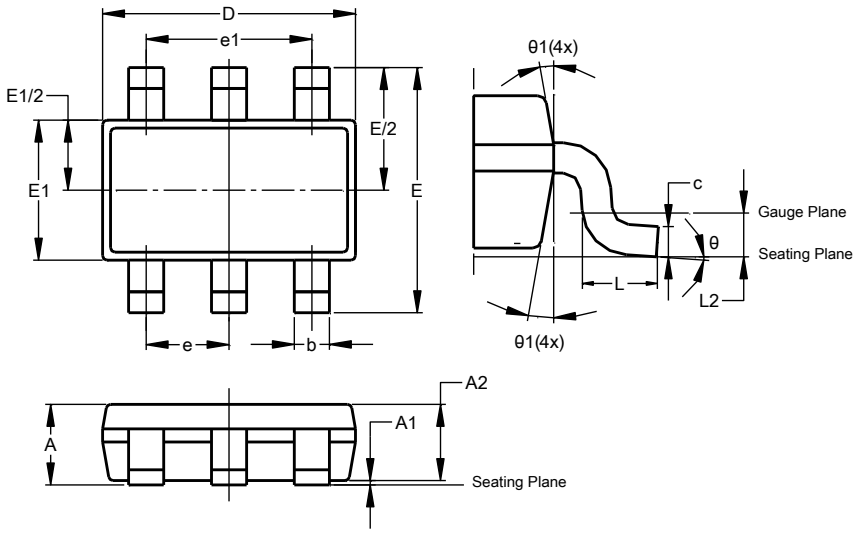
XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP64060QWU-7	TSOT26	TGQ

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26

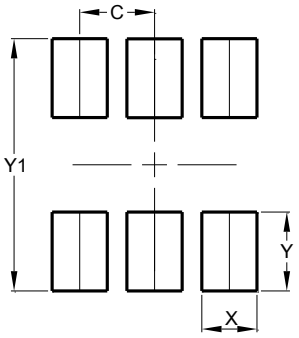


TSOT26			
Dim	**Min**	**Max**	**Typ**
A	—	1.00	—
A1	0.010	0.100	—
A2	0.840	0.900	—
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	—
c	0.120	0.200	—
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	—
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	—
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.200

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