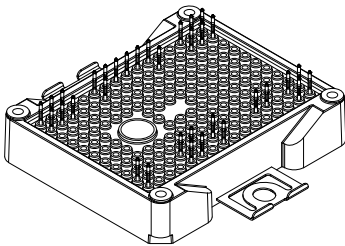
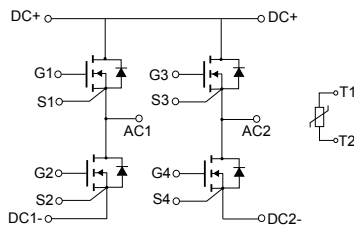


## ACEPACK 2 power module, fourpack topology, 1200 V, 13 mΩ typ. SiC Power MOSFET gen.2 with NTC


**ACEPACK 2**


### Features

- Fourpack topology
- ACEPACK 2 power module
  - 13 mΩ of typical  $R_{DS(on)}$  each switch
  - Insulation voltage UL certified of 2.5 kVrms
  - Integrated NTC temperature sensor
  - DBC Cu-Al<sub>2</sub>O<sub>3</sub>-Cu based
  - Press fit contact pins

### Applications

- DC/DC converter

### Description

This ACEPACK 2 power module in fourpack topology integrates advanced silicon carbide Power MOSFET technology from STMicroelectronics. The module leverages the innovative properties of the wide-bandgap SiC material and a high-thermal-performance substrate. The result is exceptionally low on-resistance per unit area and excellent switching performance that is virtually independent of temperature. An NTC sensor completes the design.



#### Product status link

[A2F12M12W2-F1](#)

#### Product summary

<b>Order code</b>	A2F12M12W2-F1
<b>Marking</b>	A2F12M12W2-F1
<b>Package</b>	ACEPACK 2
<b>Leads type</b>	Press fit
<b>Packing</b>	Tray

# 1 Electrical rating

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	1200	V
$V_{GS}$	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
$I_D$	Drain current (continuous) at $T_H = 25\text{ °C}$	75	A
$I_{DM}^{(1)}$	Repetitive peak drain current	150	A
$T_J$	Maximum junction temperature	175	°C
	Operating junction temperature range under switching conditions	-40 to 150	

1. Pulse width limited by maximum junction temperature.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJH}$	Thermal resistance, junction-to-heat sink ( $T_{IM} = 80\text{ }\mu\text{m}$ , $\lambda = 3\text{ W}\cdot\text{m}^{-1}\cdot\text{°C}^{-1}$ )	0.43	°C/W

## 2 Electrical characteristics

**Table 3. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1200			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}$ , $I_D = 75\text{ A}$		13	17	mΩ
		$V_{GS} = 18\text{ V}$ , $I_D = 75\text{ A}$ , $T_J = 150\text{ °C}$		20		
$V_{GS(th)}$	Gate threshold voltage	$I_D = 10\text{ mA}$ , $V_{DS} = V_{GS}$	1.9	3.0	4.9	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 1200\text{ V}$ , $V_{GS} = 0\text{ V}$			200	μA
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0$ , $V_{GS} = -10\text{ to }22\text{ V}$			±1	μA
$C_{iss}$	Input capacitance	$f = 1\text{ MHz}$ , $V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$		7000		pF
$C_{oss}$	Output capacitance			440		pF
$C_{rss}$	Reverse transfer capacitance			56		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$		1		Ω
$Q_g$	Total gate charge	$V_{DD} = 800\text{ V}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $I_D = 100\text{ A}$		294		nC
$Q_{gs}$	Gate-source charge			65		nC
$Q_{gd}$	Gate-drain charge			109		nC

**Table 4. Switching energy**

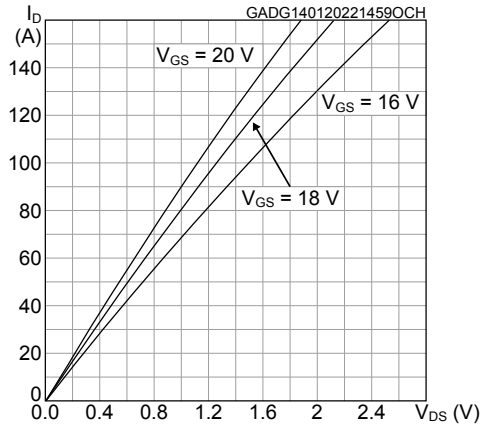
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}$	Turn-on switching energy	$V_{DD} = 800\text{ V}$ , $I_D = 75\text{ A}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $R_G = 5.6\text{ Ω}$	-	1.48	-	mJ
$E_{off}$	Turn-off switching energy			-	0.35	
$E_{on}$	Turn-on switching energy	$V_{DD} = 800\text{ V}$ , $I_D = 75\text{ A}$ , $V_{GS} = -5\text{ to }18\text{ V}$ , $R_G = 5.6\text{ Ω}$ , $T_J = 150\text{ °C}$	-	1.51	-	mJ
$E_{off}$	Turn-off switching energy			-	0.32	

**Table 5. Source-drain diode**

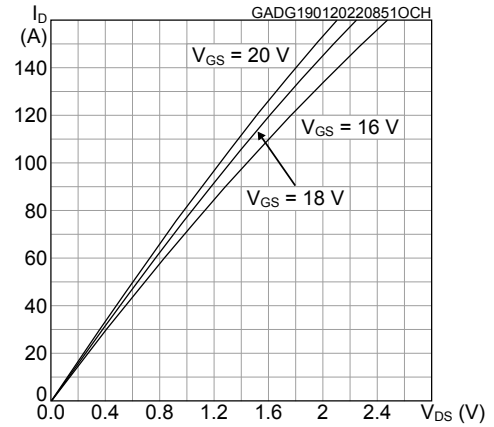
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward on voltage drop	$V_{GS} = 0\text{ V}$ , $I_{SD} = 75\text{ A}$	-	2.9	-	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 75\text{ A}$ , $V_{DD} = 800\text{ V}$ , $V_{GS} = -5\text{ V}$	-	42	-	ns
$Q_{rr}$	Reverse recovery charge		-	896	-	nC
$I_{RRM}$	Reverse recovery current		-	60	-	A
$E_{rr}$	Reverse recovery energy		-	336	-	μJ

## 2.1 Electrical characteristics (curves)

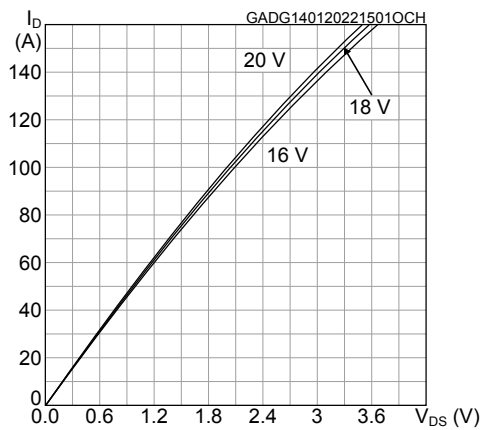
**Figure 1. Typical output characteristics ( $T_J = -40^\circ\text{C}$ )**



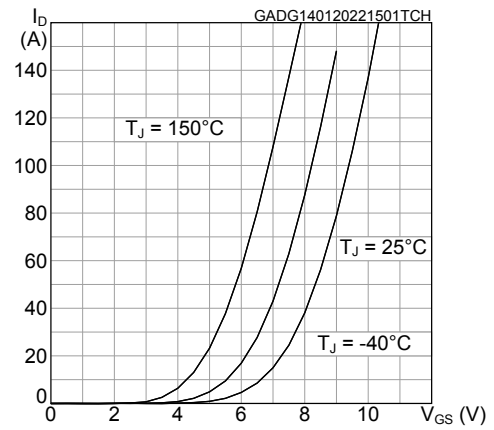
**Figure 2. Typical output characteristics ( $T_J = 25^\circ\text{C}$ )**



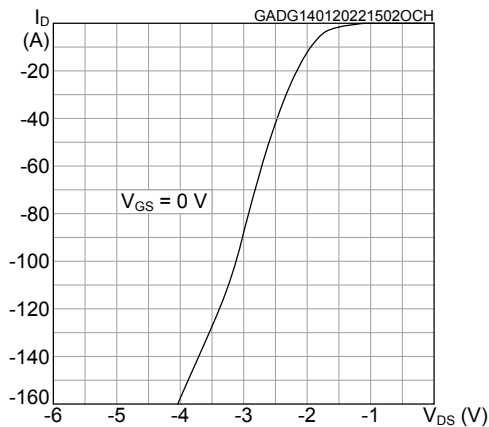
**Figure 3. Typical output characteristics ( $T_J = 150^\circ\text{C}$ )**



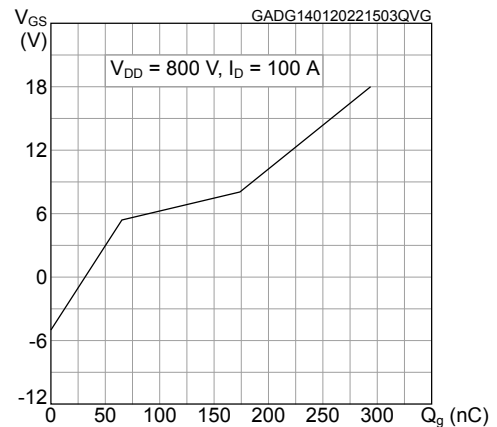
**Figure 4. Typical transfer characteristics**



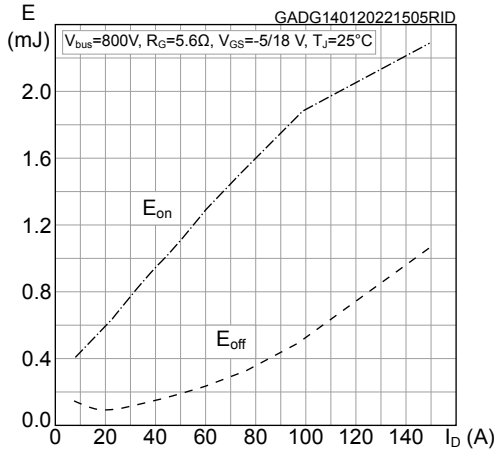
**Figure 5. Typical diode forward characteristics (terminal)**



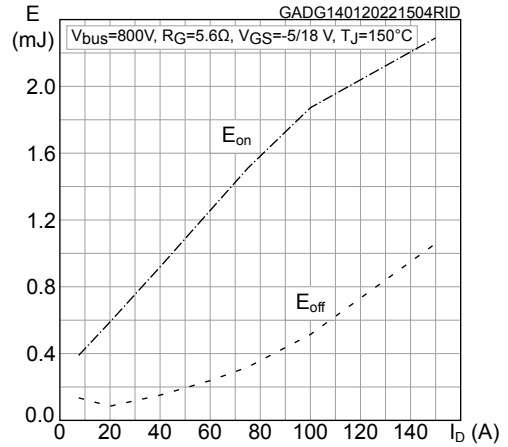
**Figure 6. Typical gate charge characteristics**



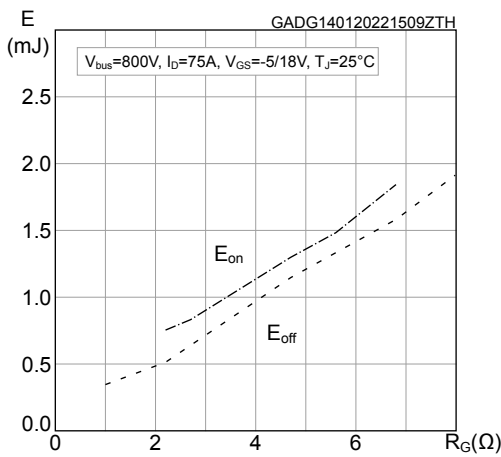
**Figure 7. Typical switching energy vs drain current**  
( $T_J = 25^\circ\text{C}$ )



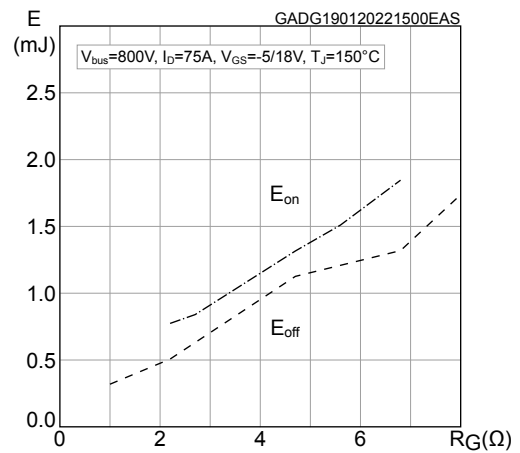
**Figure 8. Typical switching energy vs drain current**  
( $T_J = 150^\circ\text{C}$ )



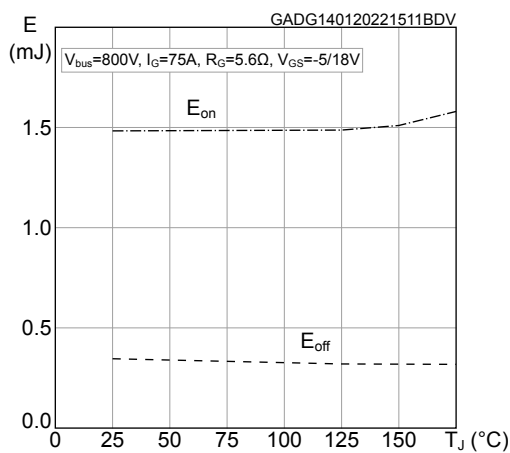
**Figure 9. Typical switching energy vs gate resistance**  
( $T_J = 25^\circ\text{C}$ )



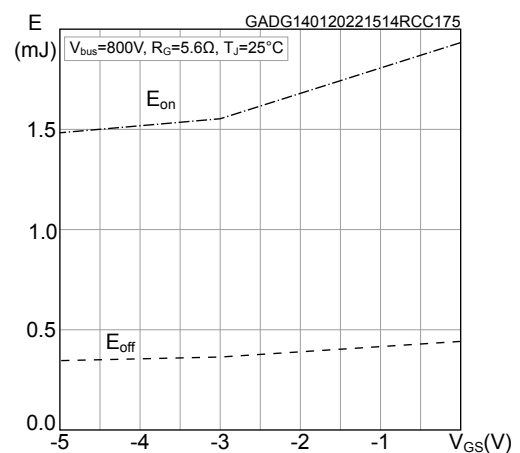
**Figure 10. Typical switching energy vs gate resistance**  
( $T_J = 150^\circ\text{C}$ )



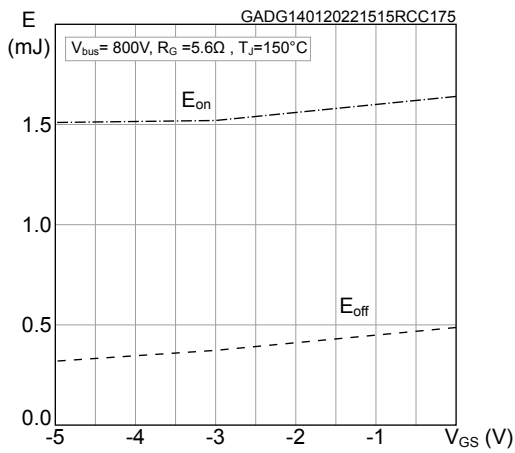
**Figure 11. Typical switching energy vs temperature**



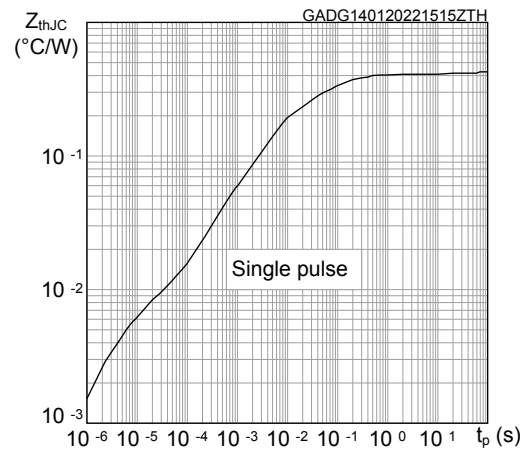
**Figure 12. Typical switching energy vs  $V_{GS}$  ( $T_J = 25^\circ\text{C}$ )**



**Figure 13. Typical switching energy vs  $V_{GS}$  ( $T_J = 150\text{ }^\circ\text{C}$ )**



**Figure 14. Maximum transient thermal impedance**

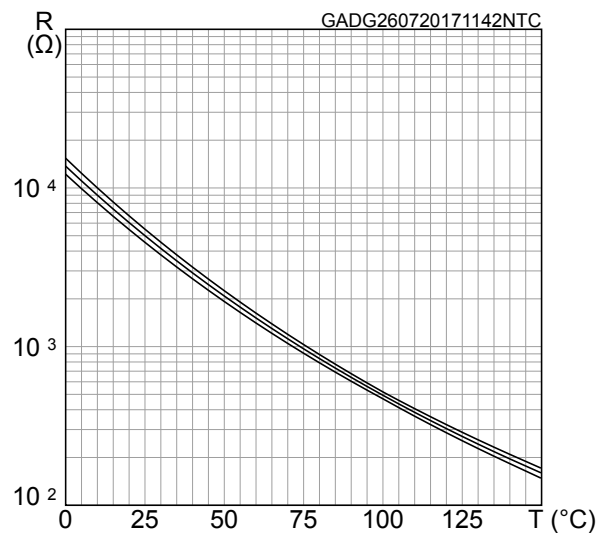


### 3 NTC

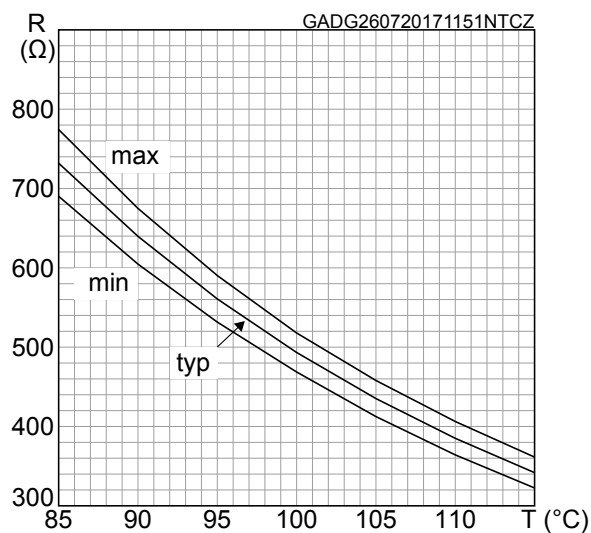
**Table 6. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R <sub>25</sub>	Resistance rating	T = 25 °C		5		kΩ
R <sub>100</sub>	Resistance rating	T = 100 °C		493		Ω
ΔR <sub>100</sub> /R	Resistance tolerance		-5		5	%
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

**Figure 15. NTC typical resistance vs temperature**



**Figure 16. NTC resistance vs temperature, zoom**



## 4 Package

Table 7. ACEPACK 2 package

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{ISO}$	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, $t = 60$ s)	2.5			kVrms
$M_d$	Mounting torque (M4 screw)	2.0		2.3	N•m
CTI	Comparative tracking index	200			
$L_s$	Stray inductance module loop		12		nH
$T_{stg}$	Storage temperature range	-40		125	°C



## 5 Electrical topology and pin description

Figure 17. Electrical topology and pin description

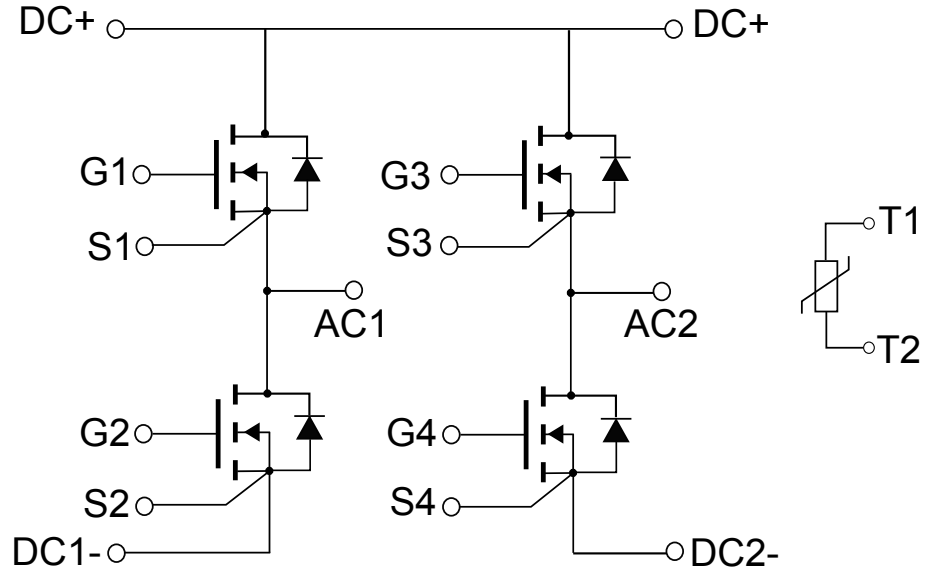
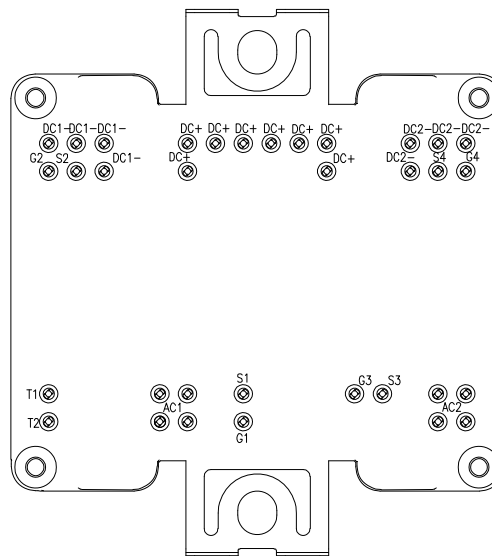


Figure 18. Package top view with pinout



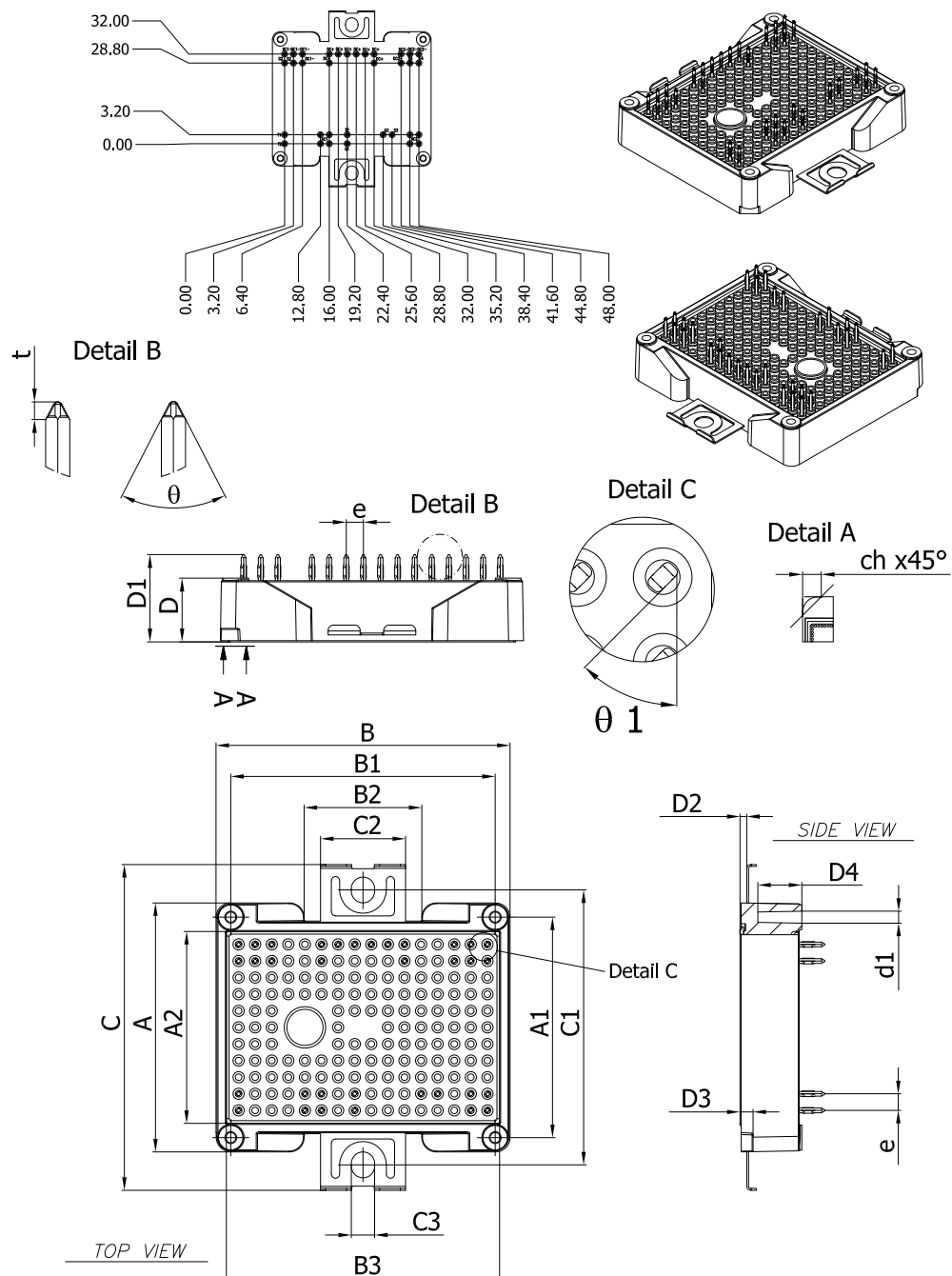
GADG051020211046SA

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 6.1 ACEPACK 2 fourpack press fit package information

Figure 19. ACEPACK 2 fourpack press fit package outline (dimensions are in mm)

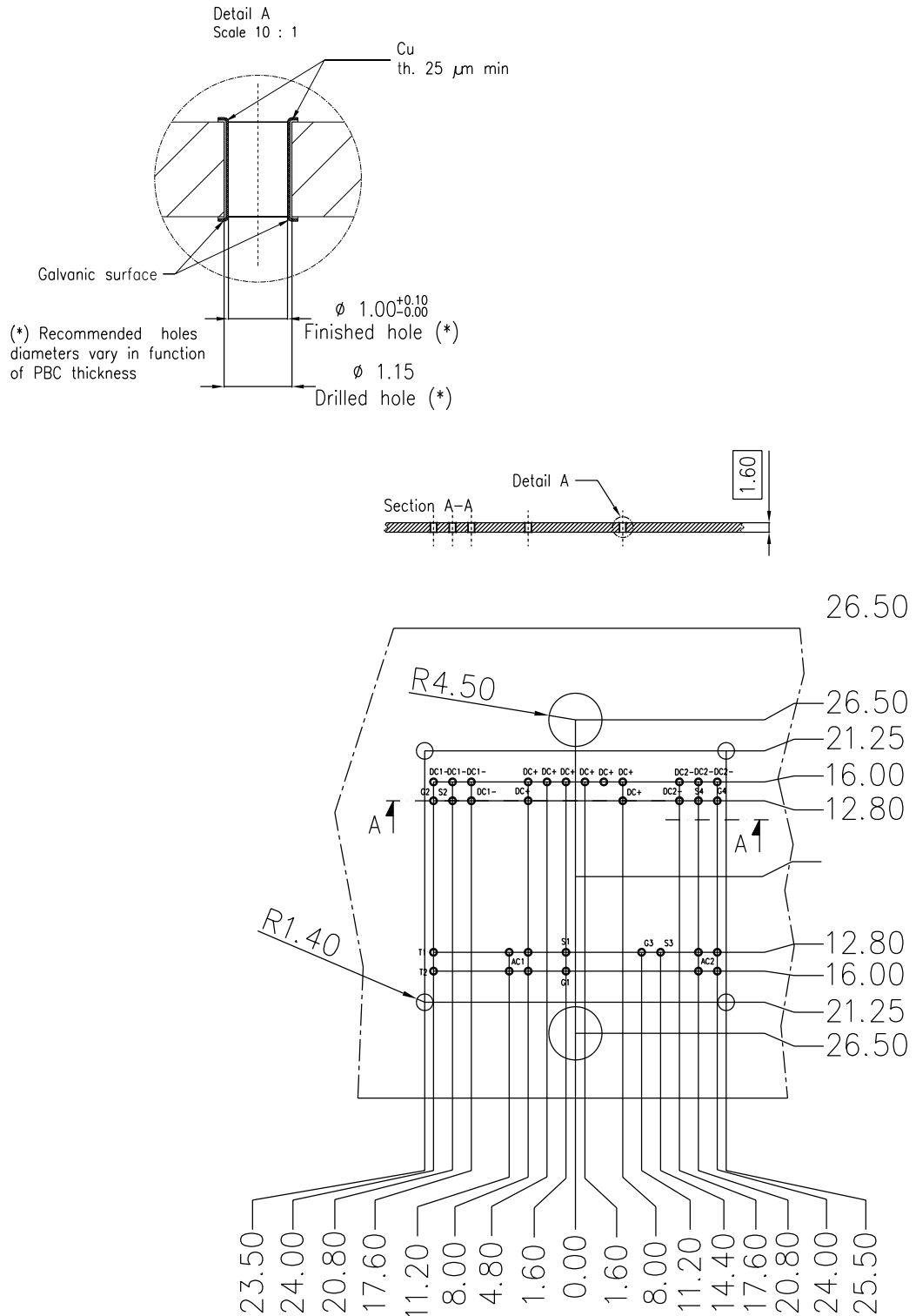


8569722\_12\_fourpack\_press\_fit

**Table 8. ACEPACK 2 fourpack press fit mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2	37.00 REF		
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3	52.70 REF		
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
e	3.20 BSC		
d1	2.30 REF		
ch	3.50 REF		

Figure 20. ACEPACK 2 fourpack press fit recommended PCB holes layout (dimensions are in mm)



8569722\_12\_fourpack\_press\_fit\_holes\_layout

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
18-Oct-2021	1	First release.
01-Feb-2022	2	<p>Updated the description in cover page, <i>Table 2. Thermal data</i>, <i>Table 3. Electrical characteristics</i> and <i>Table 5. Source drain diode</i>.</p> <p>Updated <i>Table 7. ACEPACK 2 package</i>.</p> <p>Added <i>Section 4 Electrical characteristics (curves)</i>.</p> <p>Minor text changes.</p>
11-Feb-2022	3	<p>Updated title, features and description in cover page.</p> <p>Updated <i>Section 1 Electrical rating</i>, <i>Section 3 NTC</i>, <i>Section 4 Package</i> and <i>Section 5 Electrical topology and pin description</i>.</p> <p>Added <i>Section 2 Electrical characteristics</i>.</p> <p>Minor text changes.</p>

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