2.7 V to 5.5 V Input, 4 A Single Synchronous Buck DC/DC Converter for Automotive

BD9S402MUF-C

General Description

BD9S402MUF-C is a synchronous buck DC/DC converter with built-in low ON resistor power MOSFETs. It can provide current up to 4 A. Small inductor is applicable due to high switching frequency of 2.2 MHz. It has fast transient response performance due to current mode control. It has a built-in phase compensation circuit. Applications can be created with a few external components.

Features

- QuiCur™
- Nano Pulse Control™
- AEC-Q100 Qualified *(Note 1)*
- Functional Safety Supportive Automotive Products
- Single Synchronous Buck DC/DC Converter
- Adjustable Soft Start Function
- Output Discharge Function
- Power Good Output
- Under Voltage Lockout Protection (UVLO)
- Short Circuit Protection (SCP)
- Output Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- Wettable Flank QFN Package

(Note 1) Grade 1

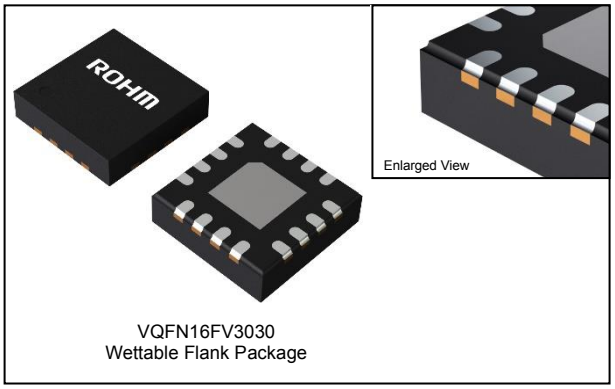
Applications

- Automotive Equipment
- Other Electronic Equipment

Key Specifications

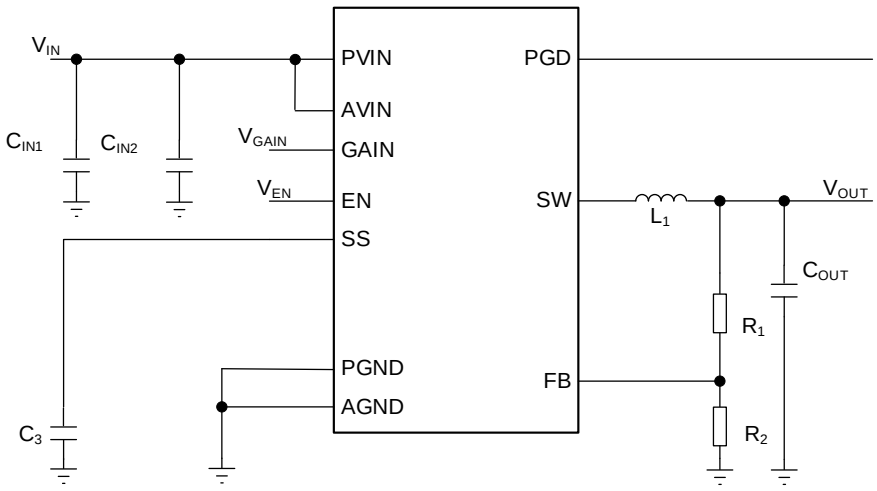
- Input Voltage: 2.7 V to 5.5 V
- Output Voltage Setting: 0.6 V to V_{PVIN} x 0.75 V
- Output Current: 4 A (Max)
- Switching Frequency: 2.2 MHz (Typ)
- High Side FET ON Resistance: 60 mΩ (Typ)
- Low Side FET ON Resistance: 35 mΩ (Typ)
- Shutdown Circuit Current: 0 μA (Typ)
- Operating Temperature: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN16FV3030	3.0 mm x 3.0 mm x 1.0 mm



VQFN16FV3030
Wettable Flank Package

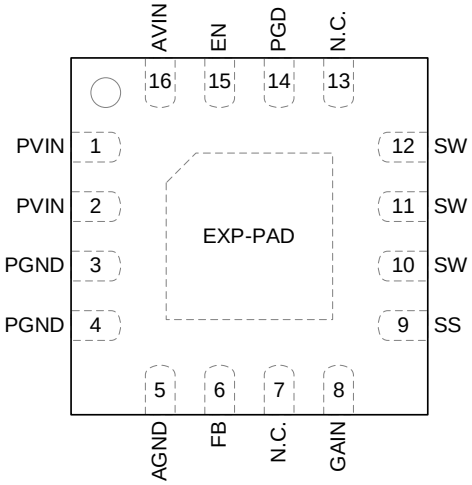
Typical Application Circuit



Contents

Pin Configuration

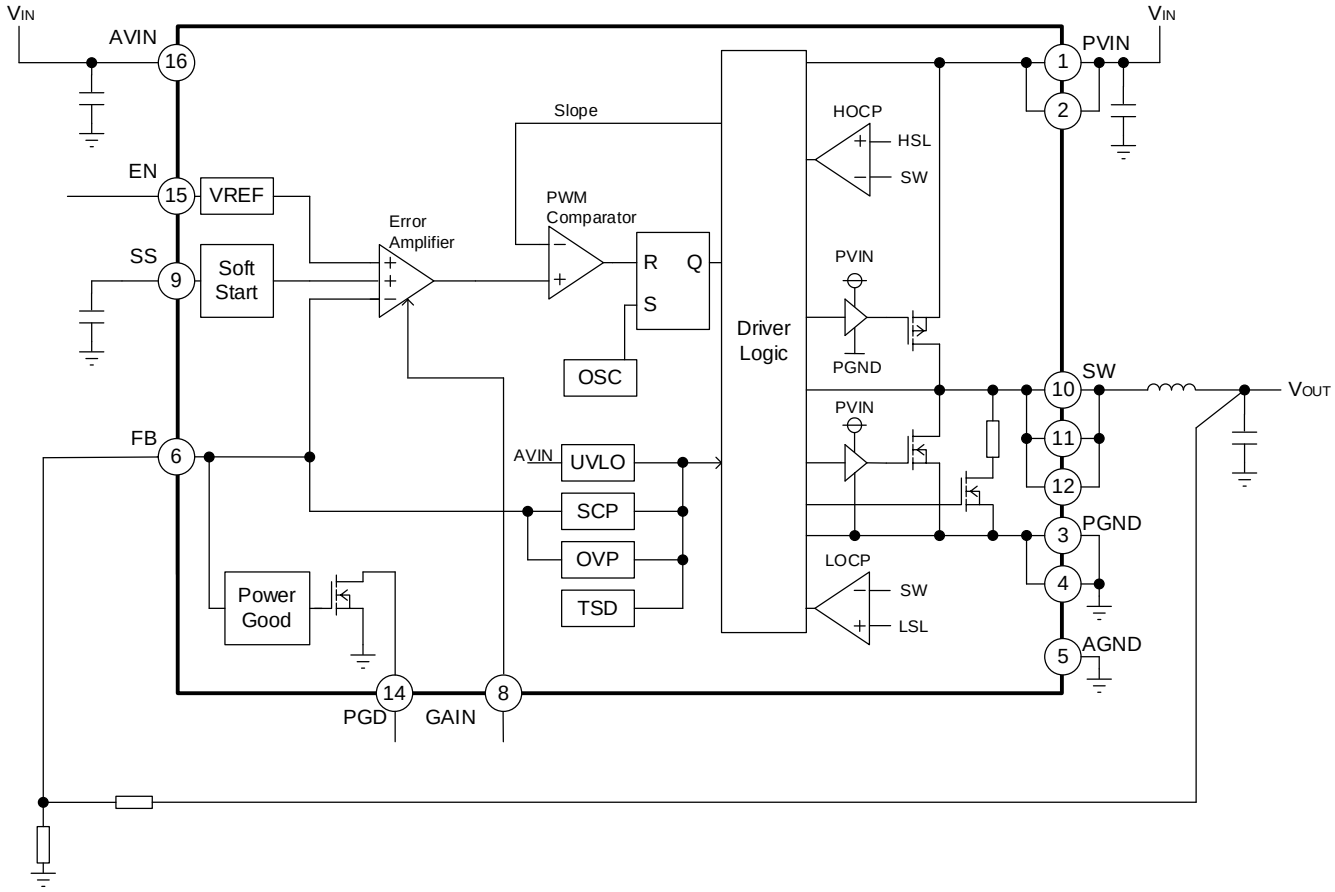
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply input pins that are used for the output stage of the switching regulator. Connect a ceramic capacitor of 10 µF as a recommended value. For details, see Selection of Components Externally Connected 4. Selection of Input Capacitor.
3, 4	PGND	Ground pins for the output stage of the switching regulator.
5	AGND	Ground pin.
6	FB	V_{OUT} feedback pin. Connect output voltage divider to this pin to set the output voltage. For the output voltage setting method, see Selection of Components Externally Connected 3. Output Voltage Setting.
7	N.C.	This pin is not connected to the chip. Use this as open. If this pin is used other than open and adjacent pins are expected to be shorted, confirm if there is any problem with the actual application.
8	GAIN	This pin switches the gain of the internal error amplifier of the device. When this pin is set to High, the device is in the fast load response mode, and when it is set to Low or open, the device is in the low output capacitance mode. For details, see Function Explanations 6. Error Amplifier Gain Switching Function.
9	SS	Pin for setting the Soft Start Time. The rise time of the output voltage can be set by connecting a capacitor to this pin. See Selection of Components Externally Connected 6. Selection of Soft Start Capacitor for how to set the capacitance value.
10, 11, 12	SW	Switch pin. These pins are connected to the drain of the High Side FET and the Low Side FET.
13	N.C.	This pin is not connected to the chip. Use this as open. If this pin is used other than open and adjacent pins are expected to be shorted, confirm if there is any problem with the actual application.
14	PGD	Power Good pin, an open drain output. It is needs to be pulled up to the power supply with a resistor. See Function Explanations 3. Power Good Function for setting the resistance.
15	EN	Device enable pin. Turning this pin Low forces, the device to enter the shutdown mode. Turning this pin High makes the device to start up.
16	AVIN	Power supply input pin for internal circuit. This pin is shorted to the PVIN pin. Connect a ceramic capacitor of 4700 pF as a recommended value.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

Block Diagram



Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. UVLO (Under Voltage Lock Out)
   The UVLO block is for under voltage lockout protection. It shuts down the device when the V_{AVIN} falls to 2.45 V (Typ) or lower. The threshold voltage has a hysteresis of 100 mV (Typ).

3. SCP (Short Circuit Protection)
   This is the short circuit protection circuit. After Soft Start is judged to be completed, if the FB pin voltage falls to 0.42 V (Typ) or less and remain in that state for 1 ms (Typ), output MOSFETs turn OFF for 14 ms (Typ) and then restart the operation.

4. OVP (Over Voltage Protection)
   This is the output over voltage protection circuit. When the FB pin voltage becomes V_{FB} +8 % (Typ) or more, it turns the output MOSFETs OFF. After output voltage falls V_{FB} +6 % (Typ) or less, the output MOSFETs return to normal operation.

5. TSD (Thermal Shutdown)
   This is the thermal shutdown circuit. It shuts down the device when the junction temperature (Tj) reaches to 175 °C (Typ) or more. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation with hysteresis of 25 °C (Typ).

6. HOCP (High Side Over Current Protection)
   This block detects the current flowing through the High Side FET and limits the current flowing at each cycle of switching frequency.

7. LOCP (Low Side Over Current Protection)
   This block detects the current flowing through the Low Side FET and limits the current flowing at each cycle of switching frequency.

8. Soft Start
   The Soft Start circuit slows down the rise of output voltage during startup, which allows the prevention of output voltage overshoot. The Soft Start Time can be specified by connecting a capacitor to the SS pin. See Selection of Components Externally Connected 6. Selection of Soft Start Capacitor for how to calculate the capacitance. A built-in Soft Start function is provided, and a Soft Start is initiated in t_{SS} (Electrical Characteristics) when the SS pin is open.

9. Error Amplifier
   This block is an error amplifier with a reference voltage of 0.6 V (Typ) and FB pin voltage as inputs, and the gain setting can be switched between High and Low on the GAIN pin.

10. PWM Comparator
    The PWM Comparator block compares the output voltage of the Error Amplifier and the Slope signal to determine the output switching pulse duty.

11. OSC (Oscillator)
    This block generates the oscillating frequency.

12. Driver Logic
    This block controls switching operation and various protection functions.

13. Power Good
    When the FB pin voltage reaches V_{FB} (0.6 V, Typ) within +6 % to -2 %, the built-in Nch MOSFET turns OFF and the PGD output turns High. There is a 2 % hysteresis on the threshold voltage, so the PGD output turns Low when the FB pin voltage reaches outside +8 % to -4 % of V_{FB}.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{PVIN}, V_{AVIN}	-0.3 to +7.0	V
EN Voltage	V_{EN}	-0.3 to V_{AVIN}	V
GAIN Voltage	V_{GAIN}	-0.3 to V_{AVIN}	V
PGD Voltage	V_{PGD}	-0.3 to +7.0	V
FB, SS Voltage	V_{FB}, V_{SS}	-0.3 to V_{AVIN}	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN16FV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23.0	10.0	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{PVIN}, V_{AVIN}	2.7	5.5	V
Operating Temperature	Ta	-40	+125	°C
Output Current	I_{OUT}	-	4	A
Output Voltage Setting	V_{OUT}	0.6*(Note 1)*	V_{PVIN} x 0.75	V
SW Minimum ON Time	t_{ONMIN}	-	50	ns

(Note 1) Although the output voltage is configurable at 0.6 V or more, it may be limited by the SW minimum ON pulse width. For the configurable range, refer to the Output Voltage Setting in Selection of Components Externally Connected.

Electrical Characteristics

(Unless otherwise specified Ta = Tj = -40 °C to +125 °C, V_{AVIN} = V_{PVIN} = 5.0 V, V_{EN} = 5.0 V, Typical value is Tj = +25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN						
Shutdown Circuit Current	I_{SDN}	-	0	10	µA	V_{EN} = 0 V, Tj = 25 °C
Circuit Current	I_{CC}	0.90	1.80	2.70	mA	V_{GAIN} = 0 V, I_{OUT} = 0 mA Non-switching, Tj = 25 °C
UVLO Detection Voltage	V_{UVLO1}	2.30	2.45	2.60	V	V_{AVIN} Falling
UVLO Release Voltage	V_{UVLO2}	2.40	2.55	2.70	V	V_{AVIN} Rising
UVLO Hysteresis Voltage	$V_{UVLO-HYS}$	50	100	125	mV	
ENABLE						
EN Input Voltage High	V_{ENH}	1.0	-	V_{AVN}	V	
EN Input Voltage Low	V_{ENL}	GND	-	0.4	V	
EN Input Current	I_{EN}	2	4	6	µA	V_{EN} = 5 V, Tj = 25 °C
GAIN						
GAIN Input Voltage High	V_{GAINH}	V_{AVIN} - 1.0	-	V_{AVIN}	V	
GAIN Input Voltage Low	V_{GAINL}	GND	-	0.8	V	
GAIN Input Current	I_{GAIN}	6	11	16	µA	V_{GAIN} = 5 V, Tj = 25 °C
Reference Voltage						
FB Pin Voltage	V_{FB}	0.594	0.600	0.606	V	
FB Input Current	I_{FB}	-	0	0.1	µA	V_{FB} = 0.6 V
Soft Start						
EN Waiting Time	t_{WAIT}	100	230	400	µs	
Soft Start Time	t_{SS}	0.75	1.00	1.25	ms	SS Pin OPEN
SS Charge Current	I_{SS}	-1.4	-1.0	-0.6	µA	
Switching Frequency						
Switching Frequency	f_{SW}	2.0	2.2	2.4	MHz	
Power Good						
PGD Falling (Fault) Voltage	V_{PGDTH_FF}	V_{FB} x 0.94	V_{FB} x 0.96	V_{FB} x 0.97	V	V_{FB} Falling
PGD Rising (Good) Voltage	V_{PGDTH_RG}	V_{FB} x 0.96	V_{FB} x 0.98	V_{FB} x 0.99	V	V_{FB} Rising
PGD Rising (Fault) Voltage	V_{PGDTH_RF}	V_{FB} x 1.06	V_{FB} x 1.08	V_{FB} x 1.09	V	V_{FB} Rising
PGD Falling (Good) Voltage	V_{PGDTH_FG}	V_{FB} x 1.04	V_{FB} x 1.06	V_{FB} x 1.07	V	V_{FB} Falling
PGD Falling (Fault) Detection delay time	$t_{PGDELFF}$	60	105	150	µs	
PGD Rising (Fault) Detection delay time	$t_{PGDELRF}$	60	105	150	µs	
PGD Output Leakage Current	$I_{LEAKPGD}$	-	0	1	µA	V_{PGD} = 5 V, Tj = 25 °C
PGD FET ON Resistance	R_{PGD}	20	50	80	Ω	
PGD Output Low Level Voltage	V_{PGDL}	0.02	0.05	0.12	V	I_{PGD} = 1 mA
Switch MOSFET						
High Side FET ON Resistance	R_{ONH}	30	60	100	mΩ	V_{PVIN} = 5 V
		35	70	110	mΩ	V_{PVIN} = 3.3 V
Low Side FET ON Resistance	R_{ONL}	20	35	60	mΩ	V_{PVIN} = 5 V
		23	38	63	mΩ	V_{PVIN} = 3.3 V
High Side FET Leakage Current	$I_{LEAKSWH}$	-	0	5	µA	V_{PVIN} = 5.5 V, V_{SW} = 0 V Tj = 25° C
Low Side FET Leakage Current	$I_{LEAKSWL}$	-	0	5	µA	V_{PVIN} = 5.5 V, V_{SW} = 5.5 V Tj = 25 °C
High Side FET Current Limit *(Note 1)*	I_{OCPH}	4.6	6.4	8.2	A	
Low Side FET Current Limit *(Note 1)*	I_{OCPL}	4.0	5.4	7.0	A	
SW Discharge Resistance	R_{DIS}	30	60	100	Ω	V_{EN} = 0 V, Vsw = 3.3 V

(Note 1) This is design value. Not production tested.

Electrical Characteristics – continued

(Unless otherwise specified Ta = Tj = -40 °C to +125 °C, V_{AVIN} = V_{PVIN} = 5.0 V, V_{EN} = 5.0 V, Typical value is Tj = +25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCP, OVP						
Short Circuit Protection Detection Voltage	V_{SCP}	0.34	0.42	0.50	V	V_{FB} Falling
Output Over Voltage Protection Detection Voltage	V_{OVP}	V_{FB} x 1.06	V_{FB} x 1.08	V_{FB} x 1.09	V	V_{FB} Rising

Typical Performance Curves (Reference Data)

Unless otherwise specified $V_{IN} = V_{EN}$

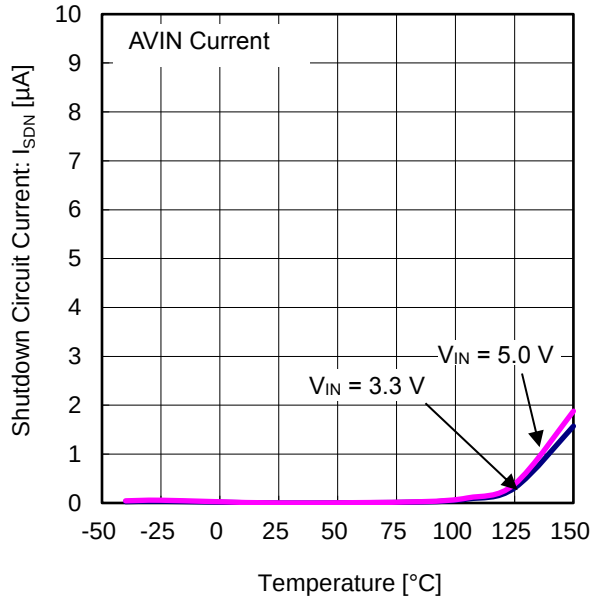


Figure 1. Shutdown Circuit Current vs Temperature

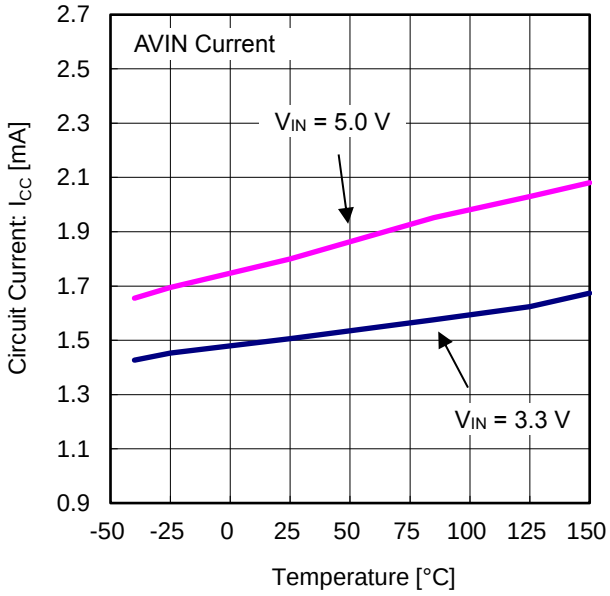


Figure 2. Circuit Current vs Temperature

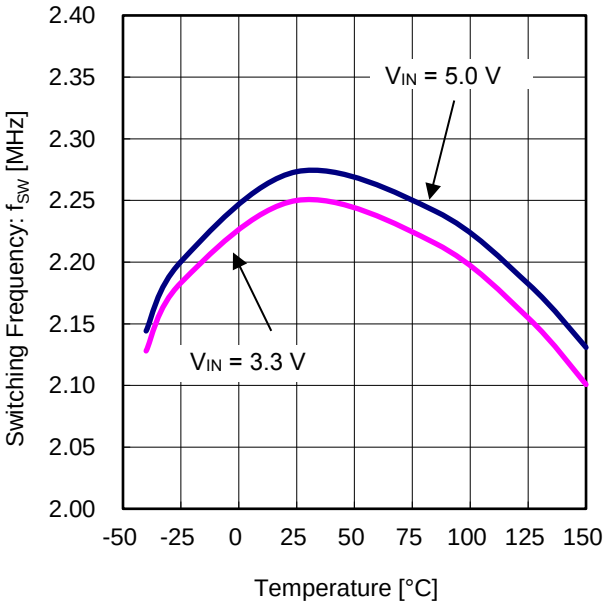


Figure 3. Switching Frequency vs Temperature

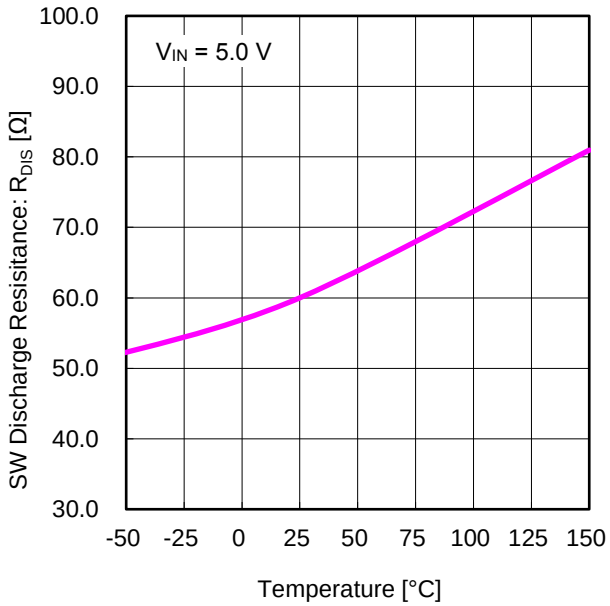


Figure 4. SW Discharge Resistance vs Temperature

Typical Performance Curves (Reference Data) – continued

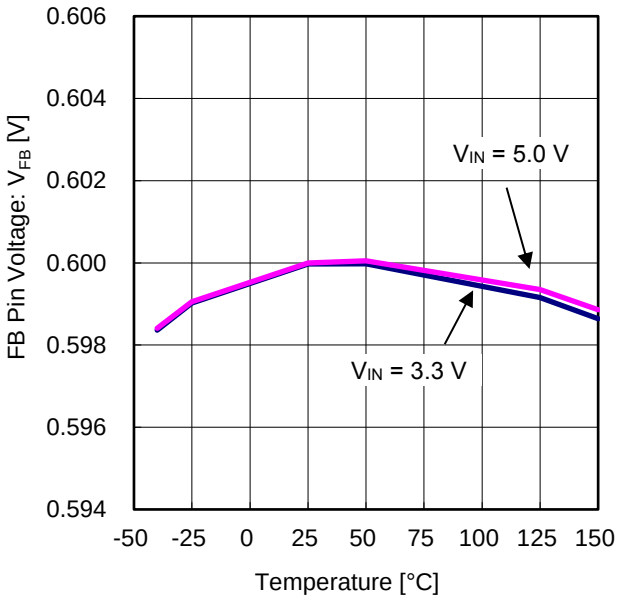


Figure 5. FB Pin Voltage vs Temperature

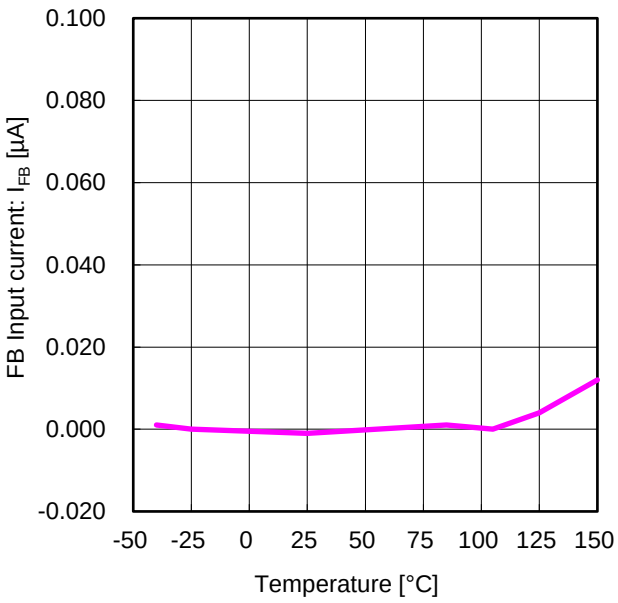


Figure 6. FB Input Current vs Temperature

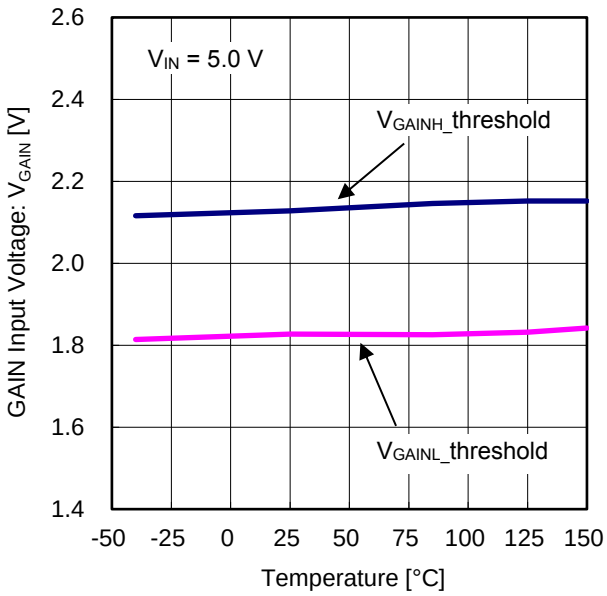


Figure 7. GAIN Input Voltage vs Temperature

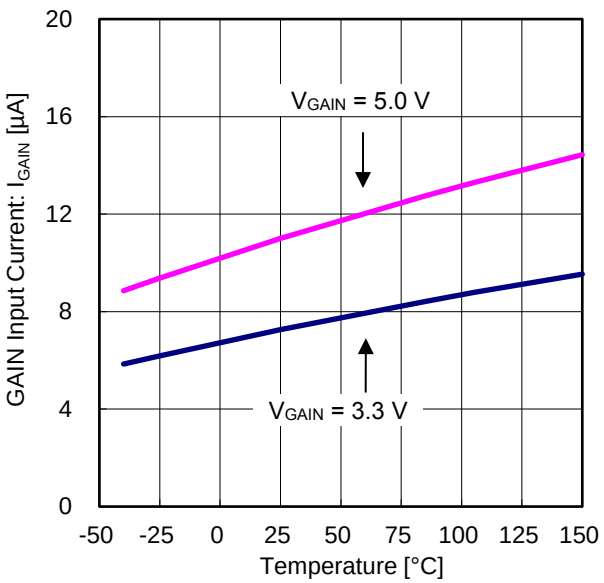


Figure 8. GAIN Input Current vs Temperature

Typical Performance Curves (Reference Data) – continued

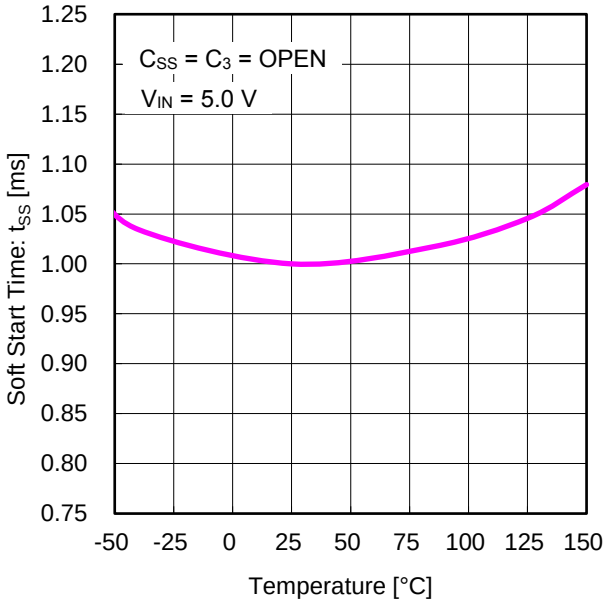


Figure 9. Soft Start Time vs Temperature

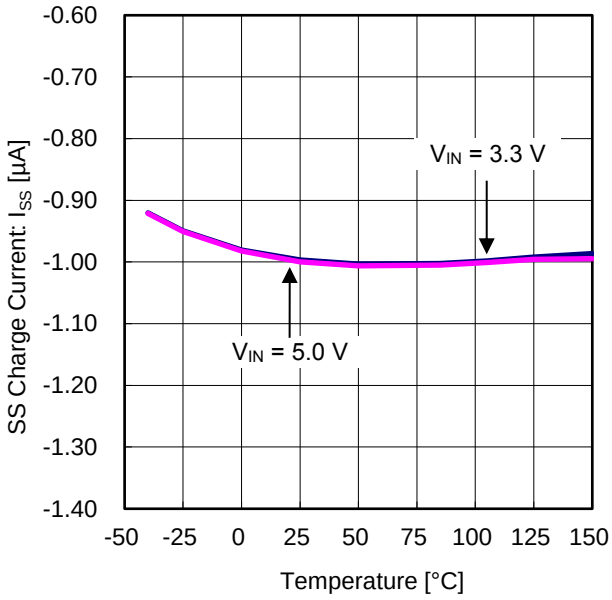


Figure 10. SS Charge Current vs Temperature

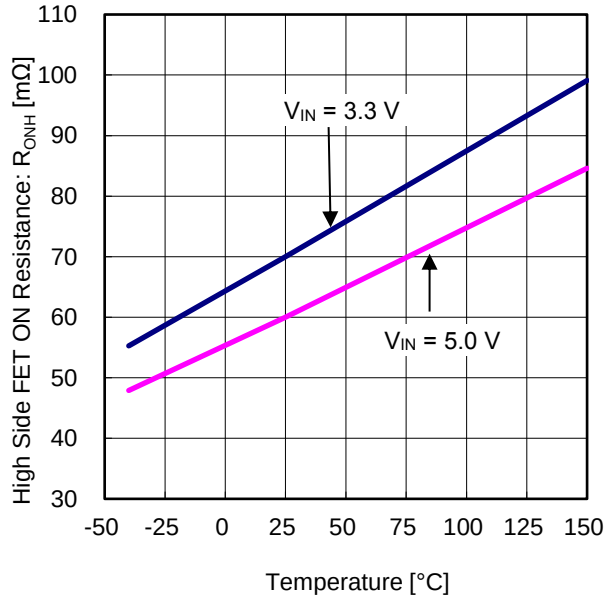


Figure 11. High Side FET ON Resistance vs Temperature

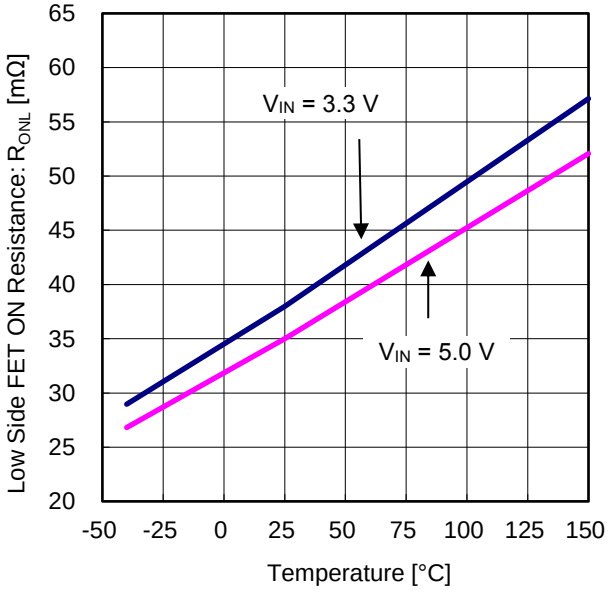


Figure 12. Low Side FET ON Resistance vs Temperature

Typical Performance Curves (Reference Data) – continued

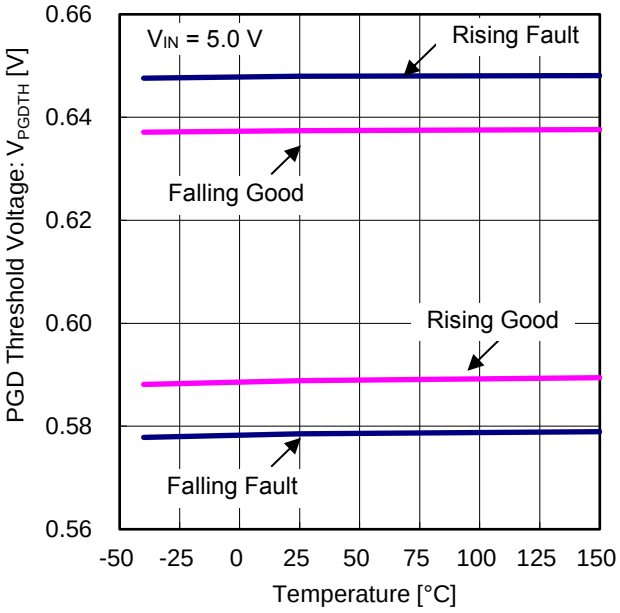


Figure 13. PGD Threshold Voltage vs Temperature

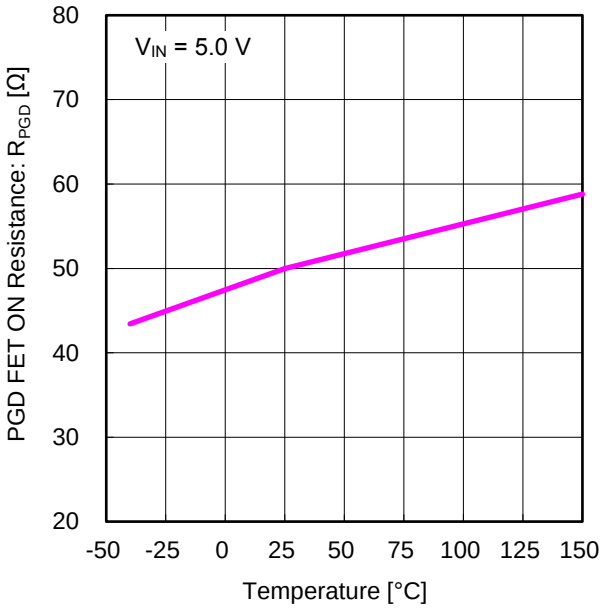


Figure 14. PGD FET ON Resistance vs Temperature

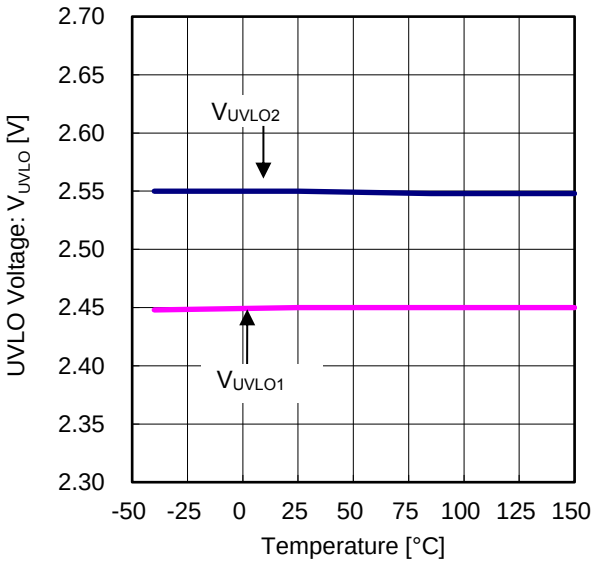


Figure 15. UVLO Voltage vs Temperature

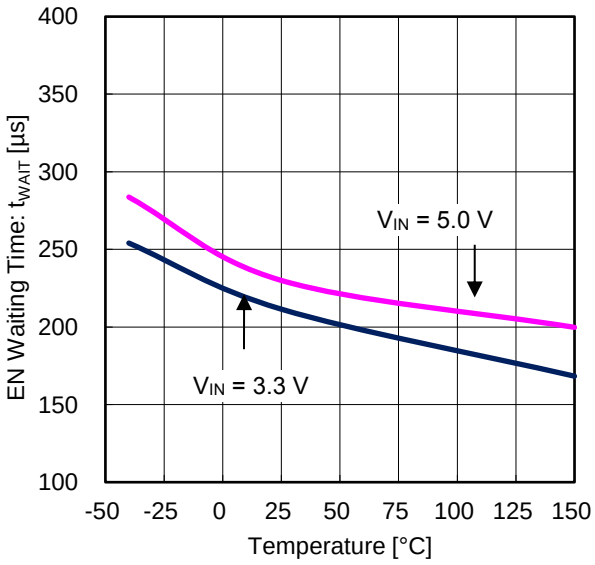


Figure 16. EN Waiting Time vs Temperature

Typical Performance Curves (Reference Data) – continued

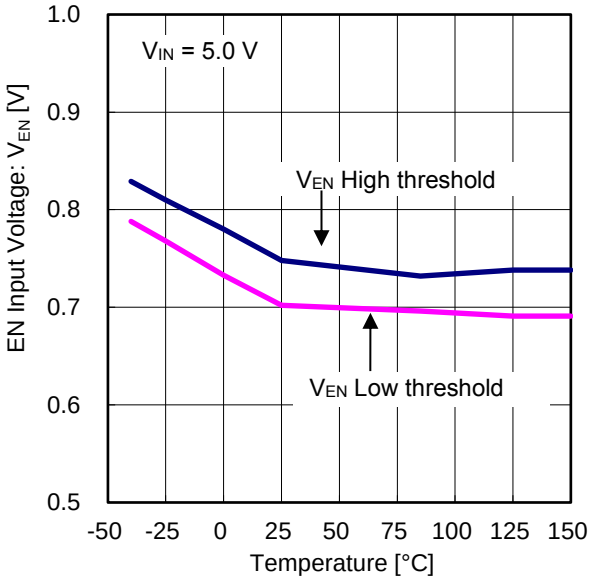


Figure 17. EN Input Voltage vs Temperature

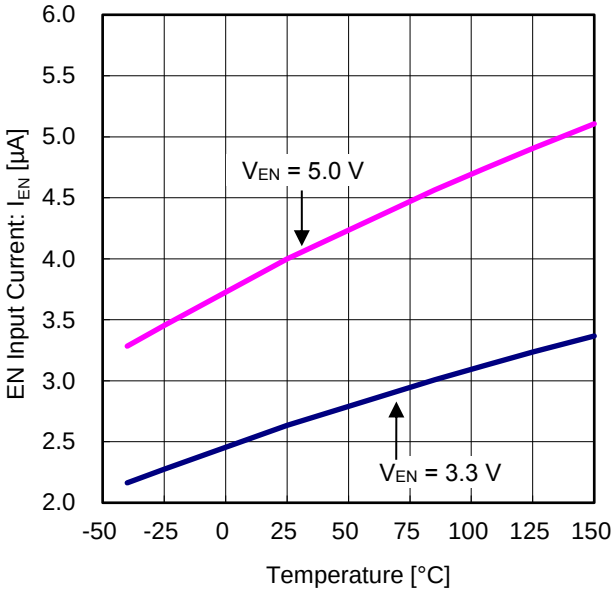


Figure 18. EN Input Current vs Temperature

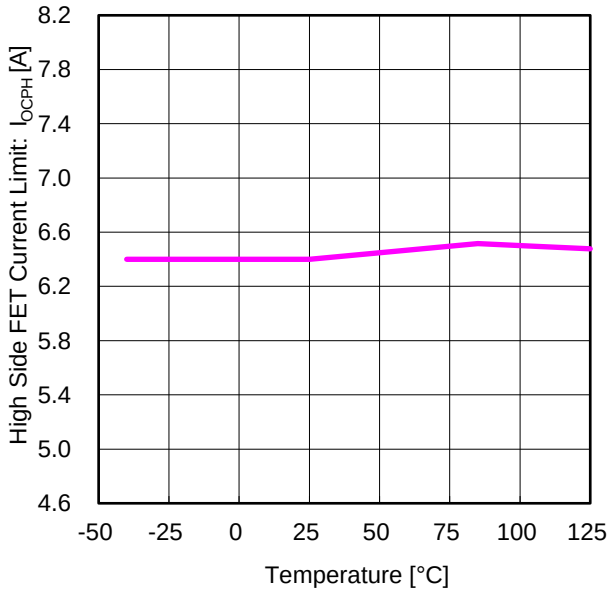


Figure 19. High Side FET Current Limit vs Temperature

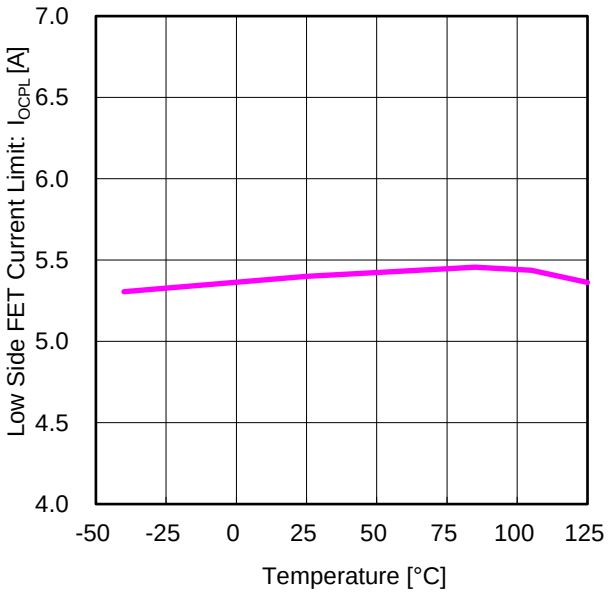


Figure 20. Low Side FET Current Limit vs Temperature

Typical Performance Curves (Reference Data) – continued

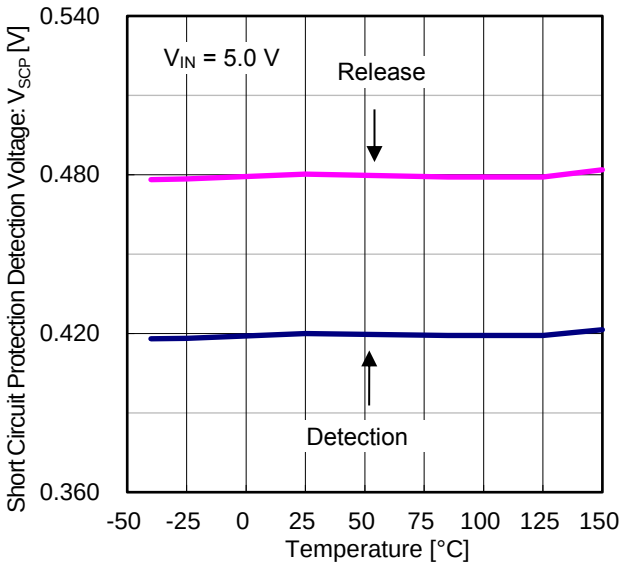


Figure 21. Short Circuit Protection Detection Voltage vs Temperature

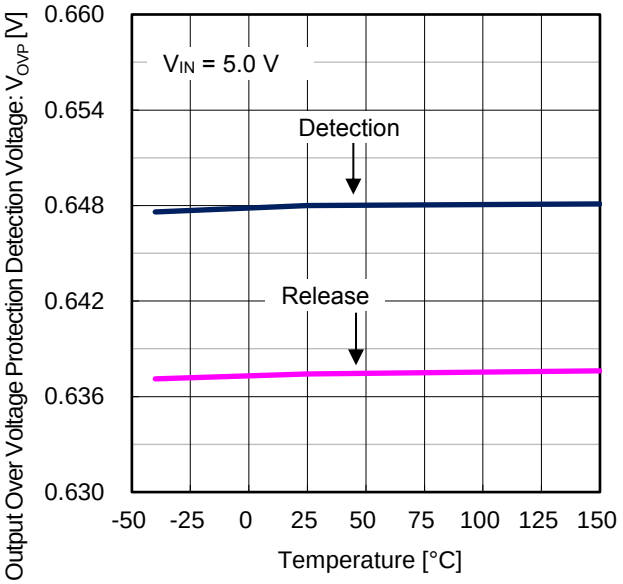


Figure 22. Output Over Voltage Protection Detection Voltage vs Temperature

Function Explanations

1. Enable Control

The device shutdown can be controlled by the voltage applied to the EN pin. When EN voltage V_{EN} becomes V_{ENH} (1.0 V) or more, the internal circuit is activated, and the device starts up with Soft Start.
The delay time t_{WAIT} (230 µs, Typ) is implemented from the EN pin becoming High to V_{OUT} starting up. When the SS pin is open, the device starts with the built-in Soft Start Time t_{SS} (1.0 ms, Typ). When V_{EN} becomes V_{ENL} (0.4 V) or less, the device is shutdown. During shutdown, the SW pin is pulled down with resistance R_{DIS} (60 Ω, Typ) to discharge the output voltage.

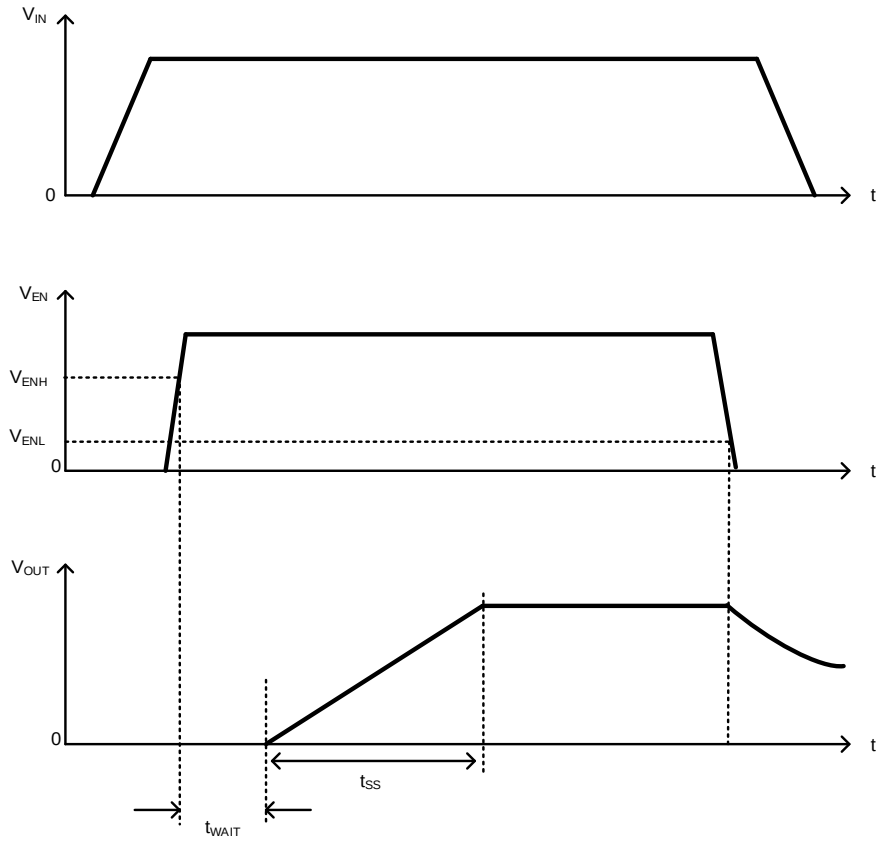


Figure 23. Enable ON/OFF Timing Chart

2. Nano Pulse Control™

Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition. Narrow SW ON Pulse enables direct convert of high input voltage to low output voltage. The output voltage V_{OUT} = 0.8 V or less can be output directly from the supply voltage V_{IN} = 5.0 V at 2.2 MHz.

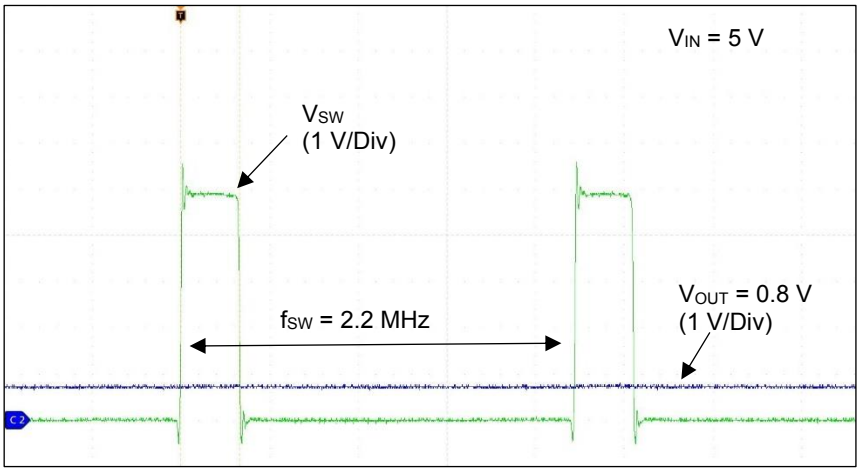


Figure 24. Switching Waveform (V_{IN} = 5.0 V, V_{OUT} = 0.8 V, I_{OUT} = 1.0 A, f_{SW} = 2.2 MHz)

Function Explanations – continued

3. Power Good Function

When the FB pin voltage becomes 0.6 V (Typ) within -2 %, the open drain output MOSFET of the PGD pin turns OFF and the PGD pin output becomes High by the pull-up resistor. When the FB pin voltage is out of 0.6 V (Typ) -4 % and the condition continues for $t_{PGDELFF}$ (105 µs, Typ), the PGD pin open drain MOSFET turns ON and the PGD pin is pulled down with an impedance of 60 Ω (Typ).When the FB pin voltage is out of 0.6 V (Typ) -4 % and the time until the voltage returns to within -2 % is shorter than $t_{PGDELFF}$, the PGD state is maintained High.
The Power Good Function also operates when output overvoltage is detected. If the FB pin voltage is outside the range of 0.6 V (Typ) +8 % and the condition continues for $t_{PGDELRF}$ (105 µs, Typ) time, the open drain output MOSFET of the PGD pin turns ON and the PGD pin is pulled down with an impedance of 60 Ω (Typ). When the FB pin voltage becomes within 0.6 V (Typ) +6 %, the open drain output MOSFET of the PGD pin turns OFF and the output becomes High. It is recommended that the PGD pin be pulled up to the power supply with a resistor from 2 kΩ to 100 kΩ or less.
If the power good function is not used, connect the PGD pin to OPEN or GND.
During shutdown, the PGD pin is pulled down if V_{AVIN} is 1.2 V or more.

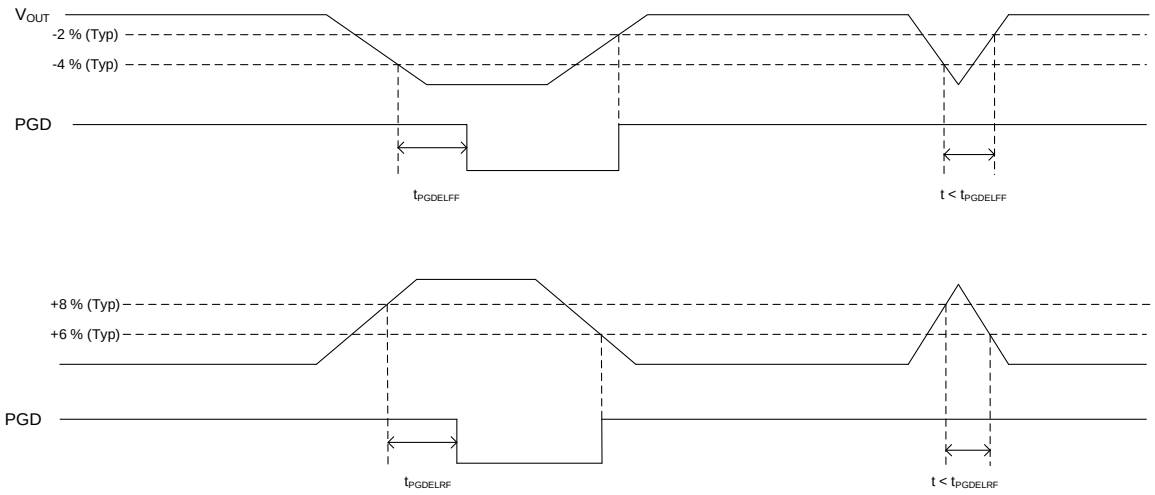


Figure 25. Power Good Timing Chart

4. Output Discharge Function

When even one of the following conditions is satisfied, output is discharged with 50 Ω (Typ) resistance through the SW pin.

- V_{EN} becomes 0.4 V or less
- V_{IN} becomes 2.45 V (Typ) or less (UVLO)
- V_{FB} becomes 0.42 V (Typ) or less and remains there for 1 ms (Typ) (SCP)
- V_{FB} becomes 0.6 V (Typ) +8 % or more (OVP)
- Tj becomes 175 °C (Typ) or more (TSD)

When all the above conditions are released, output discharge is stopped.

5. QuiCur™

QuiCur™ is a combination of technologies that provides high-speed load response.
This technology reduces the amount of output voltage change in response to transient changes in load current.
It also reduces the capacitance of output capacitors required for power supply ICs, thereby reducing the number of components and the board mounting area.

6. Error Amplifier Gain Switching Function

The gain of the error amplifier in the device can be switched by the GAIN pin; connecting the GAIN pin to the AVIN pin sets the device in the fast load response mode, in which the error amplifier gain is set high, to suppress output voltage changes during load transients. At this time, connect an output capacitor C_{OUT} of 44 µF (Typ) or more.
When the GAIN pin is connected to the AGND pin or left open, the error amplifier gain is set to low, and the mode becomes the low output capacitance mode that operates stably even when C_{OUT} is 22 µF (Typ). However, the output voltage change during load transients will be larger than in the fast load response mode. Do not switch the GAIN pin connection during operation.

Protection Function

1. Short Circuit Protection (SCP)

The Short Circuit Protection block compares the FB pin voltage with the internal reference voltage V_{REF}. When the FB pin voltage has fallen to 0.42 V (Typ) or less and remained there for 1 ms (Typ), SCP stops the operation for 14 ms (Typ) and subsequently initiates a restart. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

EN Pin	FB Pin	Short Circuit Protection	Short Circuit Protection Operation
1.0 V or more	≤ 0.42 V (Typ)	Enabled	ON
	≥ 0.48 V (Typ)		OFF
0.4 V or less	-	Disabled	OFF

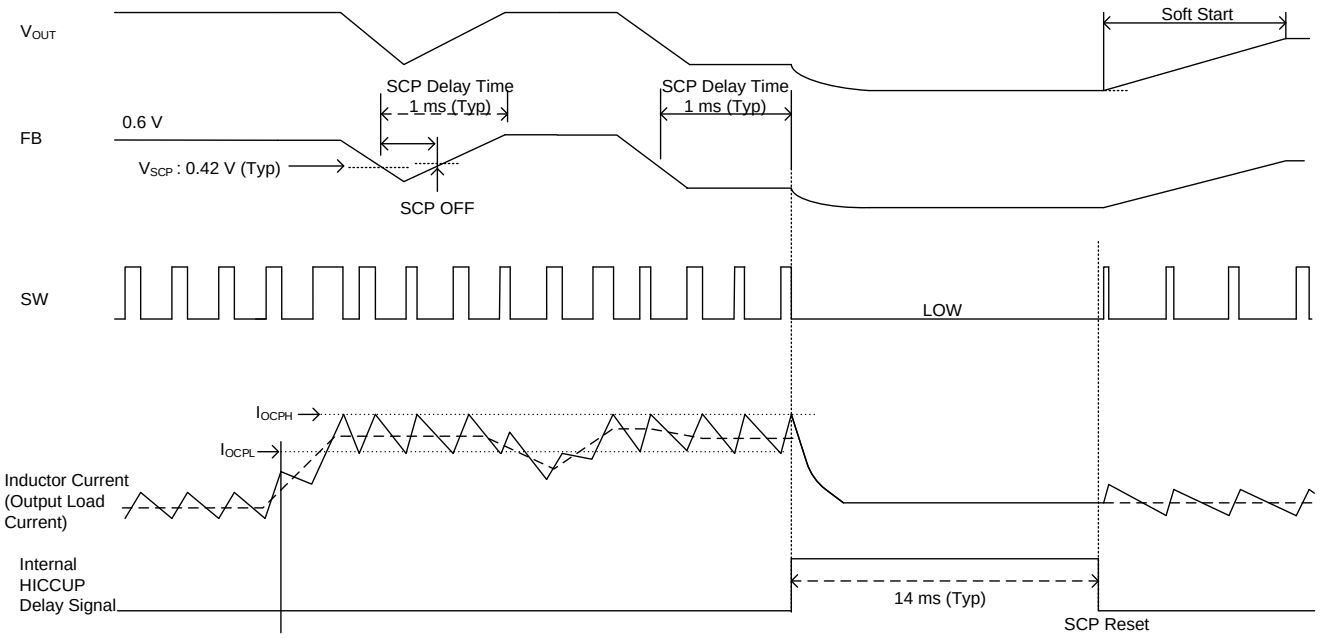


Figure 26. Short Circuit Protection (SCP) Timing Chart

2. Over Current Protection (OCP)

The Over Current Protection function limits the current flowing to the High Side FET and Low Side FET. When the current flowing to the High Side FET reaches I_{OCPH}, the High Side FET is turned OFF and the peak current limit is applied. Next, when the Low Side FET is turned ON, the current flowing to the Low Side FET is monitored and if it is larger than I_{OCPL}, the turn-on operation is skipped due to the current limit of the Low Side FET.

As the Low Side FET ON state continues, the inductor current decreases, and when it becomes I_{OCPL} or less, the current limit is released, and SW turns ON by the next set signal inside the device. This series of operations provides over current protection. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

Protection Function – continued

3. Under Voltage Lock Out Protection (UVLO)

It shuts down the device when the AVIN pin voltage falls to 2.45 V (Typ) or less.
The threshold voltage has a hysteresis of 100 mV (Typ).

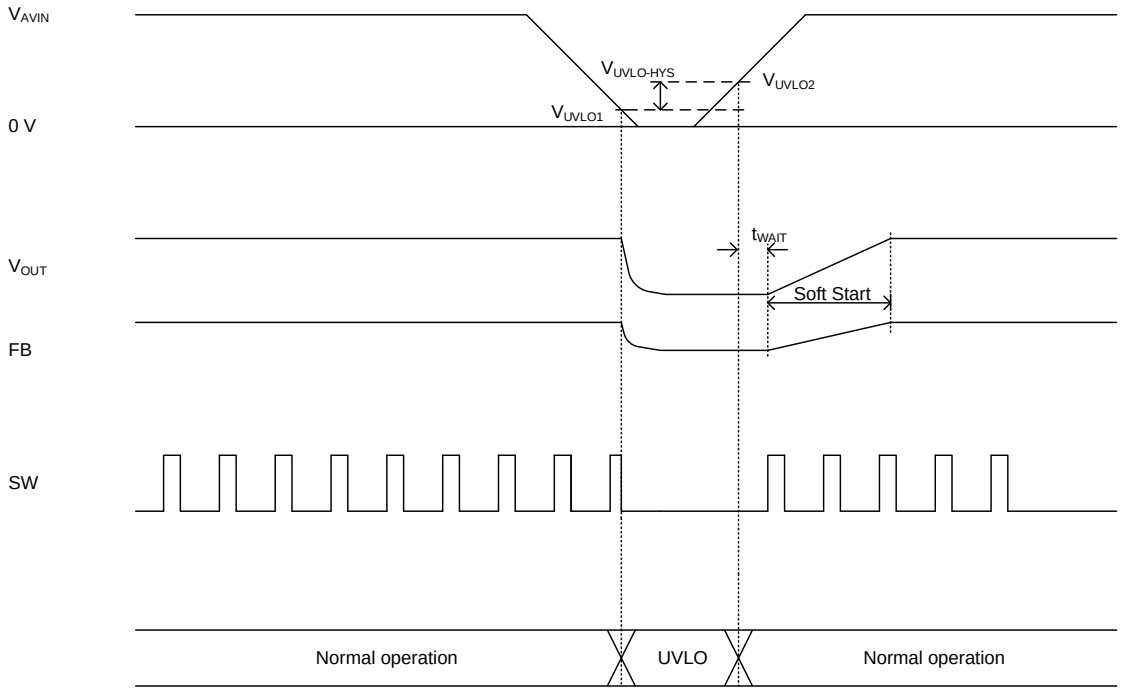


Figure 27. Under Voltage Lock Out Protection (UVLO) Timing Chart

4. Thermal Shutdown (TSD)

This is the thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. However, if the rating is exceeded for a continued period and the junction temperature (Tj) rises to 175 °C (Typ), the TSD circuit activates and the output MOSFETs turn OFF. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

5. Over Voltage Protection (OVP)

The device incorporates an over voltage protection circuit to minimize the output voltage overshoot when recovering from fast load transients or output fault conditions. If the FB pin voltage becomes Output Over Voltage Protection Detection Voltage V_{FB} + 8% or more, the MOSFETs on the output stage are turned OFF to prevent the increase in the output voltage. After detection, switching operation is resumed if the output decreases, the over voltage state is released. Output Over Voltage Protection Detection Voltage and Release Voltage have a hysteresis of 2 %.

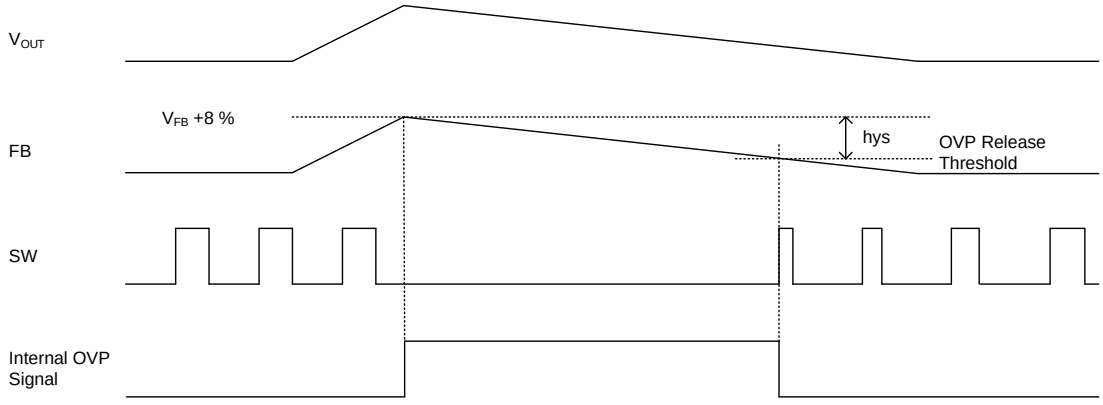


Figure 28. Over Voltage Protection (OVP) Timing Chart

Selection of Components Externally Connected

Necessary parameters in designing the power supply are as follows:

Table 1. Application Specification

Parameter	Symbol	Example Value
Input Voltage	V_{IN}	5.0 V
Output Voltage	V_{OUT}	1.2 V
Switching Frequency	f_{SW}	2.2 MHz (Typ)
Output Capacitor	C_{OUT}	44 µF
Soft Start setting time	t_{SS_EXT}	6.0 ms (Typ)
Maximum Output Current	I_{OUTMAX}	4 A

1. Application Example

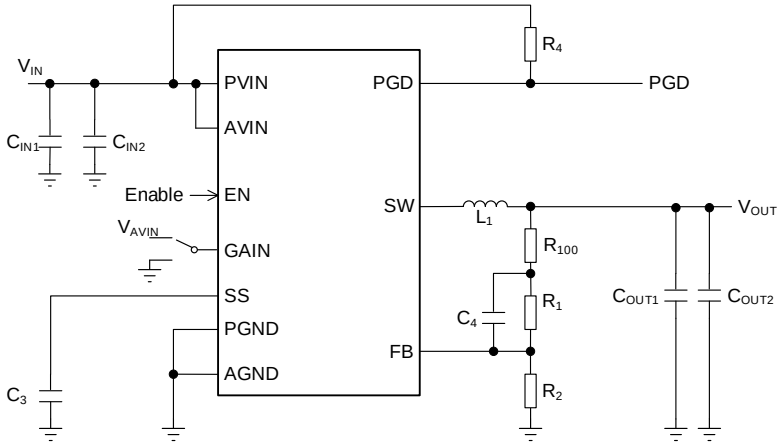


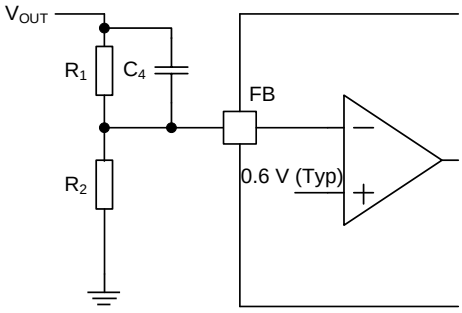
Figure 29. Application Circuit

2. Switching Frequency

The switching frequency f_{SW} is fixed at 2.2 MHz (Typ) inside the IC.

3. Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio. It is recommended to use the resistor values shown in Table 2 for each output voltage setting.



$$V_{OUT} = \frac{R_1+R_2}{R_2} \times 0.6 \ \text{[V]}$$

※ SW Minimum ON Time that BD9S402MUF-C can output stably in the entire load range is 50 ns.
Use this value to calculate the input and output conditions that satisfy the following equation.

$$50 \ \text{[ns]} \leq \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Figure 30. Feedback Resistor Circuit

Table 2. Configuration Resistors and Capacitor

Output Voltage V_{OUT}	R_1	R_2	C_4
0.8 V	13 kΩ	39 kΩ	47 pF
0.9 V	15 kΩ	30 kΩ	47 pF
1.0 V	22 kΩ	33 kΩ	47 pF
1.2 V	47 kΩ	47 kΩ	47 pF
1.5 V	15 kΩ	10 kΩ	47 pF
1.8 V	30 kΩ	15 kΩ	33 pF
3.3 V	68 kΩ	15 kΩ	33 pF

Selection of Components Externally Connected – continued

4. Selection of Input Capacitor

The input capacitor requires a large capacitance value for C_{IN1} and a small capacitance value for C_{IN2}. Use ceramic capacitor for these capacitors. C_{IN1} is used to suppress the ripple noise, and C_{IN2} is used to suppress the switching noise. These ceramic capacitors are effective by being placed as close as possible to the PVIN pin and the AVIN pin. The capacitance value of C_{IN1} should be 4.7 µF or more. In addition, the voltage rating has to be more than twice the typical input voltage. Set the capacitance value so that it does not fall to its minimum required value against the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, etc. Use components which are comparatively same with the components used in "Application Characteristic Data (Reference Data)". A nominal 4700 pF is recommended for the C_{IN2} capacitance value. Moreover, factors like the PCB layout and the position of the capacitor may lead to IC malfunction. Refer to "PCB layout Design".

5. Selection of Output LC Filter

The inductor in the DC/DC converter supplies a continuous current to the load and functions as a filter to smooth the output voltage. When a large inductor is selected, the Inductor ripple current ΔI_L and the output ripple voltage ΔV_{P-P} are reduced. It is the trade-off between the size and the cost of the inductor. Select a nominal inductance value between 0.33 µH and 0.68 µH.

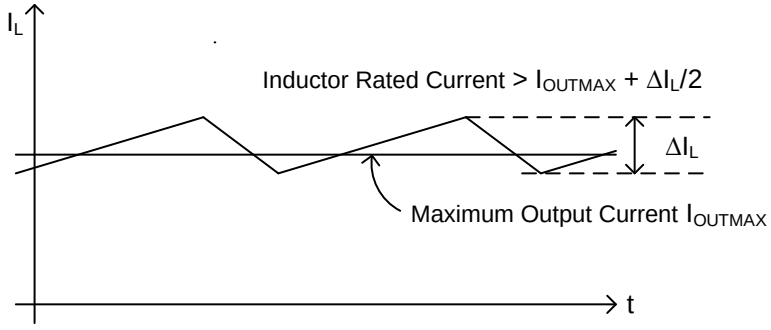


Figure 31. Waveform of Current through Inductor

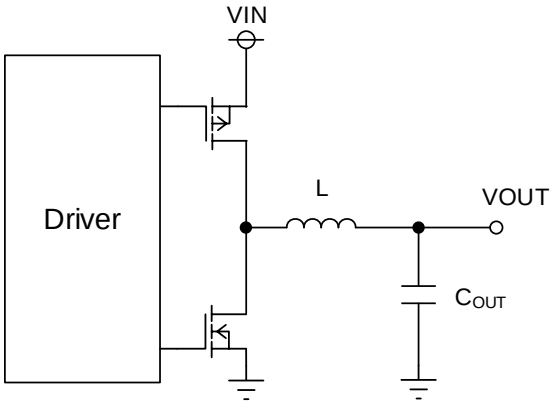


Figure 32. Output LC Filter Circuit

Inductor ripple current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 882 \text{ [mA]}$$

where

V_{IN}	is the 5.0 V
V_{OUT}	is the 1.2 V
L_1	is the 0.47 µH
f_{SW}	is the 2.2 MHz (Switching Frequency)

The rated current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L.

Table 3. List of Inductors

Manufacturer	Inductor Series	Inductance [µH]	DCR [mΩ]	I_{TEMP} [A]	W x L x H [mm]
TDK	SPM5030VT	0.33	4.2	14.2	5.1 x 5.3 x 3.0
TDK	SPM5030VT	0.47	5.4	12.9	5.1 x 5.3 x 3.0
TDK	SPM5030VT	0.68	7.4	10.7	5.1 x 5.3 x 3.0
TDK	TFM252012ALMA	0.33	13.0	7.8	2.5 x 2.0 x 1.2
TDK	TFM252012ALMA	0.47	19.0	6.5	2.5 x 2.0 x 1.2
Panasonic	ETQP3M	0.47	5.8	11.6	5.5 x 5.0 x 3.0
Panasonic	ETQP3M	0.68	7.6	10.2	5.5 x 5.0 x 3.0
Coilcraft	XGL4020	0.47	4.2	19.7	4.0 x 4.0 x 2.1

5. Selection of Output LC Filter – continued

The output capacitor C_{OUT} affects the output ripple voltage characteristics. C_{OUT} satisfy the required ripple voltage characteristics. The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

where

R_{ESR} is the Equivalent Series Resistance of the output capacitor.

$$\Delta V_{RPL} = 0.882 \times \left(10 \times 10^{-3} + \frac{1}{8 \times 44 \times 2.2} \right) = 9.96 \text{ [mV]}$$

where

C_{OUT} is the 44 µF

R_{ESR} is the 10 mΩ

Next, the required capacitance value of the output capacitor C_{OUT} varies depending on the GAIN pin setting. 44 µF (Typ) or more is recommended for C_{OUT} when the GAIN pin is set to High. When the GAIN pin is set Low or open, the device can operate in low output capacitance mode with a C_{OUT} of 22 µF (Typ) or more. In consideration of variation, temperature characteristics, DC bias characteristics, aging characteristics, etc., use components equivalent to those listed in Application Characteristics Data (Reference Data).

If the total value of all capacitors connected to V_{OUT} is large, the inrush current at startup may cause the over current protection to operate and the output may not start. In this case, set the Soft Start time to satisfy the following equation. See 6. Selection of Soft Start Capacitor for how to set the Soft Start time.

$$t_{SS\_EXT} > \frac{V_{OUT} \times C_{OUT(TOTAL)}}{(I_{OCPH(MIN)} - I_{SWSTART(MAX)})} \text{ [s]}$$

where:

t_{SS_EXT} is the Soft Start setting time [s]

$C_{OUT(TOTAL)}$ is the total value of all capacitors connected to V_{OUT} [F]

$I_{SWSTART(MAX)}$ is the maximum value of output load current expected at startup [A]

$I_{OCPH(MIN)}$ is the minimum value of OCP SW current 4.6 A (Min)

V_{OUT} is the output voltage [V]

In case of large changing input voltage and output current, select the capacitance accordingly by verifying that the actual application setup meets the required specification.

6. Selection of Soft Start Capacitor

Turning the EN pin High activates the Soft Start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time t_{SS_EXT} depends on the value of the capacitor connected to the SS pin. The capacitance value should be set in the range between 3300 pF and 0.1 µF.

$$t_{SS\_EXT} = \frac{(C_3 \times V_{FB})}{I_{SS}} \text{ [s]}$$

where

t_{SS_EXT} is the Soft Start setting time

C_3 is the Capacitor connected to the SS pin

V_{FB} is the FB pin Voltage 0.6 V (Typ)

I_{SS} is the SS Charge Current 1.0 µA (Typ)

With C_3 = 0.01 µF

$$t_{SS\_EXT} = \frac{(0.01 \times 0.6)}{1.0} = 6.0 \text{ [ms]}$$

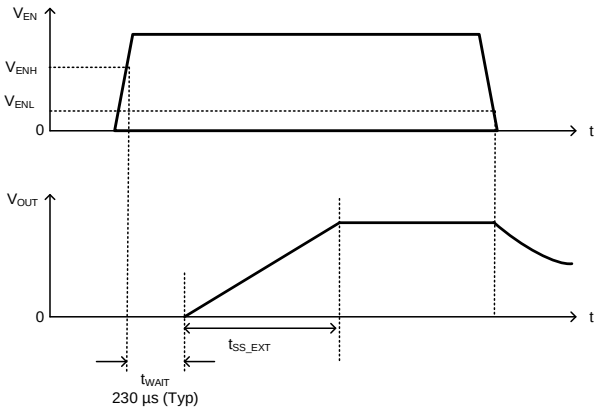


Figure 33. Soft Start Timing chart

Turning the EN pin High without connecting capacitor to the SS pin and keeping the SS pin either OPEN condition or 10 kΩ to 100 kΩ pull up condition to power source, the output rises in t_{SS} = 1.0 ms (Typ).

Selection of Components Externally Connected – continued

7. Input Voltage Startup

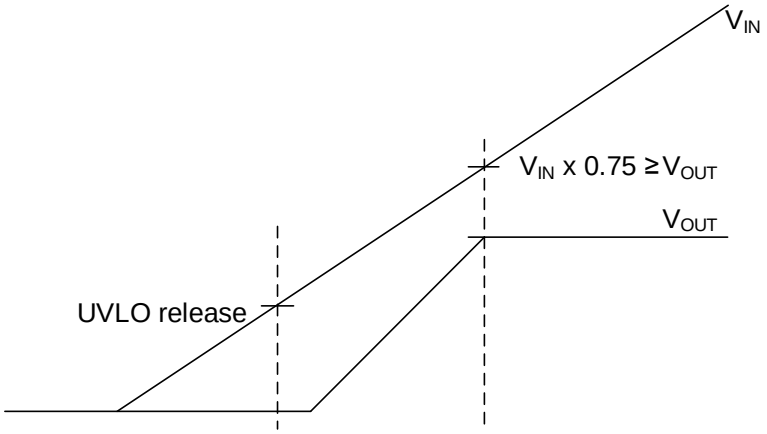


Figure 34. Input Voltage Startup Time

The Soft Start function starts up the device according to the specified Soft Start time. After UVLO is released, the voltage range that can be output during the Soft Start operation is 75 % or less of the input voltage. Note that the condition of input voltage and output voltage during the startup with Soft Start should satisfy the following expression.

$$V_{IN} \geq \frac{V_{OUT}}{0.75} \text{ [V]}$$

Application Characteristic Data (Reference Data)

Measurement Circuit

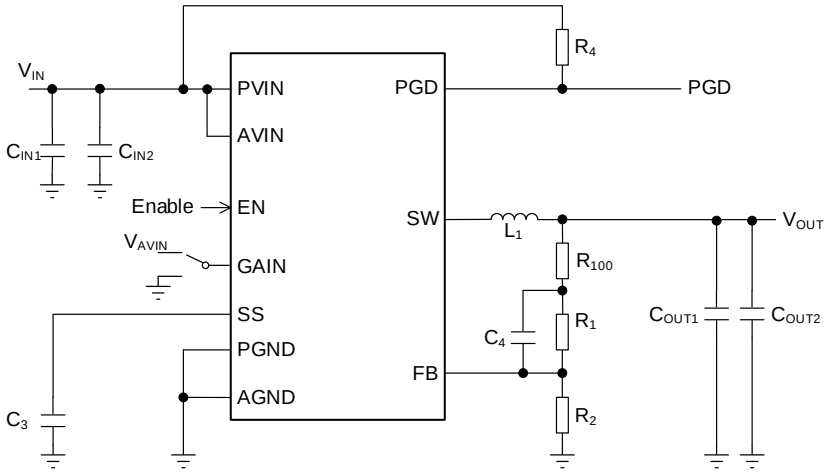


Figure 35. Measurement Schematic

Table 4. List of Components for the fast load response mode (Note 1) (GAIN = High)

NO	Package	Parameter	Part Name	Type	Manufacture
L_1	-	0.47 µH	SPM5030VT-R47M-D	Inductor	TDK
C_{OUT1}	3216	22 µF, X7R, 6.3 V	GCM31CR70J226KE26	Ceramic Capacitor	Murata
C_{OUT2}	3216	22 µF, X7R, 6.3 V	GCM31CR70J226KE26	Ceramic Capacitor	Murata
C_{IN1}	2012	10 µF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C_{IN2}	1005	4700 pF, X7R, 25 V	GCM155R71E472KA37	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	Depending on V_{OUT} (Note 2)	MCR01MZPF Series	Chip Resistor	ROHM
R_2	1005	Depending on V_{OUT} (Note 2)	MCR01MZPF Series	Chip Resistor	ROHM
R_4	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF Series	Chip Resistor	ROHM
C_3	OPEN	-	-	-	-
C_4	1005	Depending on V_{OUT} (Note 2)	GCM155R71E Series	Ceramic Capacitor	Murata
GAIN	-	High	-	-	-

Table 5. List of Components for the low output capacitance mode (Note 1) (GAIN = Low)

NO	Package	Parameter	Part Name	Type	Manufacture
L_1	-	0.47 µH	SPM5030VT-R47M-D	Inductor	TDK
C_{OUT1}	3216	22 µF, X7R, 6.3 V	GCM31CR70J226KE26	Ceramic Capacitor	Murata
C_{OUT2}	OPEN	-	-	-	-
C_{IN1}	2012	10 µF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C_{IN2}	1005	4700 pF, X7R, 25 V	GCM155R71E472KA37	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	Depending on V_{OUT} (Note 2)	MCR01MZPF Series	Chip Resistor	ROHM
R_2	1005	Depending on V_{OUT} (Note 2)	MCR01MZPF Series	Chip Resistor	ROHM
R_4	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF Series	Chip Resistor	ROHM
C_3	OPEN	-	-	-	-
C_4	1005	Depending on V_{OUT} (Note 2)	GCM155R71E Series	Ceramic Capacitor	Murata
GAIN	-	Low	-	-	-

(Note 1) For more information on each mode, see Function explanations 6. Error Amplifier Gain Switching Function.
(Note 2) For the part parameters, see Selection of Components Externally Connected 3. Output Voltage Setting.

Application Characteristic Data (Reference Data) – continued

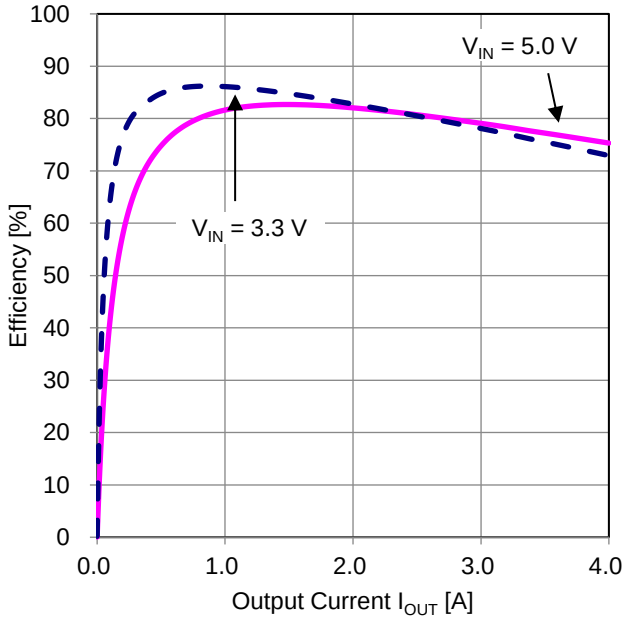


Figure 36. Efficiency vs Output Current
(V_{OUT} = 1.0 V)

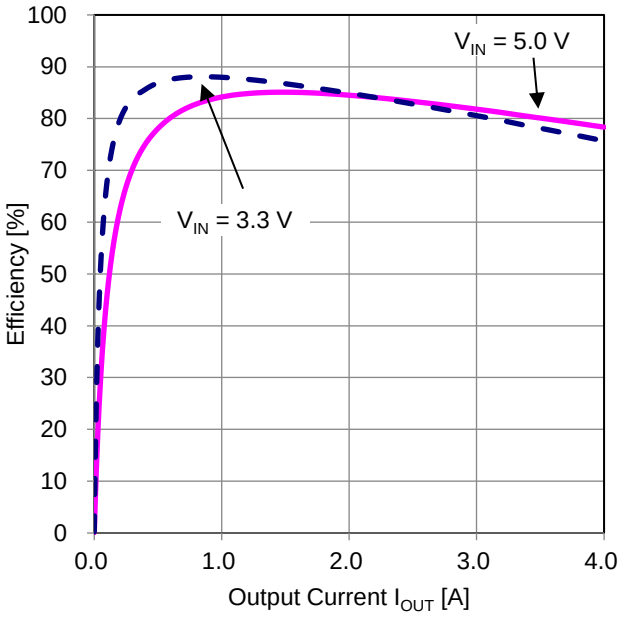


Figure 37. Efficiency vs Output Current
(V_{OUT} = 1.2 V)

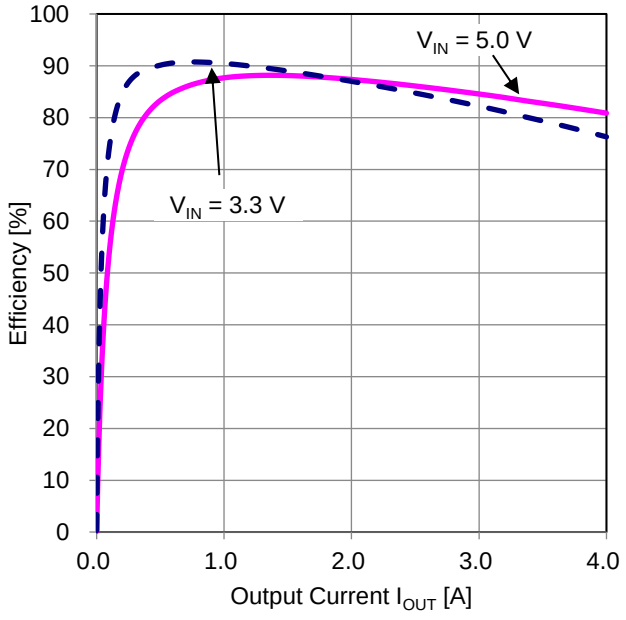


Figure 38. Efficiency vs Output Current
(V_{OUT} = 1.8 V)

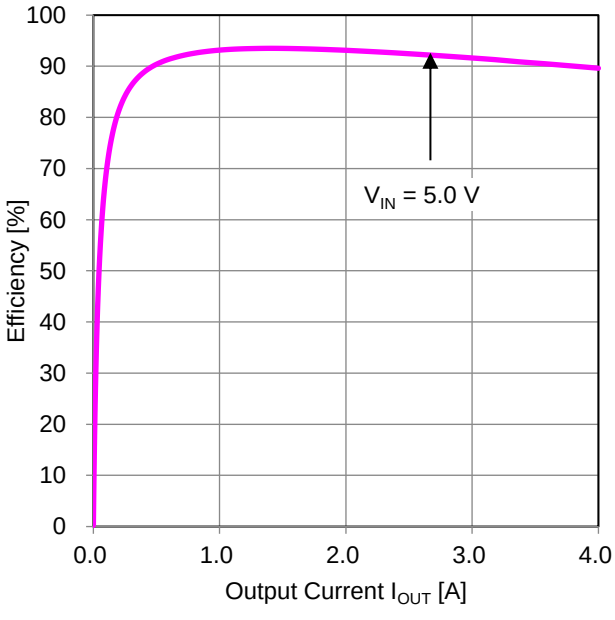


Figure 39. Efficiency vs Output Current
(V_{OUT} = 3.3 V)

Application Characteristic Data (Reference Data) – continued

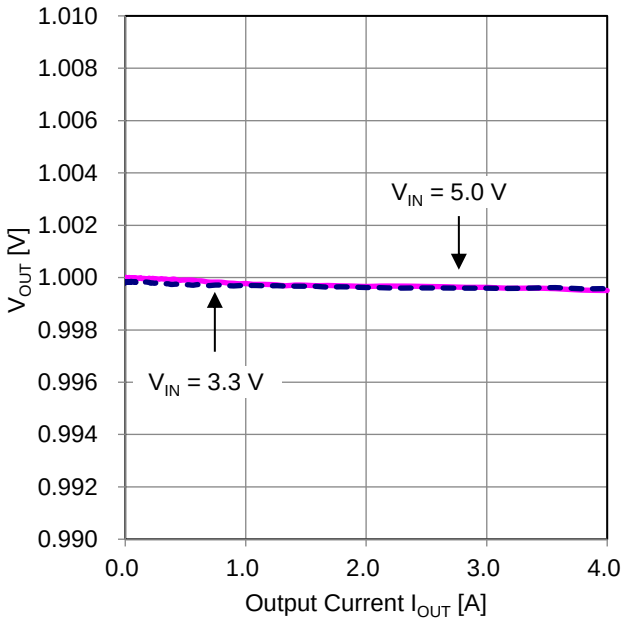


Figure 40. Output Voltage vs Output Current
(V_{OUT} = 1.0 V)

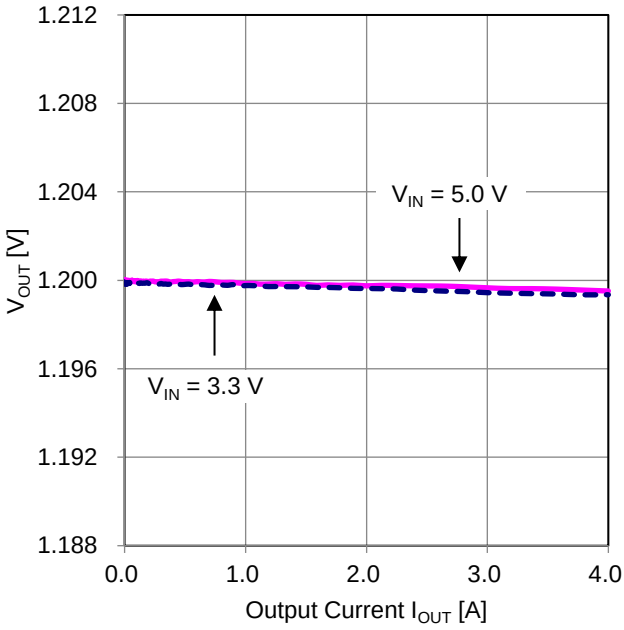


Figure 41. Output Voltage vs Output Current
(V_{OUT} = 1.2 V)

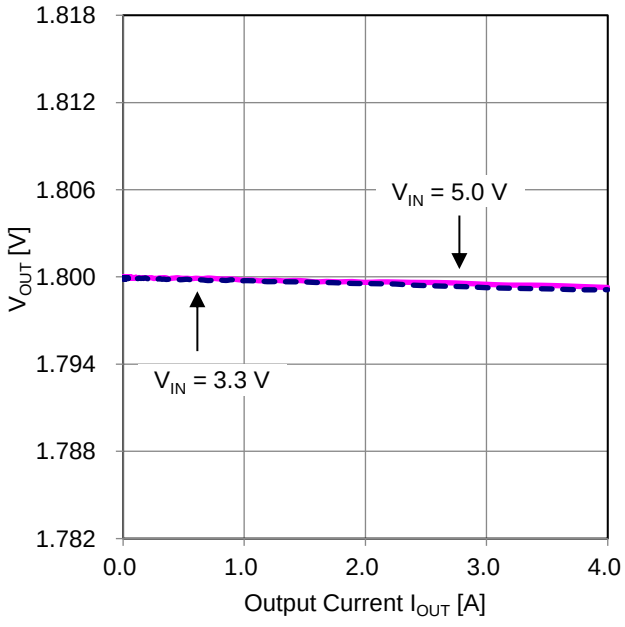


Figure 42. Output Voltage vs Output Current
(V_{OUT} = 1.8 V)

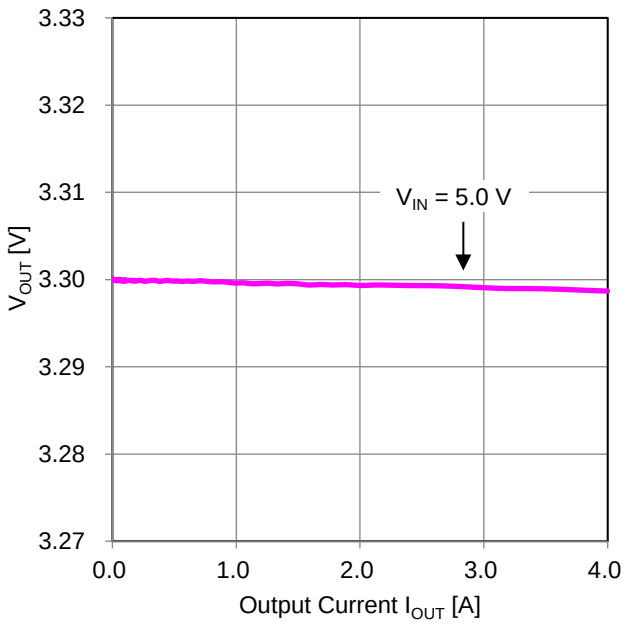


Figure 43. Output Voltage vs Output Current
(V_{OUT} = 3.3 V)

Application Characteristic Data (Reference Data) – continued

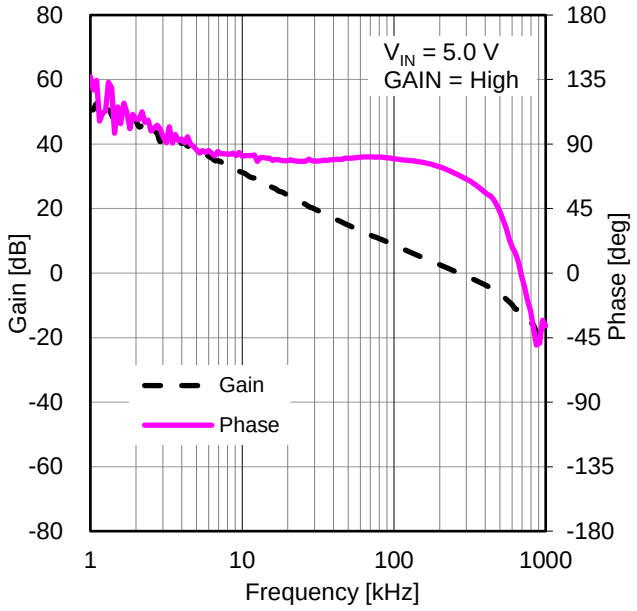


Figure 44. Frequency Characteristics
(V_{OUT} = 1.0 V, GAIN = High, I_{OUT} = 2 A)

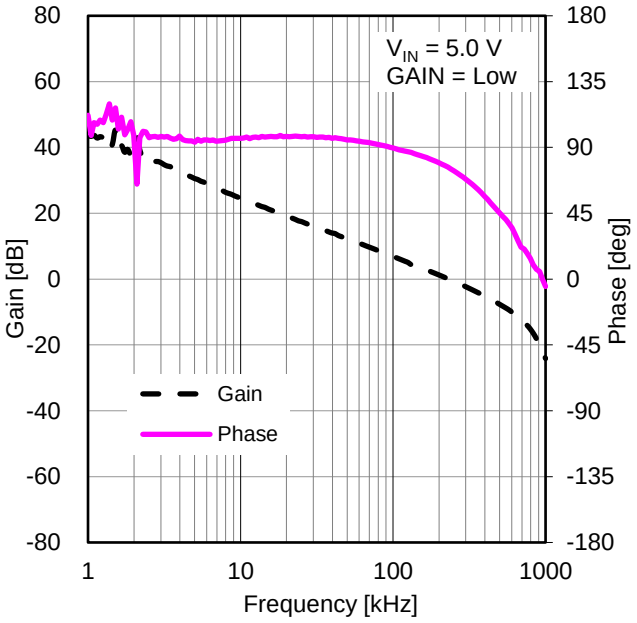


Figure 45. Frequency Characteristics
(V_{OUT} = 1.0 V, GAIN = Low, I_{OUT} = 2 A)

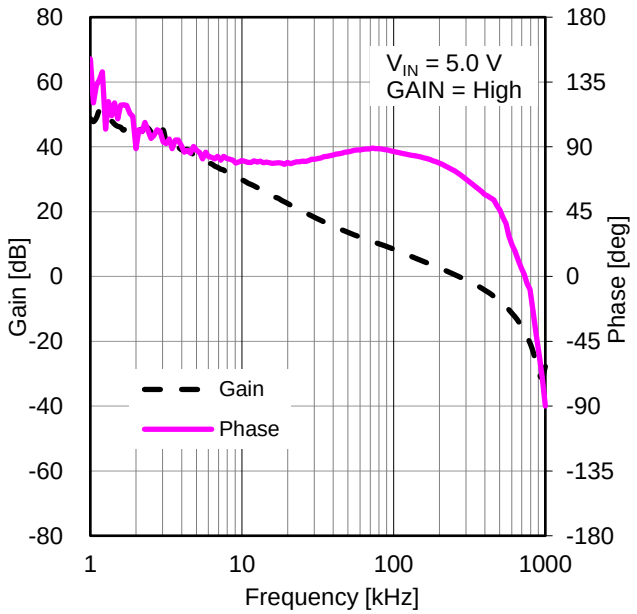


Figure 46. Frequency Characteristics
(V_{OUT} = 1.2 V, GAIN = High, I_{OUT} = 2 A)

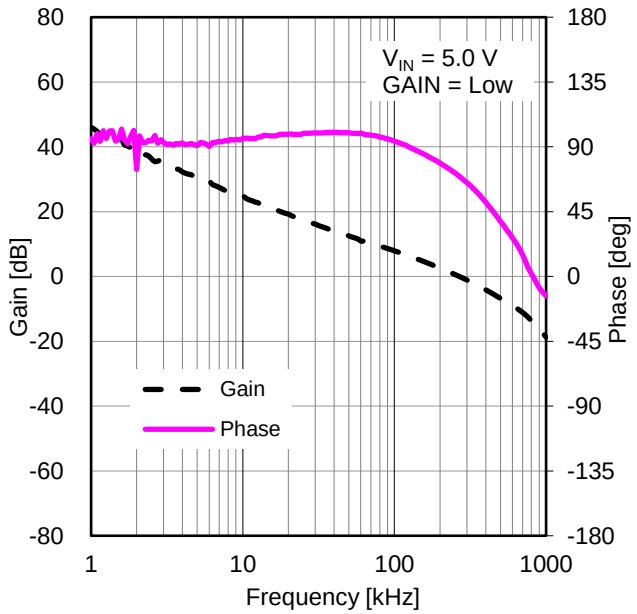


Figure 47. Frequency Characteristics
(V_{OUT} = 1.2 V, GAIN = Low, I_{OUT} = 2 A)

Application Characteristic Data (Reference Data) – continued

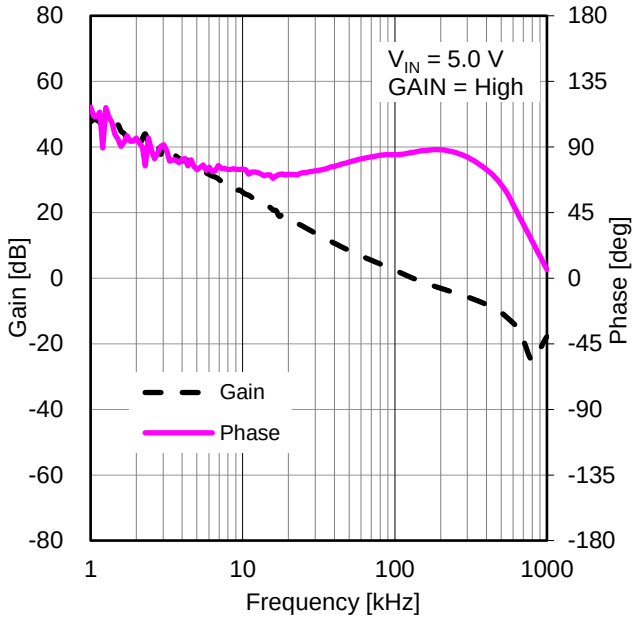


Figure 48. Frequency Characteristics
(V_{OUT} = 1.8 V, GAIN = High, I_{OUT} = 2 A)

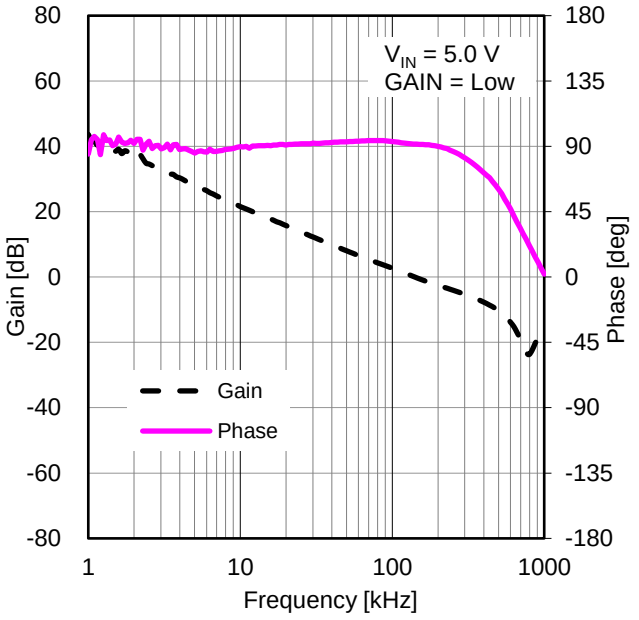


Figure 49. Frequency Characteristics
(V_{OUT} = 1.8 V, GAIN = Low, I_{OUT} = 2 A)

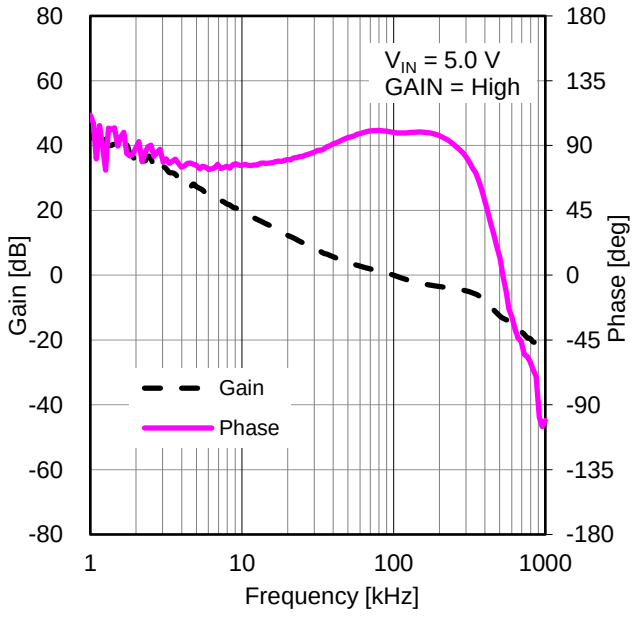


Figure 50. Frequency Characteristics
(V_{OUT} = 3.3 V, GAIN = High, I_{OUT} = 2 A)

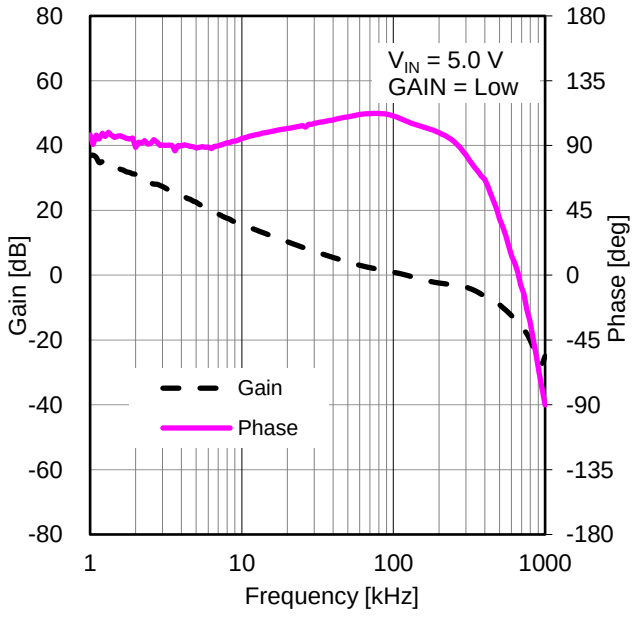


Figure 51. Frequency Characteristics
(V_{OUT} = 3.3 V, GAIN = Low, I_{OUT} = 2 A)

Application Characteristic Data (Reference Data) – continued

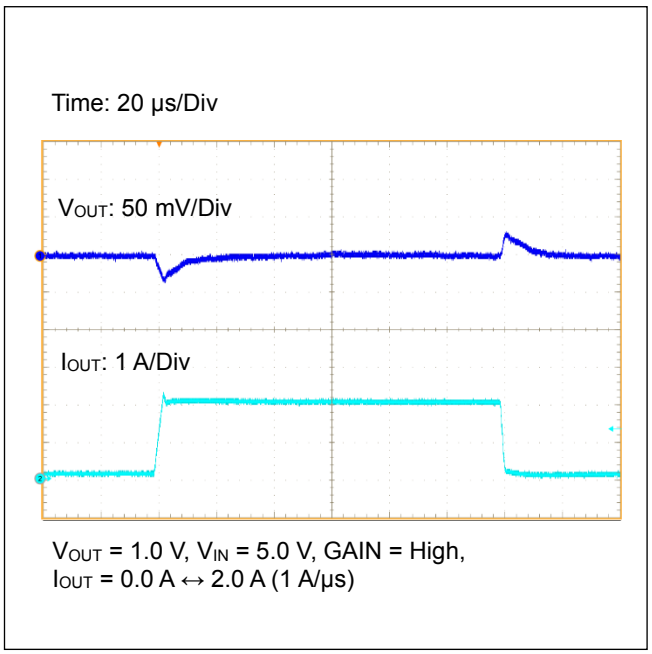


Figure 52. Load Transient Response
(V_{OUT} = 1.0 V, GAIN = High)

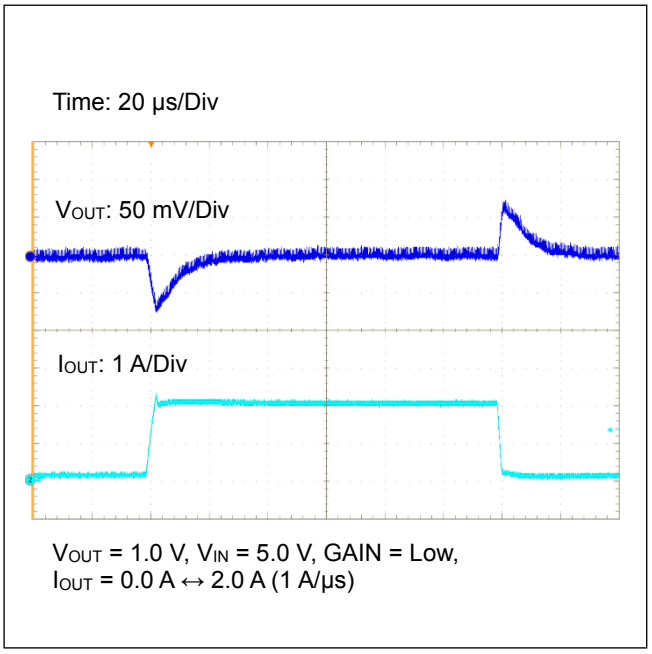


Figure 53. Load Transient Response
(V_{OUT} = 1.0 V, GAIN = Low)

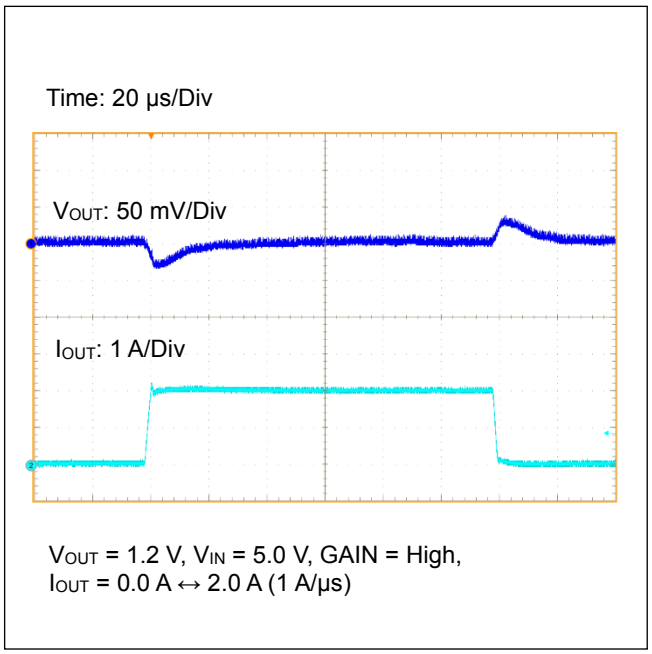


Figure 54. Load Transient Response
(V_{OUT} = 1.2 V, GAIN = High)

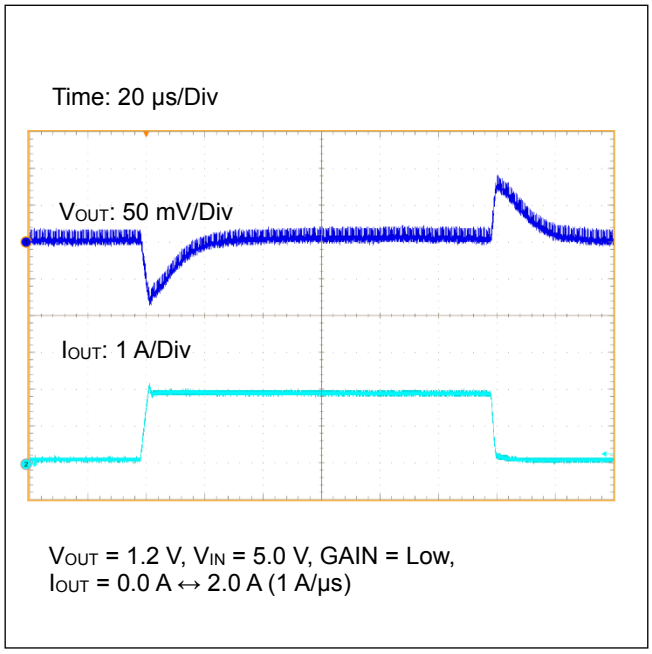


Figure 55. Load Transient Response
(V_{OUT} = 1.2 V, GAIN = Low)

Application Characteristic Data (Reference Data) – continued

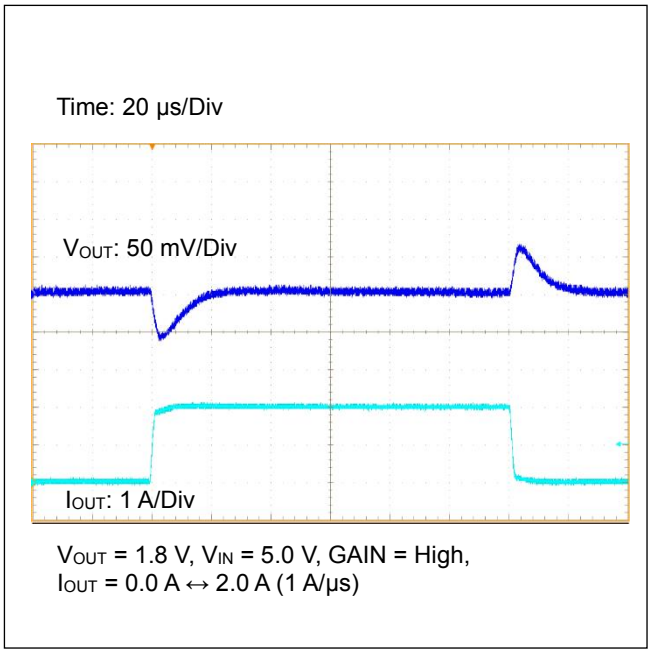


Figure 56. Load Transient Response
(V_{OUT} = 1.8 V, GAIN = High)

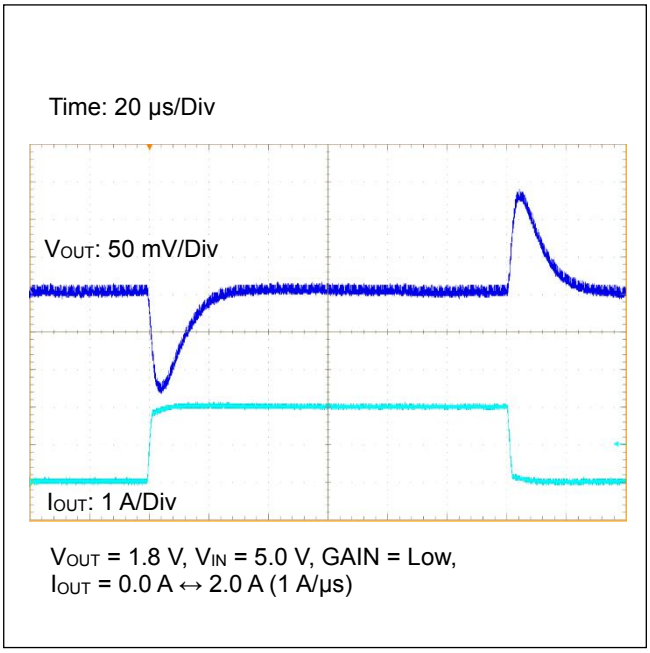


Figure 57. Load Transient Response
(V_{OUT} = 1.8 V, GAIN = Low)

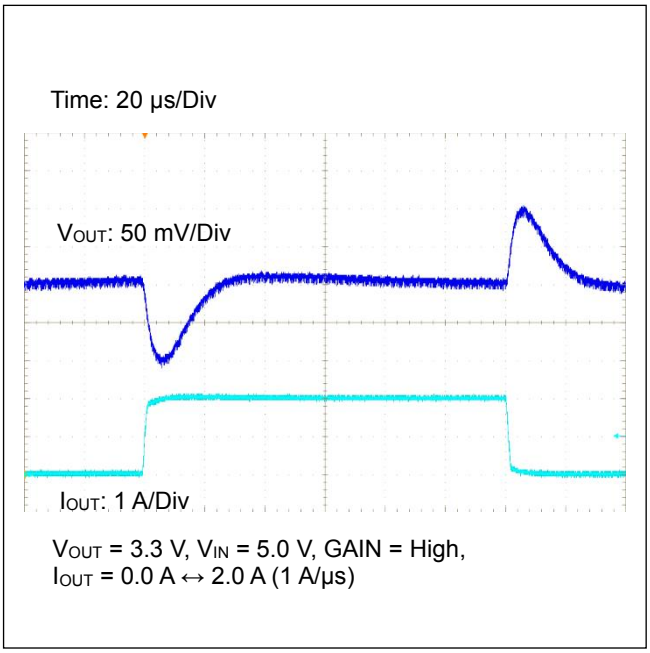


Figure 58. Load Transient Response
(V_{OUT} = 3.3 V, GAIN = High)

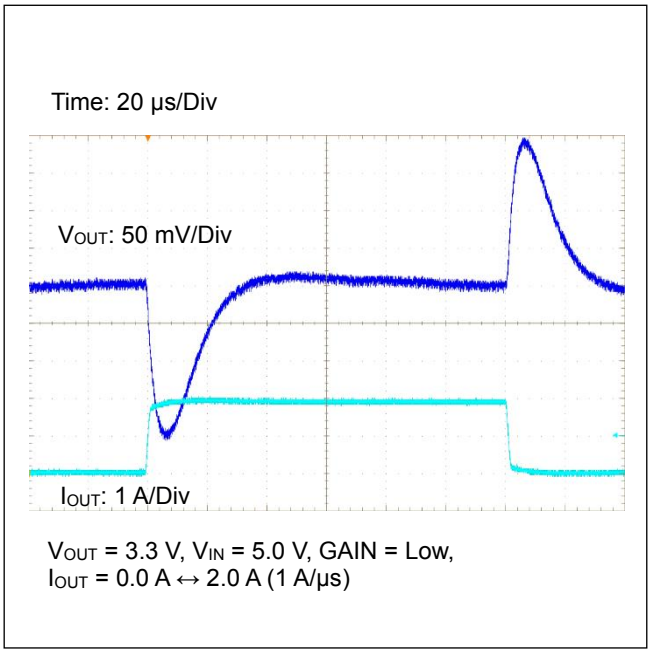


Figure 59. Load Transient Response
(V_{OUT} = 3.3 V, GAIN = Low)

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 60 to Figure 62 show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 60 is a current path when High Side Switch is ON and Low Side Switch is OFF, the Loop 2 in Figure 61 is when High Side Switch is OFF and Low Side Switch is ON. The thick line in Figure 62 shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element High Side and Low Side Switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

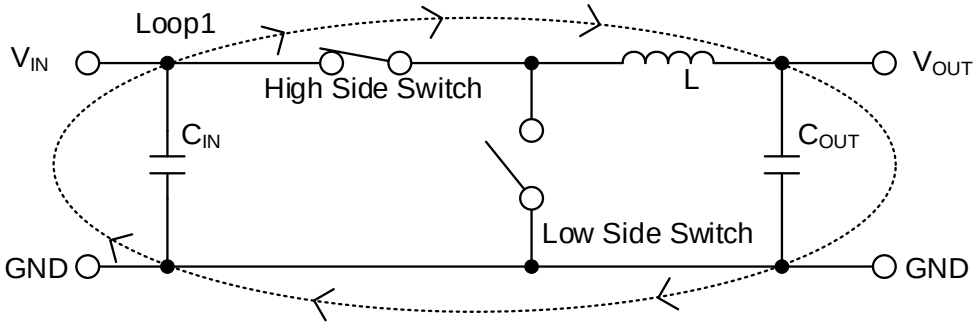


Figure 60. Current Path when High Side Switch = ON, Low Side Switch = OFF

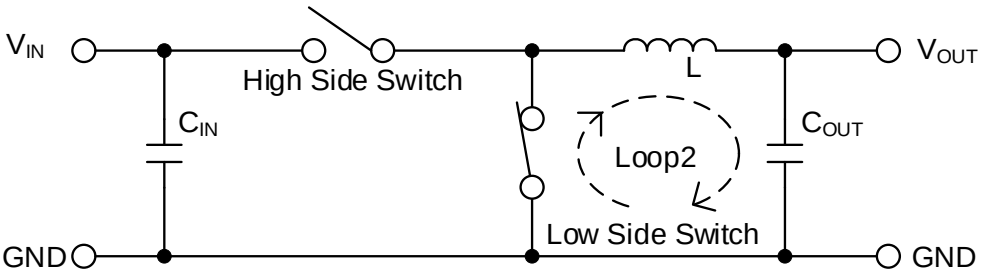


Figure 61. Current Path when High Side Switch = OFF, Low Side Switch = ON

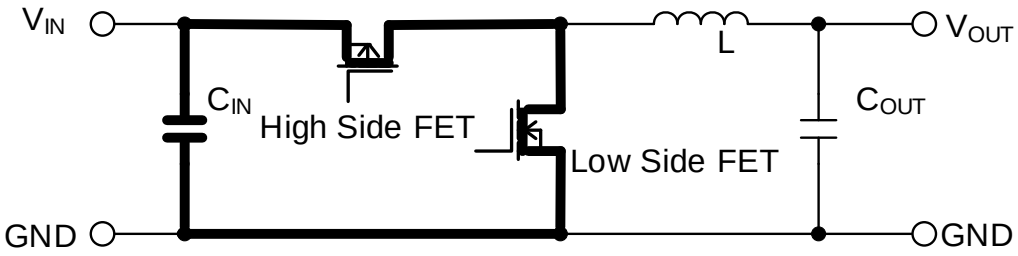
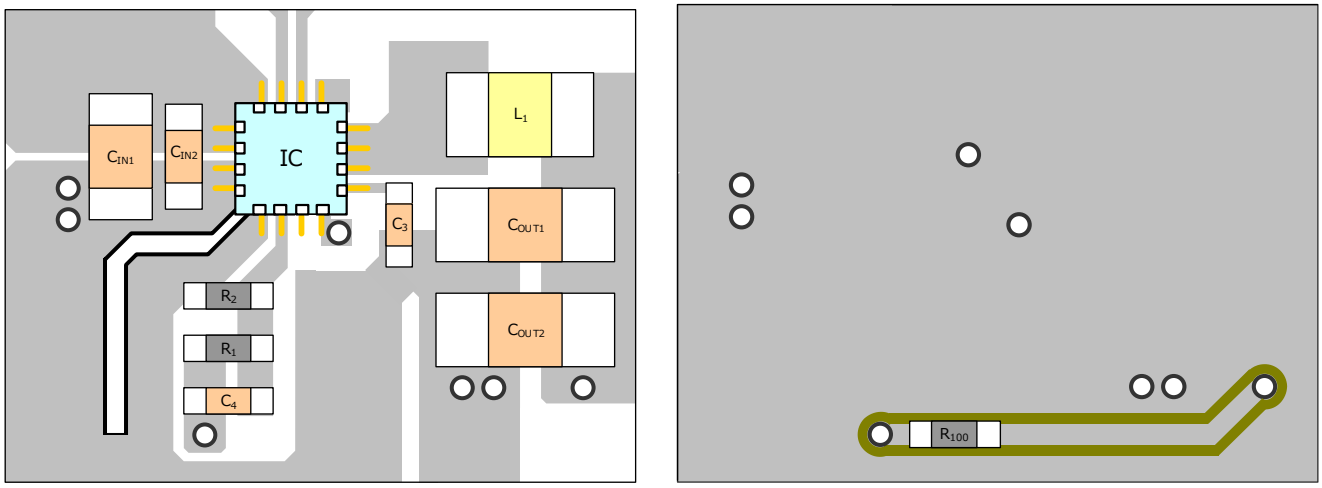


Figure 62. Difference of Current and Critical Area in Layout

PCB Layout Design – continued

When designing the PCB layout, Pay extra attention to the following points.

- Connect the input capacitor C_{IN} as close as possible to the PVIN pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern as thick and as short as possible.
- R_1 and R_2 shall be located as close as possible to the FB pin and the wiring between R_1 and R_2 to the FB pin shall be as short as possible.
- Provide line connected to FB far from the SW nodes.
- Influence from the switching noise can be minimized, by isolating Power (Input and Output Capacitor) GND and Reference (FB) GND.
- R_{100} is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_{100}, it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_{100} is short-circuited for normal use.



Example of Evaluation Board Layout (Top View)

Example of Evaluation Board Layout (Bottom View)

Figure 63. Example of Evaluation Board Layout

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

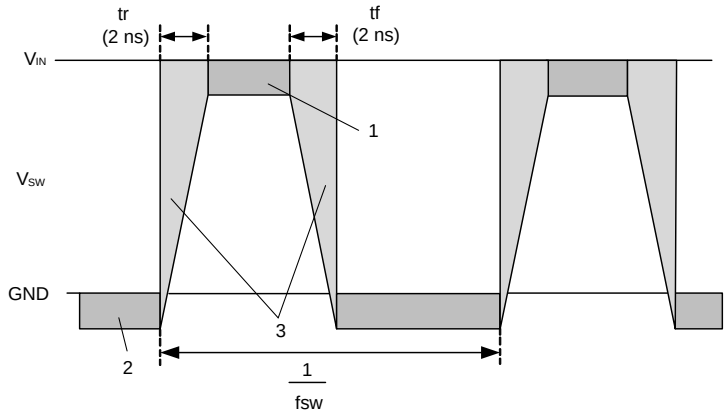
ψ_{JT} is junction to top characterization parameter (Thermal Resistance)
θ_{JA} is junction to ambient (Thermal Resistance)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

R_{ONH} is the High Side FET ON Resistance (Electrical Characteristics) [Ω]
R_{ONL} is the Low Side FET ON Resistance (Electrical Characteristics) [Ω]
I_{OUT} is the Output Current [A]
V_{OUT} is the Output Voltage [V]
V_{IN} is the Input Voltage [V]
I_{CC} is the Circuit Current (Electrical Characteristics) [A]
tr is the Switching Rise Time [s] (Typ: 2 ns)
tf is the Switching Fall Time [s] (Typ: 2 ns)
f_{SW} is the Switching Frequency (Electrical Characteristics) [Hz]

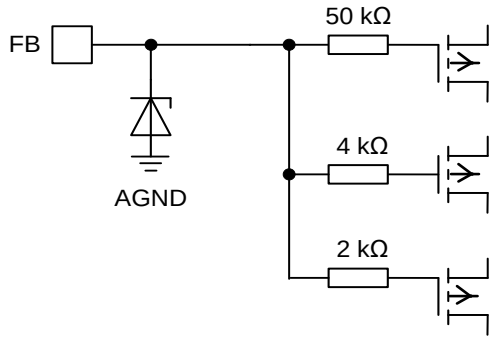


1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW}$

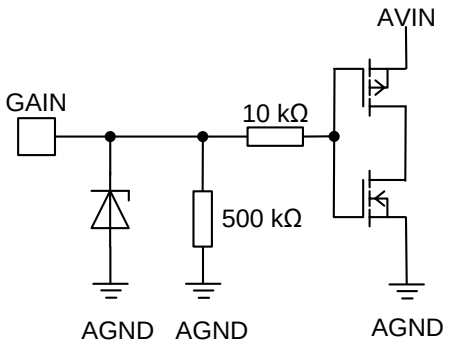
Figure 64. SW Waveform

I/O Equivalence Circuits *(Note 1)*

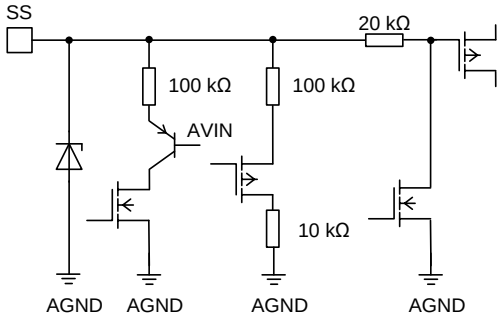
6. FB



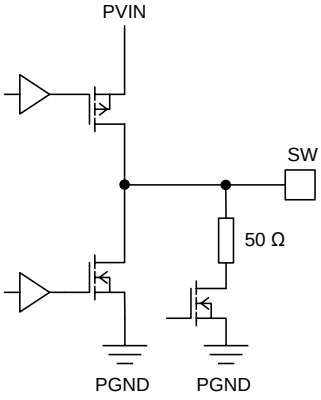
8. GAIN



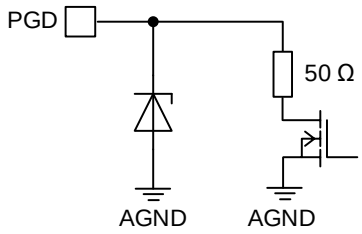
9. SS



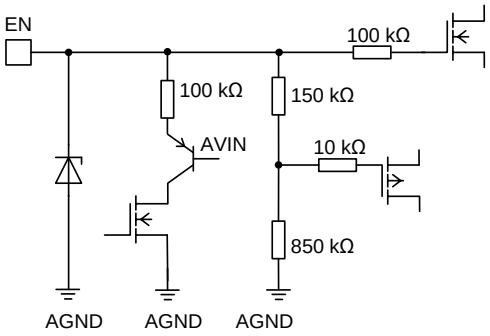
10.11.12. SW



14. PGD



15. EN



(Note 1) Resistance value is typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

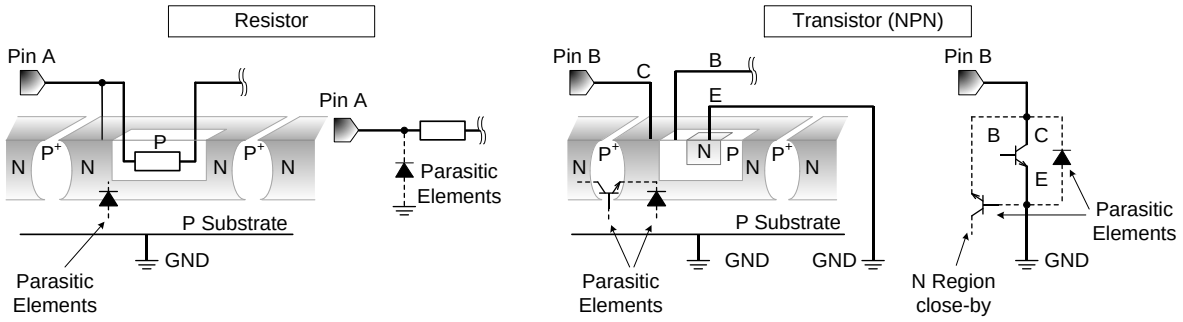


Figure 65. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

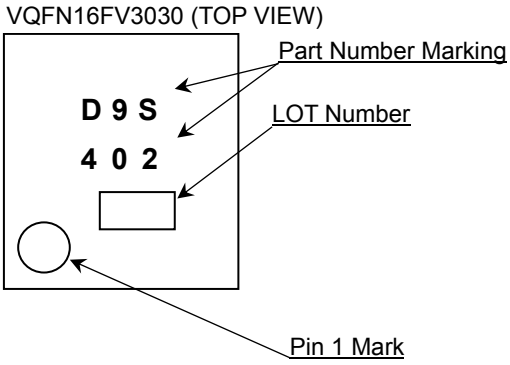
Ordering Information

B	D	9	S	4	0	2	M	U	F	-	C E 2

Package
MUF: VQFN16FV3030

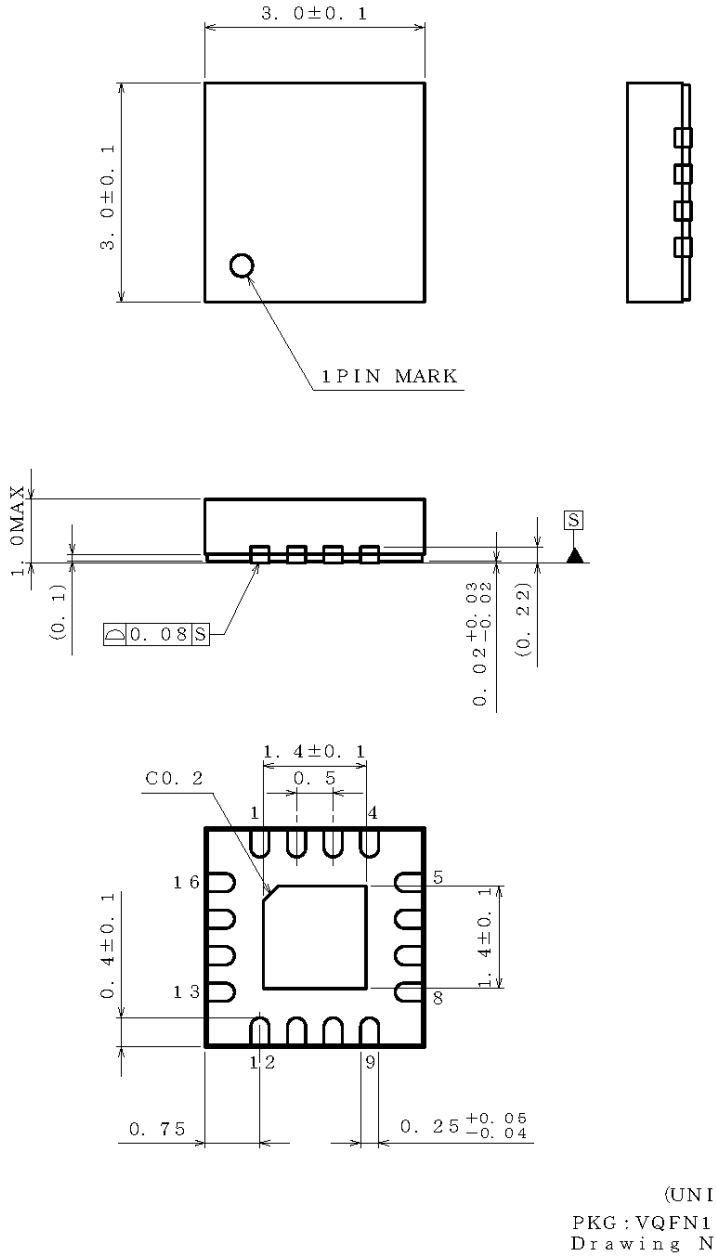
Product class
C for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN16FV3030

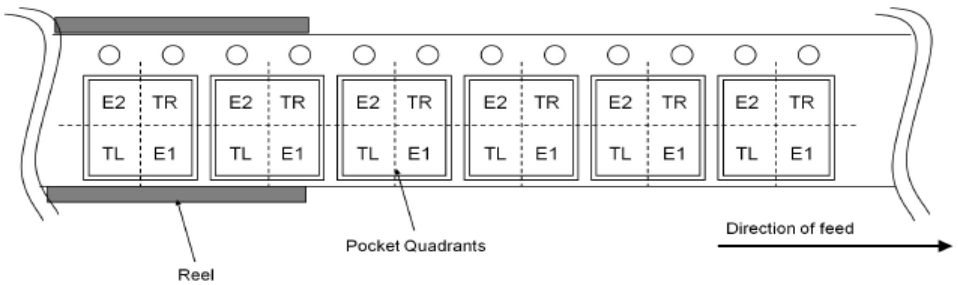


(UNIT:mm)
PKG:VQFN16FV3030
Drawing No. EX396-5001

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
10.May.2022	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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